Simulation and Analysis of Various parameters of Gate All Around Junction less Nano-wire FET

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Abstract— All existing transistors are based on the use of semiconductor junctions formed by introducing doping atoms into the semiconductor material. As the distance between junctions in modern devices drops below 10 nm, extraordinarily high doping concentration gradients become necessary. For this reason, a new device is proposed which has full CMOS functionality and is made by using nano-wires. They have near-ideal sub-threshold slope, extremely low leakage currents, and less degradation of mobility with gate voltage and temperature than classical transistors. Among several types of field effect transistor, gate all around junction less nano wire FET (GAA JL NW FET) is the recently invented one. In this paper, we analyze the Drain current characteristics of GAA JL NW FET with respect to the channel length for different materials such as Si, GaAs, InAs, InP and so on. We also analyze the threshold voltage of this newly invented FET for different materials and calculate for which material this voltage is minimum by MATLAB programming. Temperature dependency of this FET is also deeply analyzed.

Keywords — Temperature dependency, Short channel Effect, Effect of channel length.

1 INTRODUCTION

The junction less nano-wire transistor (JLNT) has become widely recognized as one of the most promising candidates for future nano-scale CMOS technology due to its excellent sub-threshold slope (SS), low drain-induced barrier lowering (DIBL) and low leakage current. But it has a disadvantage which is related to the carrier transportation or mobility. In general, carrier transport can be divided into three regimes: diffusive transport, ballistic transport, and quantum transport. When the gate length is much greater than the carrier mean free path, the carriers transit within the diffusive transport regime where scattering dominates. Carriers can reach their equilibrium states through sufficient scattering events and thus DD (Drift-Diffusion) model can capture well this equilibrium carrier transport property. When the gate length is shorter than the Broglie wavelength, the carrier transit within the quantum transport regime, where the full quantum transport approach such as NEGF is suitable to simulate strong quantum confinement and significant source to drain tunnelling. In the range between these two regimes, the carriers transit from quasi-ballistic to ballistic transport regime. The semi-classical approach Monte Carlo simulator incorporated with full band structure is able to capture the non-equilibrium transport effects.

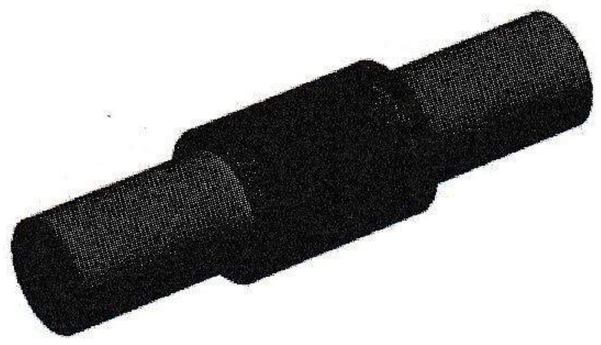

Fig. 1 Simulation structure of a cylindrical gate-all around junction less nano-wire transistor with 10nm gate length and 6nm diameter.

2 TEMPERATURE DEPENDENCY OF THRESHOLD VOLTAGE OF GAA JL NW FET

Temperature dependency of MOSFET

As with the case of oxide thickness affecting threshold voltage, temperature has an effect on the threshold voltage of a CMOS device. Expanding on part of the equation in the body effect section $\phi_F = (kT/q)$ In (N_A/N_i) Where ϕ_F is half the contact potential, k is Boltzmann's constant, T is Temperature, q is the charge of an electron, N_A is a doping parameter and N_i is the intrinsic doping parameter for the substrate.

We see that the surface potential has a direct relationship with the temperature. Looking above, that while the threshold voltage does not have a direct relationship but is not independent of the

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effects. On average this variation is between −4 mV/K and −2 mV/K depending on doping level. For a change of 30 °C this results in significant variation from the 500 mV design parameter commonly used for the 90 nm technology node.

Temperature dependency of GAA JL NW FET

For the gate all around junction less nano-wire field effect transistor, the equation stands for the threshold voltage depends upon the work function, Radius of device, thickness of oxide and the permittivity of oxide and material we used.

$$V_{th} = \Delta\varphi + \frac{kT}{q}\ln\left(\frac{8}{\delta}\right) - \frac{2kT}{q}\ln\left(R\left(1+\frac{t_{ox}}{R}\right)^{\frac{2\epsilon_r}{\epsilon_{ox}}}\right) \quad [1]$$

Where the V_{th} is the threshold voltage, $\Delta\varphi$ is the difference of work function, k is the Boltzmann's constant, T is the temperature which is varied, q is the charge of electron, R is the radius of gate all around junction less nano-wire device, t_{ox} is the thickness of oxide used, ϵ_{ox} is the permittivity of oxide used and the ϵ_r is the permittivity of material which is varied for different material.

$$\delta = \frac{q^2 n_i}{KT\epsilon_r} \quad [2]$$

In which,

$$n_i = 5.2 \times 10^{15} \times T^{\frac{3}{2}} \times e^{-\frac{E_g}{2kT}} \quad [3]$$

The graph for V_{th} with respect to the temperature T for different material is,

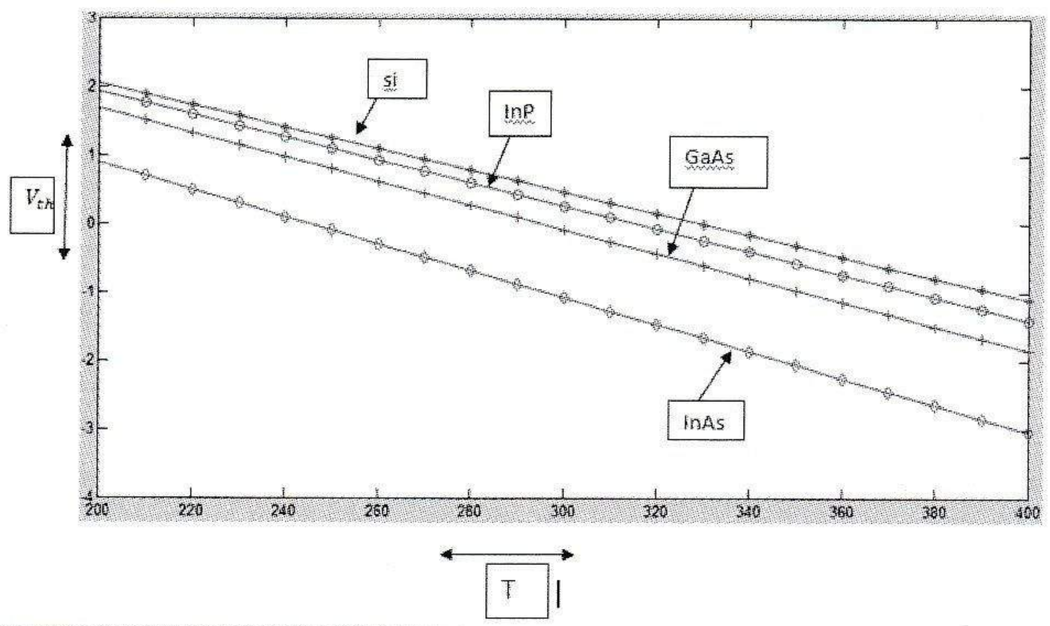

Fig. 2 Threshold voltage Vs temperature for GAA JL NW FET

Effect of channel length of GAA JL NW FET

A MOSFET device is considered to be short when the channel length is the same order of magnitude as the depletion-layer widths (x_{dD},x_{dS}) of the source and drain junction. As the channel length L is reduced to increase both the operation seed and the number of components per chip, the so-called short-channel effects arise.

Short-Channel Effects

The short-channel effects are attributed to two physical phenomena:

1. The limitation imposed on electron drift characteristics in the channel,
2. The modification of the threshold voltage due to the shortening channel length.

In particular five different short-channel effects can be distinguished:

1. Drain-induced barrier lowering and punch-through
2. Surface scattering
3. Velocity saturation
4. Impact ionization
5. Hot electrons

Channel length Vs Drain current of GAA JL NW

The relationship between the channel length and the drain current of GAA JL NW FET is

$$I_d = \mu C_{ox}\frac{W_{ch}}{L}(V_{dd} - V_{th})^2 \quad [4]$$

Where the I_d is the drain current, μ is the mobility of electron in GAA JL NW FET which is assumed 50%. W_{ch} is the width of channel, L is the channel length, V_{dd} is the supply voltage and the V_{th} is the threshold voltage.

- **Process parameters of Junctionless GAA** [5]

Gate length (Lg)	17 nm
Diameter (D) of nanowire	5 nm
Gate oxide thickness (Tox)	0.77 nm
Channel doping (Nch)	$6 \times 10^{19} cm^{-3}$
Source/drain doping (Nsd)	$6 \times 10^{19} cm^{-3}$
Gate work function (WF)	4.63
Supply voltage (Vdd)	0.8 V

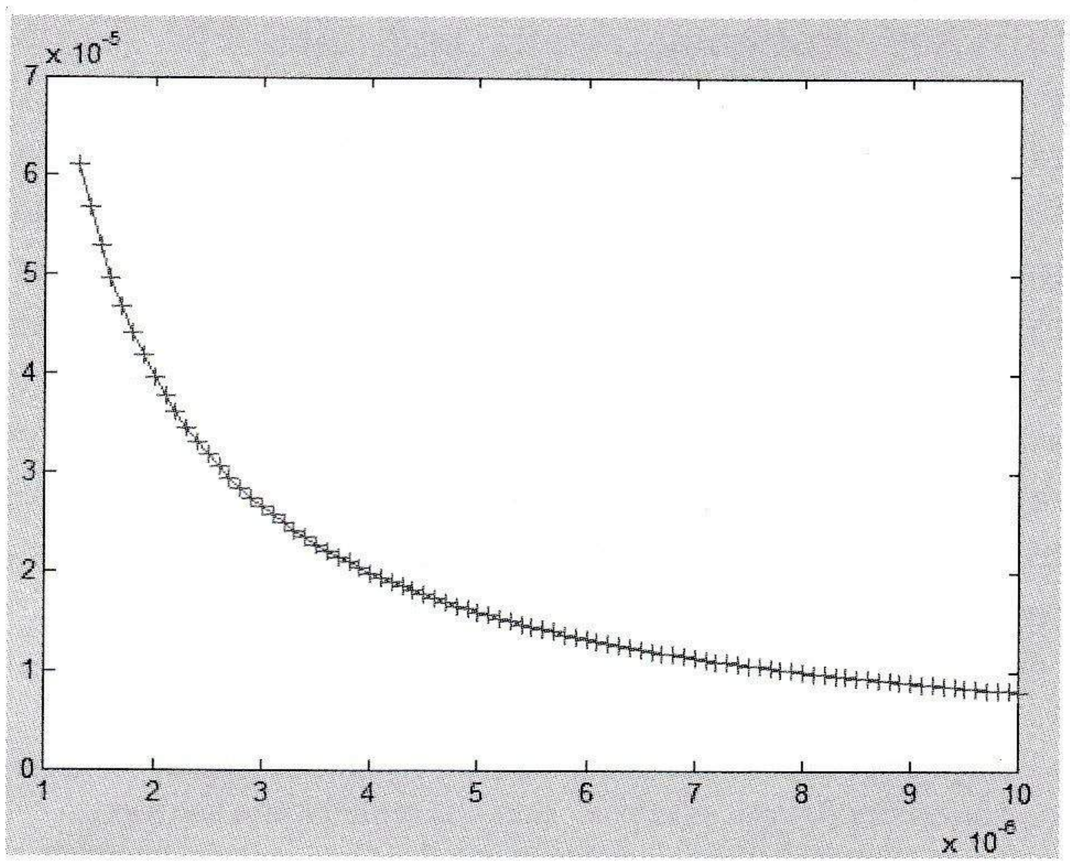

Fig. 3 channel length Vs drain current for silicon material. ($\epsilon_r = 11.7, E_g = 1.12$)

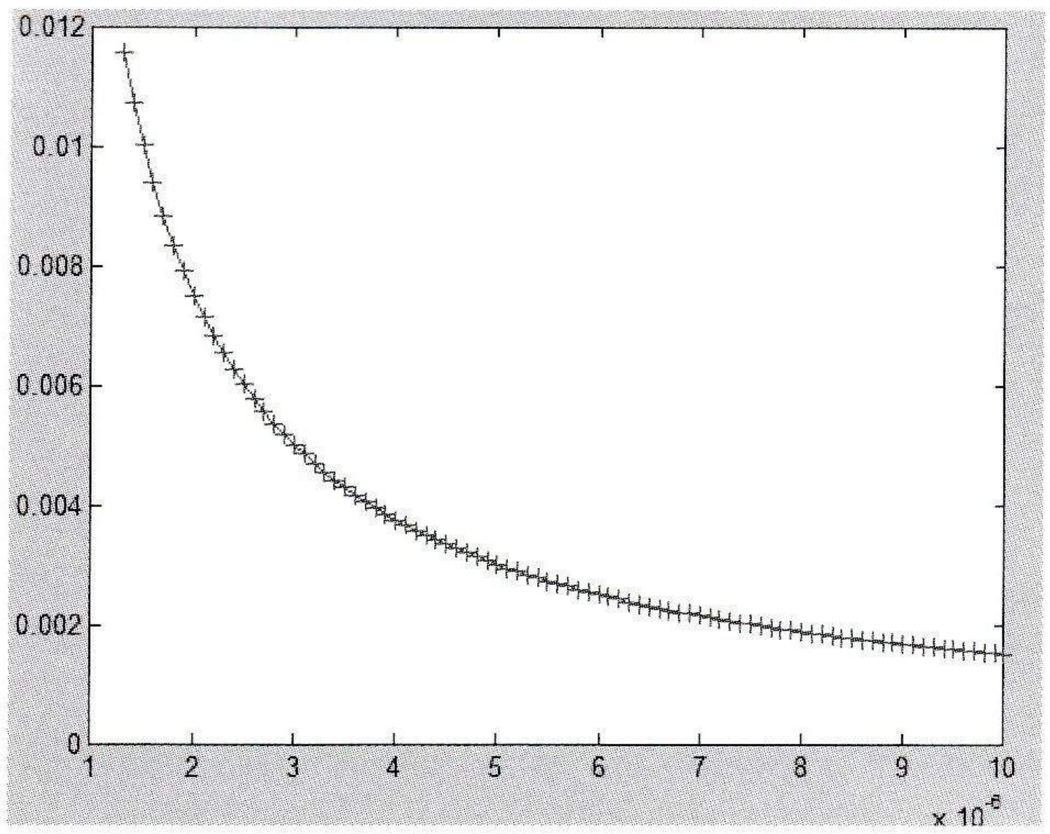

Fig.4, The drain current Vs channel length for GaAs. (ϵ_r= 13.1, E_g = 1.43)

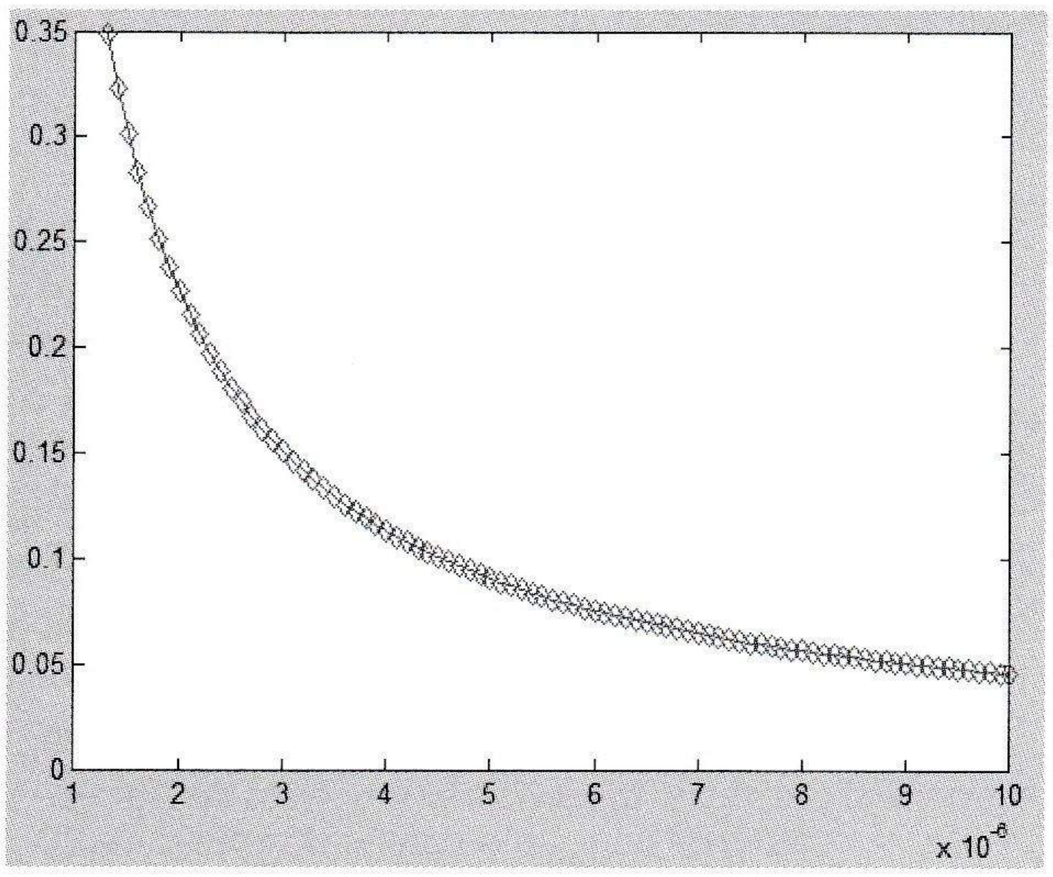

Fig.5, The drain current Vs channel length for InAs. (ϵ_r= 14.6, E_g = 0.36)

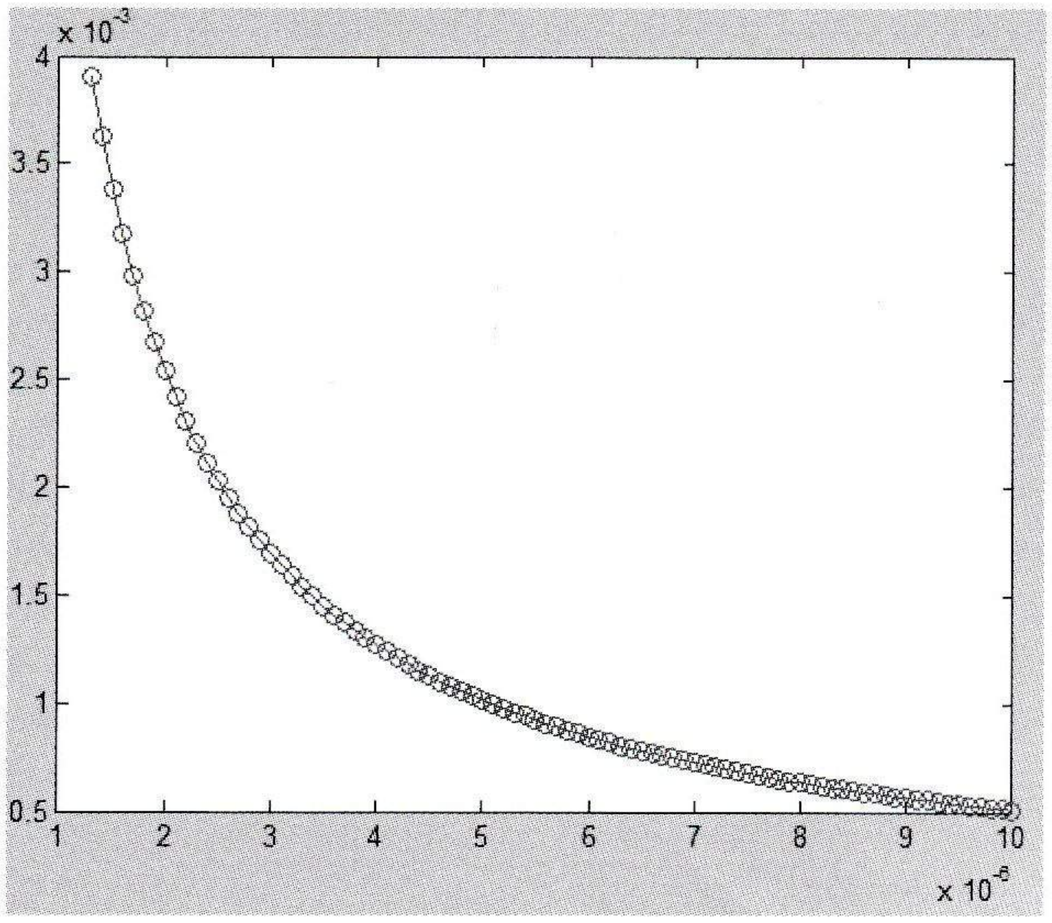

Fig.6, The drain current Vs channel length for InP. (ϵ_r= 12.4, E_g = 1.27)

From the above analysis of graph for different materials, we found the highest drain current for those materials which has less band gap energy and higher relative permittivity with same length.

2. RESULTS & DISCUSSION

In this work , we use silicon which has band gap energy Eg =1.12 and relative permittivity ϵ_r=11.7, gallium arsenide GaAs has Eg=1.43 and ϵ_r=13.1, indium arsenide InAs has Eg= 0.36 and ϵ_r=14.6 and finally indium phosphate has band gap energy Eg= 1.27 and relative permittivity ϵ_r=12.4.

In the figure 2, we found the lowest threshold voltage for InAs because it has lowest band gap energy and highest relative permittivity that we inputted.

In the figure 3, 4, 5 and 6, we see that the drain current is also maximum for InAs for the same reason.

3. CONCLUSION

Due to the aggressive scaling of transistor these has become of nano-meter sizes. At these sizes it is very hard to control the sharp source/drain-channel junctions' from the device fabrication point of view. Also many other unwanted deleterious effects such as gate leakage, short channel effects (SCEs), hot carrier effects (HCEs) etc. have been seen to be increasing. For reducing the short channel effects the gate all around FETs are the best since these provide best control over the channel from all around.

In this work, we deeply analyze the threshold voltage, drain current, temperature effect, channel length, short channel effect and various parameters of gate all around junction less nano-wire FET by using different materials such as silicon, gallium arsenide, indium arsenide, indium phosphite and so on.

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