Deviation of Ballistic Mobility in Response to Different Channel-Lengths in Quantum-Well FET

A. Arefin

Abstract— To quantify the power performance advantage of short channel III-V devices with respect to current state of the art strained Si and the role of effective carrier velocity in the channel have been investigated. Effect of channel length on carrier mobility and importance of quantum technology to develop transistors have been shown in this work. Finally, the ballistic mobility using various compound semiconductor materials such as InAs, InGaAs, InSb, InP and GaAs have been simulated. After analyzing the simulation result, the conclusion may be drawn that the mobility increases linearly if the channel length is reduced. Moreover, a higher mobility can be obtained by using a channel material having a lower effective mass.

Keywords — Ballistic mobility, channel length, quantum-well, quantum-well FET.

1 INTRODUCTION

As semiconductor technology continues to scale down in accordance with Moore's Law to nanoscale, the quantum effect is becoming more and more prominent [1]. Researchers are inventing and investigating new types of devices keeping quantum phenomena in mind. Among these nanodevices, III-V compound semiconductor based Quantum-Well FETs (QWFETs) have been proposed as a promising device option because of high-speed switching at very low supply voltages enabled by the excellent low- and high-field electron transport properties of III-V semiconductors [2].

Researchers are trying to develop the performance as well as reduce the size of all types the transistors more for as a demand of modern semiconductor industries. With the reduced channel length, ballistic transport is having more domination on channel current [3]. So now device performance is mostly dependent on the mobility of the material in the channel region [4]. Besides, channel length has also a great effect on this mobility.

In this research, the dependency of ballistic mobility on the channel length has been studied, simulated and investigated. In the simulation, channel length had a wide variation of around 20 nm. Five different channel materials, such as, InAs, InGaAs, InSb, InP and GaAs, have been brought under consideration for a better analysis.

Department of Electrical & Electronic Engineering, Northern University Bangladesh

2 QUANTUM WELL AND QUANTUM-WELL FET

Quantum wells, quantum wires and quantum dots are the basic building blocks of modern nanoelectronic devices. If the sizes of the materials are reduced, electrons can be confined and controlled more and more activities can be done at very low voltage and current levels. Most of the nanoelectronic devices are based on the semiconductor nanostructures, fabricated by tailoring the band gaps of desired level. Quantum well is the best answer of this bandgap engineering.

The term "well" in semiconductor refers to a region that is grown to possess a lower energy, so that it acts as a trap for electrons. They are referred to as "quantum" wells because these semiconductor regions are only a few atomic layers thick. In addition, that their properties are governed by quantum physics, allowing only specific energies and band gaps [5]. Because QW structures are very thin, they can be modified very easily. In short, a QW is a potential well with only discrete energy values.

QW consists of an extremely thin semiconductor, usually between 1 and 20 nm, with a small bandgap resting between materials with bandgaps too wide for electrons to jump easily (examples: GaAs QW embedded in AlGaAs, or InGaAs in GaAs).

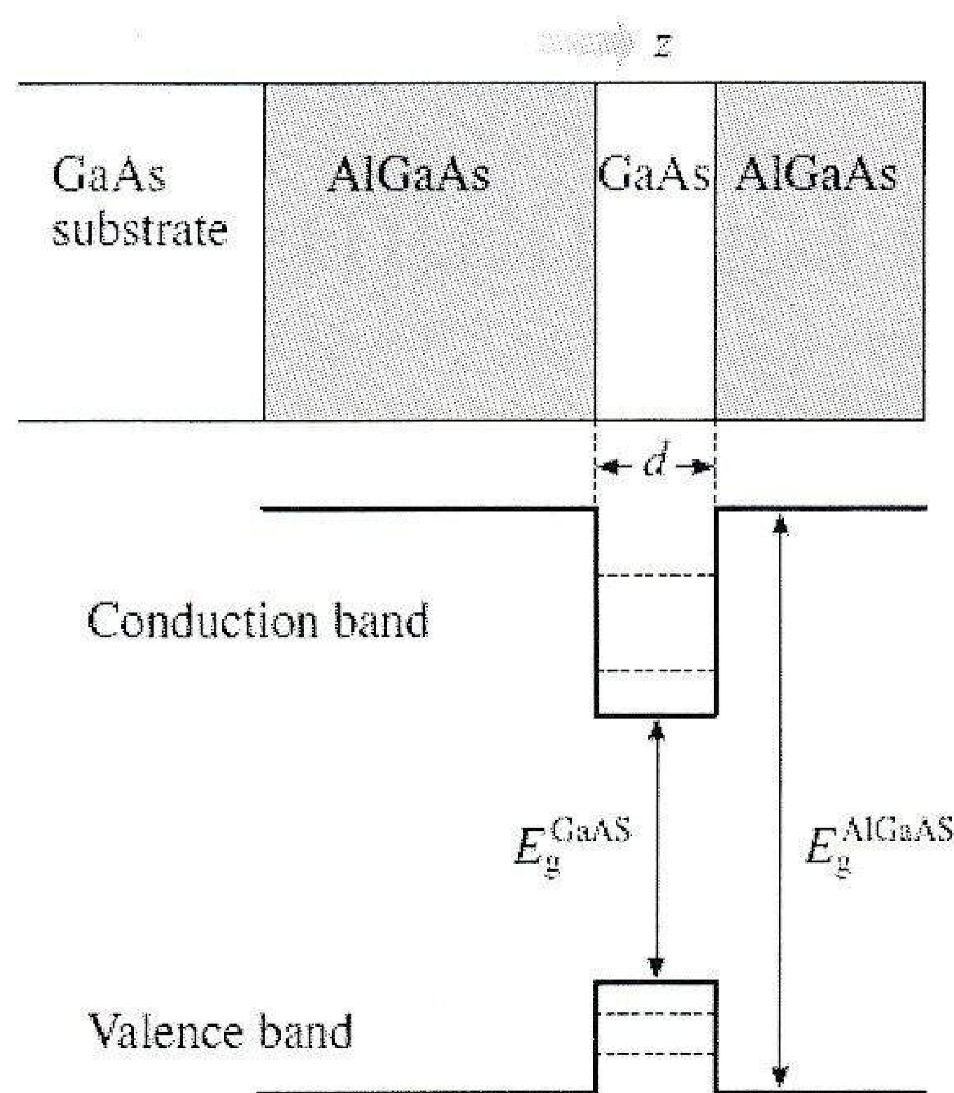

Fig. 1 GaAs QW in AlGaAs [5].

This well uses the properties of electron behavior and bandgaps to work. By placing a microscopically thin semiconductor, the electrons can be forced to remain in the two-dimensional area of this thin semiconductor, which is illustrated in Fig. 1. Trapping electrons in this manner allows for specific energy manipulation. QW can confine charges in the dimension perpendicular to the layer surface, whereas the movement in the other dimensions is not restricted.

By adjusting the aluminum content of the barrier layers and the thickness of the GaAs layer at the time of growth, the electronic properties of QWs can be changed to the user's specifications. This practice is referred to as quantum engineering.

Quantum engineering has given the researchers freedom to manipulate the properties of nanodevices. Gradually QW based devices have been invented. These devices are being very popular for their low-power and high-mobility applications.

For the heterogeneous integration of high-performance InGaAs, InAS, InSb, InP, GaAs and other kind of compound semiconductor material QWFET on Si substrate will allow low-voltage, high-speed III-V based logic circuit blocks to couple with the main stream Si CMOS platform for future microprocessor applications [6].

AlInAs QWFET is schematically shown in Fig. 2. The channel region is composed of a 10 nm $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ (2/5/3 nm, from top to bottom) QW grown on a 500 nm thick $In_{0.52}Al_{0.48}As$ layer lattice matched to InP. The $In_{0.52}Al_{0.48}As$ layer between the quantum-well channel and the gate contact acts as an insulator or barrier. A Si δ-doped layer situated 0.3 nm below the gate contact supplies the channel conduction electrons. The source/drain contacts are located on the top of the device almost 1 μm away from the gated region [7].

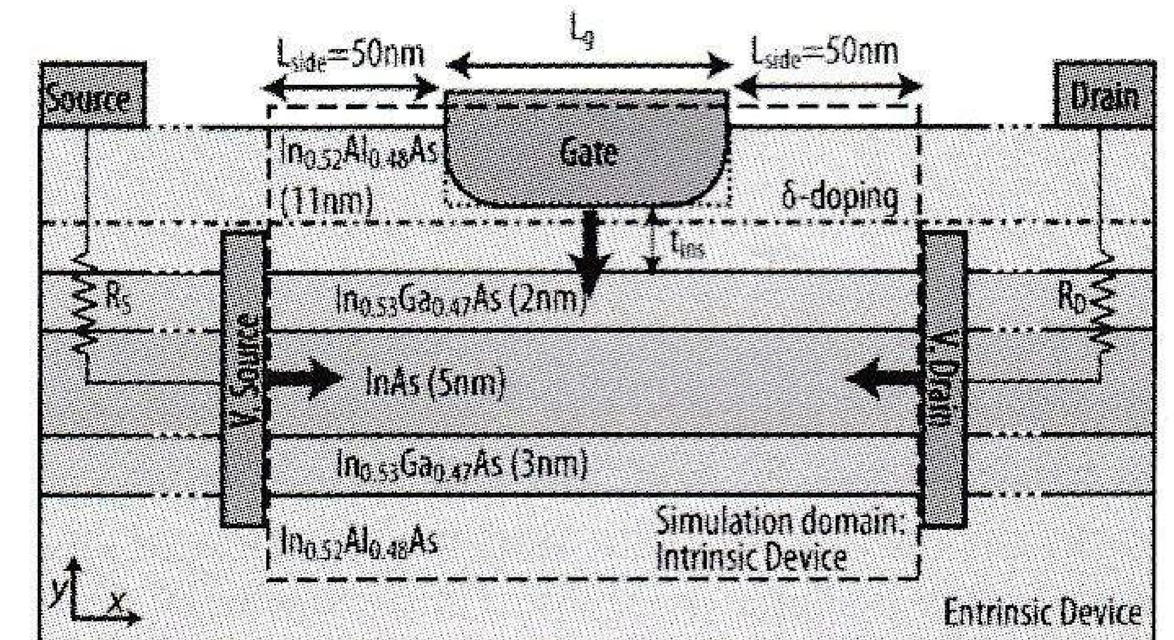

Fig. 2 Structure of InAs QWFET [8].

Fig. 3 shows a cross-section of a p-channel InGaSb QWFET. The heterostructure was grown on a semi-insulating GaAs substrate. Growth of the structure began with a relaxed $Al_{0.70}Ga_{0.30}Sb$ buffer 1.5 μm thick, followed by a 5 nm layer doped with Be and 21 nm of undoped $Al_{0.70}Ga_{0.30}Sb$. Then, a 7.5 nm $In_{0.40}Ga_{0.60}Sb$ channel layer is grown along with a 7 nm thick barrier comprised of 3 nm of $Al_{0.70}Ga_{0.30}Sb$ and 4 nm of $In_{0.20}Al_{0.80}Sb$. Finally, the heterostructure is capped off by a highly-doped bilayer of $In_{0.85}As_{0.15}Sb$ (30 nm) with InAs (5 nm) on top with Be [9].

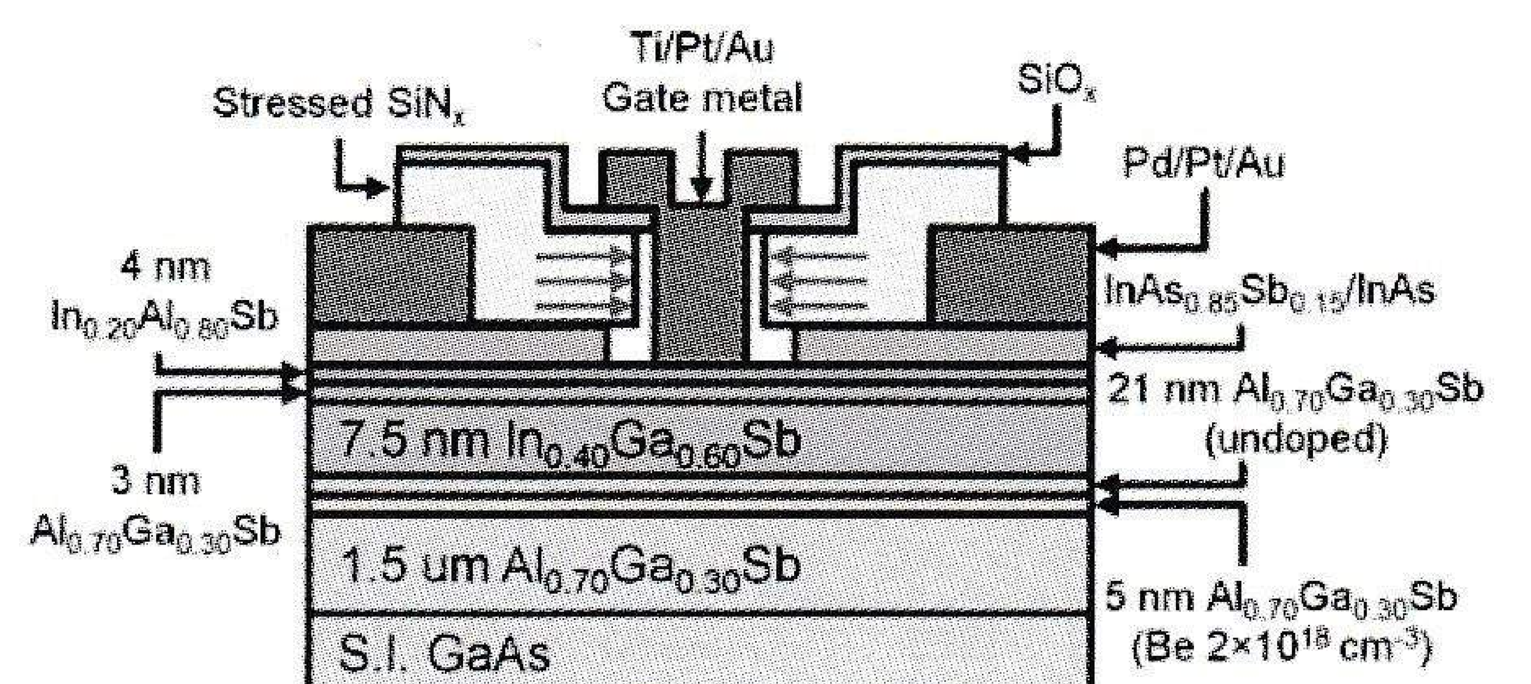

Fig. 3 Structure of a p-channel InGaSb QWFET [9].

3 Carrier Mobility In QWFET

Aggressive supply voltage scaling to 0.5 V and below while maintaining transistor performance is a direct path toward reducing power consumption. This goal can be achieved by using suitable materials in the channel with better carrier mobility. So the calculation of this carrier mobility is a very important part of any research regarding nanodevices.

As shown in the previous two examples, the channel lengths of QWFETs are around a few tens

of nanometers. In these low-dimension nanodevices carriers do not transport in conventional approach. Rather, they experience a technique known as ballistic transport [10], [11]. Ballistic transport refers to the motion of electrons through the semiconductor material in the complete absence of collisions [12].

Various researches are being undergone to calculate the carrier mobility due to ballistic transport in nanodevices accurately. 2D numerical simulation self-consistently solves the Poisson's equation with carrier continuity equation using a drift-diffusion model. To accurately capture the non-equilibrium carrier transport (such as velocity overshoot effect), the Canali mobility model may be employed [13].

$$\mu(E) = \frac{\mu_{low}}{\left[1 + \left(\frac{(\alpha+1)\mu_{low}E}{v_{sat}}\right)^{\beta}\right]^{\frac{1}{\beta}}}$$

Here, μ_{low} is the low field mobility, v_{sat} is the saturation velocity and β is a constant reflecting the steepness of carrier mobility profile in the channel. For example, $\mu_{low(In0.7Ga0.3As)}$ = 12000 cm^2/V.s and $\mu_{low(In0.53Ga0.47As)}$ = 10000 cm^2/V.s and for electrons, $v_{sat} = 0.93\times10^7$ cm/s and $\beta = 2$ [14].

As the device dimension is scaled down, unlike Si MOSFETs with moderate mobility values, QWFETs with III–V compound semiconductors possess high electron mobility up to 15000 cm^2/Vs or even higher. For example, $In_{0.7}Ga_{0.3}As$ QWFET has a low-field electron mobility of 12000 cm^2/Vs with carrier density of 2×10^{12} cm^{-2} in the channel and thus, its mean-free-path is calculated to be approximately 150 nm. Therefore, QWFETs with gate-length approaching 15 nm are expected to operate close to the ballistic limit [10] across a range of operating bias conditions. In order to quantify the significance of ballistic transport, the short-channel mobility of QWFETs has been investigated in detail [15].

The high carrier mobility in long channel III-V based QWFET arises from a combination of its low electron mass, reduced Columbic scattering and lower interface roughness scattering. In the short-channel QWFETs, electrons are launched with thermal velocity (V_{th}) from source into the channel and pass through the channel encountering few collisions. In such a scenario, the actual channel resistance is weakly dependent on the physical gate length of the device. In this respect, the effective carrier mobility for short-channel devices operating close to the ballistic limit is primarily limited by the ballistic mobility, whereas the one for long-channel devices is primarily governed by the bulk mobility. The ballistic mobility is given by [16].

$$\mu_{\text{ballistic}} = \frac{2qL}{\pi m_n^* V_{th}}$$

In order to extract the effective mobility for short-channel $In_{0.7}Ga_{0.3}As$ QWFETs, the experimental transfer characteristics are obtained [17].

4 Results And Discussion

For the simulation, the dimensions of the device have been considered identical to those reported in [17]. The composite channel consists of 3/8/4 nm thick $In_{0.53}Ga_{0.47}As/In_{0.7}Ga_{0.3}As/In_{0.53}Ga_{0.47}As$ and features both regular and buried-Pt gate stack with L_G = 20 nm in direct contact with the upper $In_{0.52}Al_{0.48}As$ barrier forming a Schottky junction. The devices have total channel thickness of 15 nm, the lateral spacer thickness of 80 nm and a source to drain electrode spacing of 2 μm. The regular Pt Schottky gate device has an effective insulator thickness of 11 nm.

Considering few device approximations as mentioned in [14], mobility of QWFET has been simulated with respect to a varying channel length up to 20 nm. Investigations have been made for a total of five different channel materials such as InAs, InGaAs, InSb, InP and GaAs. The result from the simulation has been illustrated in Fig. 4.

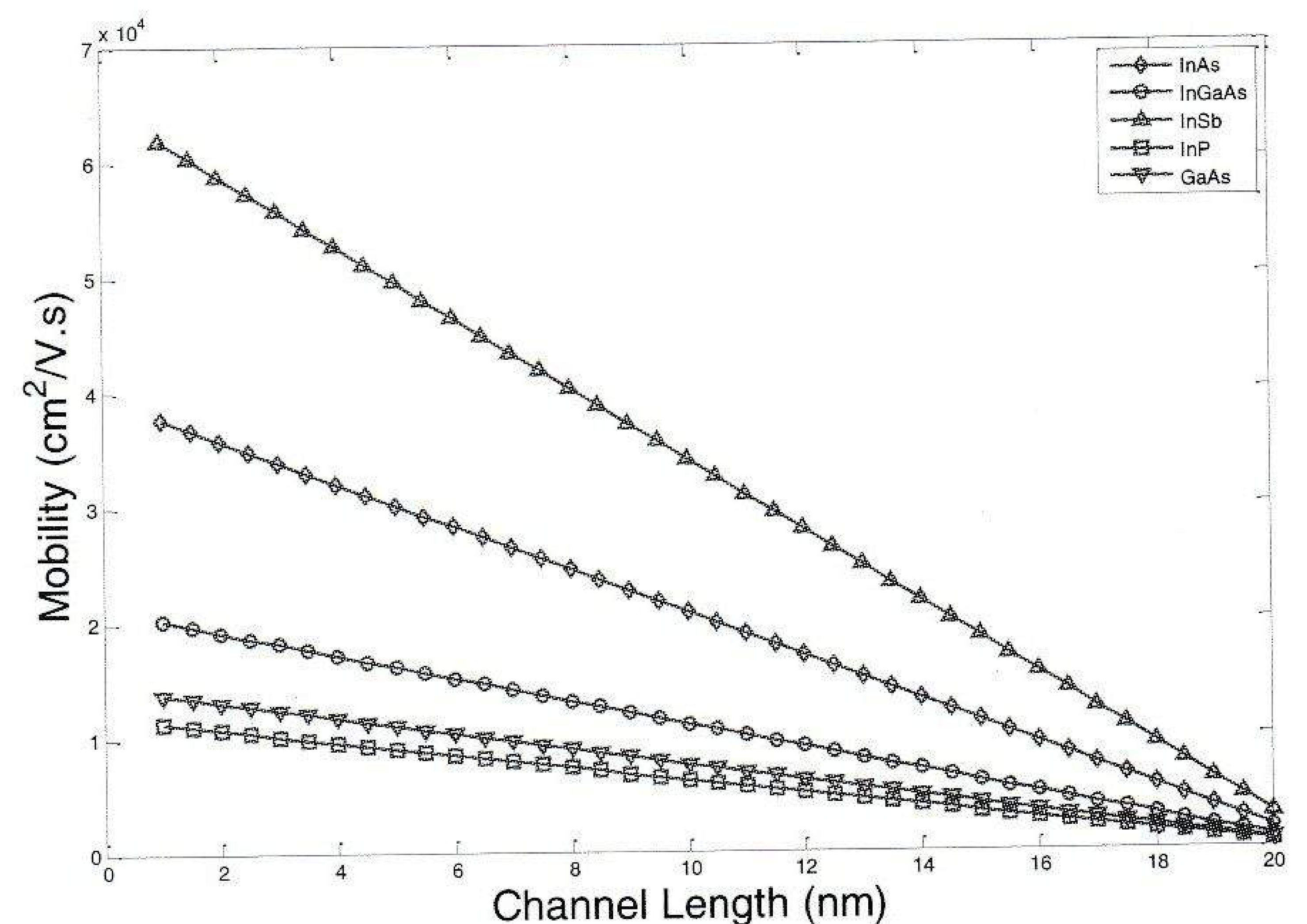

Fig. 4 Channel length dependency of mobility.

Fig. 4 depicts that the maximum mobility can be achieved from the minimum channel length. As larger channel lengths come into the picture, the mobility starts to drop linearly. The simulation result shows that for In As, the maximum and minimum mobilities are 3.77×10^4 cm^2/V.s and 0.19×10^4 cm^2/V.s. For InGaAs, these values are in

the range between 2.01×10^4 $cm^2/V.s$ and 0.1×10^4 $cm^2/V.s$. If the channel material is InSb, the mobility is 6.19×10^4 $cm^2/V.s$ for a gate length of 1 nm and 0.31×10^4 $cm^2/V.s$ for a gate length of 20 nm. For InP, these values are 1.13×10^4 $cm^2/V.s$ and 0.06×10^4 $cm^2/V.s$, respectively. And the mobility of GaAs lies in the range from 1.37×10^4 $cm^2/V.s$ to 0.07×10^4 $cm^2/V.s$. So, it can be seen evidently that the mobility is increased if the channel length of the QWFET is reduced.

Fig. 4 also portrays different values of mobilities for different channel materials. For example, InSb can achieve the highest mobility of 6.19×10^4 $cm^2/V.s$ in a QWFET with a channel length of 1 nm. Whereas InP has the lowest mobility, 1.13×10^4 $cm^2/V.s$, for the same channel length. For this particular length, the mobilities for InAs, InGaAs and GaAs are 3.77×10^4 $cm^2/V.s$, 2.01×10^4 $cm^2/V.s$ and 1.37×10^4 $cm^2/V.s$, respectively. These results illustrates that the mobility for a material depends vastly on the effective mass of its electrons. The lesser the effective mass, the higher the mobility, and vice versa.

5 Conclusion

The purpose of this research was to comprehend the physics of nanodevices like QWFETs. Mobility is a vibrant physical property of the material that the channel of the device is consisted of. The study was basically done for exploring the ballistic mobility for different channel lengths as well as the impact of using different materials on this mobility.

Carrier mobility has a great impact on transistor drive current [18]. And transistor drive current is the key to the characteristic of any device. Thus quantified evaluation of mobility is one of the fundamental information that was needed to be explored. The result of this research will help to discover many more other properties of quantum transistors in the future as well as to find out the opportunities of this device for future applications.

References

[1] R. R. Schaller, "MOOR's Law: Past, Present and Future," *IEEE Spectrum*, pp. 53-59, June 1997.

[2] L. Gippert, "Quantum Transistors: Towards Nanoelectronics," *IEEE Spectrum*, pp. 46-51, September 2000.

[3] S. Park, Y. Kim, H. Kim, H. Im and H. Kim N. Kim, "Characteristics of Ballistic Tansport in Short-Channel MOSFETs," *Journal of the Korean Physical Society*, vol. 45, pp. S928-S932, December 2004.

[4] Mejia, J. Hovarth, H. N. Alshareef, D. K. Cha, R. Ramirez-Bon, B. E. Gnade, and M. A. Quevedo-Lopez A. L. Salas-Villasenor, "Impact of Gate Dielectric in Carrier Mobility in Low Temperature Chalcogenide Thin Film Transistors for Flexible Electronics," *Electrochemical and Solid-State Letters*, vol. 13, no. 9, pp. H313-H316, 2010.

[5] M. Fox and R. Ispasoiu, "Quantum Well, Superlattices and Bandgap Engineering," in *Handbook of Electronic and Photonic Materials*.: Springer, 2007, pp. 1021-1040.

[6] D. H. Kim and J. A. Alamo, "Lateral and vertical scaling of In0.7Ga0.3As HEMTs for Post-Si-CMOS logic applications," *IEEE Transactions on Electron Devices*, vol. 55, no. 10, pp. 2546-2553, 2008.

[7] D. Kim and J. D. Alamo, "30-nm InAs pseudomorphic HEMTs on an InP substrate with a current-gain cutoff frequency of 628 GHz," *IEEE Electron Device Letters*, vol. 29, no. 8, pp. 830-833, 2008.

[8] G. Klimeck, D. H. Kim, J. D. Alamo and M. Luisier N. Kharche, "Multiscale Metrology and Optimization of Ultra-Scaled InAs Quantum Well FETs," *Purdue University Press Journal*, March 2011.

[9] L. Xia, B. R. Bennett, J. B. Boos, M. G. Ancona and J. D. Alamo L. W. Guo, "Enhancing p-channel InGaSb QW-FETs via Process-Induced Compressive Uniaxial Strain," *IEEE Electron Device Letters*, vol. 35, no. 11, pp. 1088-1090, November 2014.

[10] J. Wang and M. Lundstrom, "Ballistic Transport in High Electron Mobility Transistors," *IEEE Transactions on Electron Devices*, vol. 50, no. 7, pp. 1604-1609, July 2003.

[11] M. L. P. Tan, I. H. Hii, R. Ismail and V. K. Arora I. Saad, "Ballistic Mobility and Saturation Velocity in Low-Dimensional Nanostructures," *Elsevier Microelectronics Journal*, vol. 40, no. 3, pp. 540-542, March 2009.

[12] S. L. Teitel and J. W. Wilkins, "Ballistic Transport and Velocity Overshoot in Semiconductor: Part I - Uniform Field Effects," *IEEE Transactions on Electron Devices*, vol. ED-30, no. 2, February 1983.

[13] G. Majni, R. Minder and G. Ottaviani C. Canali, "Electron and Hole Drift Velocity Measurements in Silicon and Their Empirical Relation to Electric Field and Temperature," *IEEE Transactions on Electron Devices*, vol. 22, no. 11, pp. 1045-1047, November 1975.

[14] J. D. Bude, "MOSFET Modeling into the Ballistic Regime," in *In: Proceedings SISPAD*, 2000, pp. 23-26.

[15] S. Mookerjee, M. K. Hudait and S. Datta E. Hawang, "Investigation of Scalability of In0.7Ga0.3As Quantum Well Field Effect Transistor (QWFET) Architecture for Logic Applications," *Elsevier Journal: Solid-State Electronics*, pp. 82-89, May 2011.

[16] M. S. Shur, "Low Ballistic Mobility in Submicron HEMTs," *IEEE Electron Device Letter*, vol. 23, no. 9, pp. 511-513, September 2002.

[17] J. A. Alamo, J. H. Lee and K. S. Seo D. H. Kim, "Logic Suitability of 50-nm In0.7Ga0.3As HEMTs for Beyond-CMOS Applications," *IEEE Transactions of Electron Devices*, vol. 54, no. 10, pp. 2606-2613, October 2007.

[18] S. Datta, *Lessons from Nanoelectronics: A New Perspective on Transport*.: World Scientific Publishing Company, 2012.

[19] J. Wang and M. Lundstrom, "Ballistic transport in high electron mobility transistors," *IEEE Transactions on Electron Devices*, vol. 50, no. 7, pp. 1604-1609, Jly 2003.