Handbook of Photovoltaic Science and Engineering

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Other Wiley Editorial Offices

John Wiley & Sons Inc., 111 River Street, Hoboken, NJ 07030, USA

Jossey-Bass, 989 Market Street, San Francisco, CA 94103-1741, USA

Wiley-VCH Verlag GmbH, Boschstr. 12, D-69469 Weinheim, Germany

John Wiley & Sons Australia Ltd, 33 Park Road, Milton, Queensland 4064, Australia

John Wiley & Sons (Asia) Pte Ltd, 2 Clementi Loop #02-01, Jin Xing Distripark, Singapore 129809

John Wiley & Sons Canada Ltd, 22 Worcester Road, Etobicoke, Ontario, Canada M9W 1L1

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Library of Congress Cataloging-in-Publication Data

Handbook of photovoltaic science and engineering / edited by Antonio Luque and Steven Hegedus.
p. cm.
Includes bibliographical references and index.
ISBN 0-471-49196-9 (alk. paper)
1. Photovoltaic cells. 2. Photovoltaic power generation. I. Luque, A. (Antonio) II. Hegedus, Steven.

TK8322 .H33 2003
621.31′244 – dc21

2002191033

British Library Cataloguing in Publication Data

A catalogue record for this book is available from the British Library

ISBN 0-471-49196-9

Typeset in 10/12 Times by Laserwords Private Limited, Chennai, India
Printed and bound in Great Britain by Antony Rowe Ltd, Chippenham, Wiltshire
This book is printed on acid-free paper responsibly manufactured from sustainable forestry in which at least two trees are planted for each one used for paper production.

We dedicate this book to all those who have worked so hard for half a century to bring solar electricity to where it is today, and to our colleagues present and future who must work even harder in the next half century to make sure that it fulfills its potential as a widely available clean energy source.

The editors also owe much appreciation to the authors of the chapters contained in this book. Their long hours spent writing the best possible chapter covering their field of expertise, and then suffering through a storm of editorial criticisms, has hopefully made this a high-quality publication of lasting value.

Finally, we want to express our gratitude to our loved ones (Carmen, Ignacio, Sofía, Victoria, Inés, and Debbie, Jordan, Ariel) for the many hours stolen from family life while working on this book.

AL & SH
December 2, 2002

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1

Status, Trends, Challenges and the Bright Future of Solar Electricity from Photovoltaics

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1.1 THE BIG PICTURE

Congratulations! You are reading a book about a technology that has changed the way we think about energy. Solar electricity, also known as photovoltaics (PV), has shown since the 1970s that the human race can get a substantial portion of its electrical power without burning fossil fuels (coal, oil or natural gas) or creating nuclear fission reactions. Photovoltaics helps us avoid most of the threats associated with our present techniques of electricity production and also has many other benefits. Photovoltaics has shown that it can generate electricity for the human race for a wide range of applications, scales, climates, and geographic locations. Photovoltaics can bring electricity to a rural homemaker who lives 100 kilometers and 100 years away from the nearest electric grid connection in her country, thus allowing her family to have clean, electric lights instead of kerosene lamps, to listen to a radio, and to run a sewing machine for additional income. Or, photovoltaics can provide electricity to remote transmitter stations in the mountains allowing better communication without building a road to deliver diesel fuel for its generator. It can help a major electric utility in Los Angeles, Tokyo, or Madrid to meet its peak load on hot summer afternoons when air conditioners are working full time. It allows homes and businesses a new level of guaranteed energy availability and security, and photovoltaics has been powering satellites orbiting the Earth or flying to Mars for over 30 years.

Photovoltaics is an empowering technology that allows us to do totally new things, as well as, do old things better. It allows us to look at whole new modes of supplying

Handbook of Photovoltaic Science and Engineering. Edited by A. Luque and S. Hegedus
 ISBN: 0-471-49196-9

electricity to different markets around the world and out of the world (in outer space). It also allows us to do what we already do (generate electricity, which is distributed over the transmission grid) but to do it in a sustainable, pollution-free, equitable fashion. Why is photovoltaics equitable? Because nearly every one has access to sunlight!

Electricity is the most versatile form of energy we have. It is what allows citizens of the developed countries to have nearly universal lighting on demand, refrigeration, hygiene, interior climate control in their homes, businesses and schools, and widespread access to various electronic and electromagnetic media. Access to and consumption of electricity is closely correlated with quality of life. Figure 1.1 shows the Human Development Index (HDI) for over 60 countries, which includes over 90% of the Earth's population, versus the annual per capita electricity use (adapted from ref 1). The HDI is compiled by the UN and calculated on the basis of life expectancy, educational achievement, and per capita Gross Domestic Product. To improve the quality of life in many countries, as measured by their HDI, will require increasing their electricity consumption by factors of 10 or more, from a few hundred to a few thousand kilowatt-hrs (kWh) per year. How will we do it? Our choices are to continue applying the answers of the last century such as burning more fossil fuels (and releasing megatons of CO_2, SO_2, and NO_2) or building more nuclear plants (despite having no method of safely disposing of the high-level radioactive waste) or to apply the new millennium's answer of renewable, sustainable, nonpolluting, widely available clean energy like photovoltaics and wind. (Wind presently generates over a thousand times more electricity than photovoltaics but it is very site-specific, whereas photovoltaics is generally applicable to most locations.)

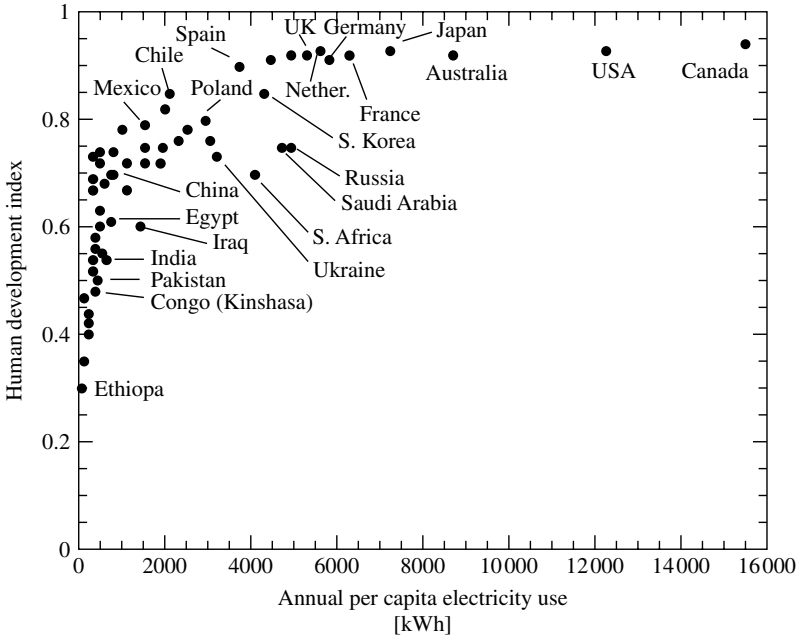

Figure 1.1 Human development index (HDI) vs. per capita kW usage [1]

1.2 WHAT IS PHOTOVOLTAICS?

Photovoltaics is the technology that generates direct current (DC) electrical power measured in Watts (W) or kiloWatts (kW) from semiconductors when they are illuminated by photons. As long as light is shining on the solar cell (the name for the individual PV element), it generates electrical power. When the light stops, the electricity stops. Solar cells never need recharging like a battery. Some have been in continuous outdoor operation on Earth or in space for over 30 years.

Table 1.1 lists some of the advantages and disadvantages of photovoltaics. Note, that they include both technical and nontechnical issues. Often, the advantages and disadvantages of photovoltaics are almost completely opposite of conventional fossil-fuel power plants. For example, fossil-fuel plants have disadvantages of: a wide range of environmentally hazardous emissions, parts which wear out, steadily increasing fuel costs, they are not modular (deployable in small increments), and they suffer low public opinion (no one wants a coal burning power plant in their neighborhood). Photovoltaics suffers none of these problems. The two common traits are that both PV and fossil fueled power plants are very reliable but lack the advantage of storage.

Notice that several of the disadvantages are nontechnical but relate to economics and infrastructure. They are partially compensated for by a very high public acceptance and awareness of the environmental benefits. During the late 1990s, the average growth rate of PV production was over 33% per annum.

What is the physical basis of PV operation? Solar cells are made of materials called semiconductors, which have weakly bonded electrons occupying a band of energy

Table 1.1 Advantages and disadvantages of photovoltaics

Advantages of photovoltaics	Disadvantages of photovoltaics
Fuel source is vast and essentially infinite	Fuel source is diffuse (sunlight is a relatively low-density energy)
No emissions, no combustion or radioactive fuel for disposal (does not contribute perceptibly to global climate change or pollution)	
Low operating costs (no fuel)	High installation costs
No moving parts (no wear)	
Ambient temperature operation (no high temperature corrosion or safety issues)	
High reliability in modules (>20 years)	Poorer reliability of auxiliary (balance of system) elements including storage
Modular (small or large increments)	
Quick installation	
Can be integrated into new or existing building structures	
Can be installed at nearly any point-of-use	Lack of widespread commercially available system integration and installation so far
Daily output peak may match local demand	Lack of economical efficient energy storage
High public acceptance	
Excellent safety record	

called the *valence band*. When energy exceeding a certain threshold, called the *band gap energy*, is applied to a valence electron, the bonds are broken and the electron is somewhat "free" to move around in a new energy band called the *conduction band* where it can "conduct" electricity through the material. Thus, the free electrons in the conduction band are separated from the valence band by the band gap (measured in units of electron volts or eV). This energy needed to free the electron can be supplied by photons, which are particles of light. Figure 1.2 shows the idealized relation between energy (vertical axis) and the spatial boundaries (horizontal axis). When the solar cell is exposed to sunlight, photons hit valence electrons, breaking the bonds and pumping them to the conduction band. There, a specially made selective contact that collects conduction-band electrons drives such electrons to the external circuit. The electrons lose their energy by doing work in the external circuit such as pumping water, spinning a fan, powering a sewing machine motor, a light bulb, or a computer. They are restored to the solar cell by the return loop of the circuit via a second selective contact, which returns them to the valence band with the same energy that they started with. The movement of these electrons in the external circuit and contacts is called the *electric current*. The potential at which the electrons are delivered to the external world is slightly less than the threshold energy that excited the electrons; that is, the band gap. Thus, in a material with a 1 eV band gap, electrons excited by a 2 eV photon or by a 3 eV photon will both still have a potential of slightly less than 1 V (i.e. the electrons are delivered with an energy of 1 eV). The electric power produced is the product of the current times the voltage; that is, power is the number of free electrons times their potential. Chapter 3 delves into the physics of solar cells in much greater detail.

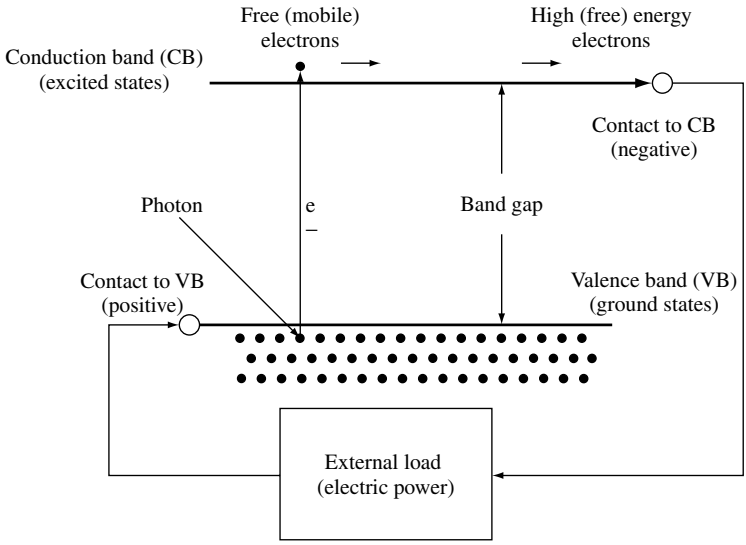

Figure 1.2 Schematic of a solar cell. Electrons are pumped by photons from the valence band to the conduction band. There they are extracted by a contact selective to the conduction band (an *n*-doped semiconductor) at a higher (free) energy and delivered to the outside world via wires, where they do some useful work, then are returned to the valence band at a lower (free) energy by a contact selective to the valence band (a *p*-type semiconductor)

Sunlight is a spectrum of photons distributed over a range of energy. Photons whose energy is greater than the band gap energy (the threshold energy) can excite electrons from the valence to conduction band where they can exit the device and generate electrical power. Photons with energy less than the energy gap fail to excite free electrons. Instead, that energy travels through the solar cell and is absorbed at the rear as heat. Solar cells in direct sunlight can be somewhat (20–30°C) warmer than the ambient air temperature. Thus, PV cells can produce electricity without operating at high temperature and without mobile parts. These are the salient characteristics of photovoltaics that explain safe, simple, and reliable operation.

At the heart of any solar cell is the *pn* junction. Modeling and understanding is very much simplified by using the *pn* junction concept. This *pn* junction results from the "doping" that produces conduction-band or valence-band selective contacts with one becoming the *n*-side (lots of negative charge), the other the *p*-side (lots of positive charge). The role of the *pn* junction and of the selective contacts will be explained in detail in Chapters 3 and 4. Here, *pn* junctions are mentioned because this term is often present when talking of solar cells, and is used occasionally in this chapter.

Silicon (Si), one of the most abundant materials in the Earth's crust, is the semiconductor used in crystalline form (c-Si) for 90% of the PV applications today (Chapter 5). Surprisingly, other semiconductors are better suited to absorb the solar energy spectrum. This puzzle will be explained further in Section 1.10. These other materials are in development or initial commercialization today. Some are called thin-film semiconductors, of which amorphous silicon (a-Si) (Chapter 12), copper indium gallium diselenide ($Cu(InGa)Se_2$ or CIGS) (Chapter 13), and cadmium telluride (CdTe) (Chapter 14) receive most of the attention. Solar cells may operate under concentrated sunlight (Chapter 11) using lenses or mirrors as concentrators allowing a small solar cell area to be illuminated with the light from larger area. This saves the expensive semiconductor but adds complexity to the system, since it requires tracking mechanisms to keep the light focused on the solar cells when the sun moves in the sky. Silicon and III-V semiconductors (Chapter 9), made from compounds such as gallium arsenide (GaAs) and gallium indium phosphide (GaInP) are the materials used in concentrator technology that is still in its demonstration stage.

For practical applications, a large number of solar cells are interconnected and encapsulated into units called PV modules, which is the product usually sold to the customer. They produce DC current that is typically transformed into the more useful AC current by an electronic device called *an inverter*. The inverter, the rechargeable batteries (when storage is needed), the mechanical structure to mount and aim (when aiming is necessary) the modules, and any other elements necessary to build a PV system are called the *balance of the system* (BOS). These BOS elements are presented in Chapters 17 to 19.

1.3 SIX MYTHS OF PHOTOVOLTAICS

Borrowing a format for discussing photovoltaics from Kazmerski [2], in this section, we will briefly present and then dispel six common myths about photovoltaics. In the following sections, we identify serious challenges that remain despite 40 years of progress in photovoltaics.

The six myths are as follows:

1. *Photovoltaics will require too much land area to ever meet significant fraction of world needs*:

Solar radiation is a rather diffuse energy source. What area of PV modules is needed to produce some useful amounts of power? Let's make some very rough estimates to give answers that will be accurate within a factor of 2. Using methods described in detail in Chapter 20 (especially equations 20.50 and 20.51 and Table 20.5), one can calculate how much sunlight falls on a square meter, anywhere in the world, over an average day or a year. We will use an average value of 4 kilowatt-hrs (kWh) per m^2 per day to represent a conservative worldwide average. Now, a typical PV module is approximately 10% efficient in converting the sunlight into electricity, so every square meter of PV module produces, on average, $4 \times 0.1 = 0.4$ kWh of electrical energy per day. We can calculate the area in m^2 needed for a given amount of electrical energy E in kWh by dividing E by 0.4 kWh/m^2. (Chapter 20 contains much more detailed methods to calculate the incident sunlight and the PV module output as a function of time of day, month of year, etc.)

Let us consider three different-sized PV applications: a family's house in an industrialized country, replacing a 1000 MW (megawatt) coal or nuclear powered generating plant, or providing all the electricity used in the USA.

First, for a typical family, let us assume that there are four people in the house. Figure 1.1 shows a range of electricity usage for the industrialized countries. Let us use 6000 kWh/person/year as an average. But, this includes all their electrical needs including at work, at school, as well as the electricity needed for manufacturing the products they buy, powering their street lights, pumping water to their homes, and so on. Since people spend about a third of the day awake in their home, let us assume that a third of their electrical needs are to be supplied in their home, or 2000 kWh/person/year. Dividing this by 365 days in a year gives about 5 kWh/person/day, or 20 kWh/day per family of four. This is consistent with household data from various sources for the US and Europe. Thus, they would need 20 kWh/0.4 kWh/m^2 or 50 m^2 of solar modules to provide their electrical power needs over the year. Thus, a rectangular area of solar modules of 5 by 10 meters will be sufficient. In fact, many roofs are about this size, and many homes have sunny areas of this size around them, so it is possible for a family of four, with all the conveniences of a typical modern home, to provide all their power from PV modules on their house or in their yard.

Next, how much land would it take to replace a 1000 MW coal or nuclear power plant that operates 24 hours/day and might power a large city? This would require 10^6 kW $\times$ 24 hr/(0.4 kWh/m^2) or 6×10^7 m^2. So, with 60 km^2 (or 24 square miles) of photovoltaics we could replace one of last century's power plants with one of this century's power plants. This is a square 8 km (or 5 miles) on a side. For the same electricity production, this is equivalent to the area for coal mining during the coal powered plant's life cycle, if it is surface mining, or three times the area for a nuclear plant, counting the uranium mining area [3]. This is also the same area required to build a 600 km (373 miles) long highway (using a 100 m wide strip of land).

Finally, we can calculate how much land is needed to power the entire US with photovoltaics (neglecting the storage issue). The US used about 3.6×10^{12} kWh of electricity in 2000. This could be met with 2×10^{10} m^2. If we compare with the area of paved roads across the country, of about 3.6×10^6 km and assume an average width

of 10 m this leads to 3.6×10^{10} m^2. It is to be concluded that all the electricity needed in the US can be met by covering the paved roads with PV modules. Of course, no one is seriously proposing this action. We use the road analogy to show that if society wanted, it could establish land use priorities favorable to photovoltaics just as it has done to accommodate the ubiquitous automobile. We are certain that each state could find areas of unused land around airports, parking spaces, rooftops, highway dividing strips, or desert land that could be used for photovoltaics.

These simplistic "back-of-the-envelope" calculations show that having enough area for PV modules is not a limit for a homeowner or a large city. Certainly, there are sunny places in every country that could be used for generating significant amounts of PV power. As will be evident in other chapters, it is the initial cost of the photovoltaics, not the amount of land that is the primary barrier to be overcome.

2. *Photovoltaics can meet all of the world's needs today if we would just pass laws requiring photovoltaics and halting all fossil and nuclear plants*:

Besides the difficulty of convincing the people's representatives to pass such a law, the first technical problem faced would be the intermittent nature of the solar radiation, available only during the day and strongly reduced in overcast skies. Energy storage would solve this problem but no cheap storage method appears on the horizon. Nevertheless, well-developed electric grids may accept large amounts of PV electricity by turning off some conventional power plants when PV plants are delivering power. Adequate grid management would allow up to 20 to 30% of the electric production to be intermittent [4].

But now for a dose of reality. The cumulative production of PV modules up to the year 2002 is about 2000 MW. Thus, if you took all of the PV panels that were ever made up to and including the year 2002, and put them all in the same sunny place at the same time, they would generate enough electricity to displace about one of last century's 500 MW smoke- or radioactive-waste–producing power plants. (This assumes that the solar plant would operate at full output for an equivalent of six hours per day owing to the daily variation in sunlight). Clearly, if we want photovoltaics to make any meaningful contribution to the world's energy supply, very massive increases in manufacturing capacity are needed. Additionally, PV electricity is very expensive, presently between 5 to 10 times more expensive than conventional alternatives. Mass use of PV electricity today could produce significant negative distortion of the economic system.

Thus, requesting the immediate and exclusive use of photovoltaics is not feasible technically or, probably, economically. It would also be socially unacceptable.

3. *Photovoltaics cannot meet any significant fraction of world needs. It will remain a small-scale "cottage" industry that will only meet the needs of specialty markets like remote homes in developing countries or space satellites*:

Figure 1.3 shows the evolution of markets associated with different applications [5]. Some used to be considered as *specialty* markets, for example, the category of "world off-grid power" which is trying to supply power to the ~1/3 of the world's citizens who lack it. The grid-connected market, whose growth has been meteoric in the past decade, is by no means a small market. Ironically it is the large-scale (recently awakened) centralized power plant market which is the smallest "specialty" application in today's world. Thus, evidence from the recent past tends to refute

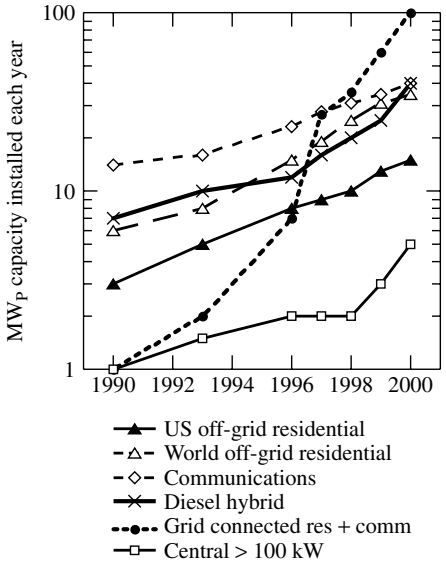

Figure 1.3 Trend in worldwide PV applications (From Reference [5] Maycock P, *Renewable Energy World* **3**, 59–74 (2000)

the modest forecasts that some attribute to photovoltaics. We shall come to this point again.

4. *No more R/D is needed since PV technology has demonstrated the technical capability to perform, so we should stop all public funding and let the economic markets decide if it is worthwhile*:

The present cost of photovoltaics is affordable for certain markets but it is still too high to actually compete with conventional electricity. If PV technology is to be promoted for environmental or social reasons, public subsidy to R&D and to installation will be necessary to stimulate production and thereby reduce costs. Without continued subsidies, photovoltaics will probably remain as a specialty cottage industry for the next half century.

Public support for photovoltaics is one of the major factors compelling politicians to fund R&D. This funding had been comparable to PV sales in the 1980s, as shown in Figure 1.4. Private funding has doubled this public support so that PV companies themselves have also heavily supported the development of photovoltaics. After two decades of constant investment in a promising market that was slow to actually start, the market finally awoke and became one of the fastest growing in the world by the beginning of the twentieth century, with sales now greatly exceeding public investment.

But, this fast growing market is still dependent on public/government funding. As with many goods and services (e.g. military hardware, commercial air travel), photovoltaics is partly publicly financed. In Germany or in Japan, for instance, significant public support is being given to grid-connected installations. If photovoltaics is going to become a major energy contender, the countries where the support has been lacking will remain technologically inferior with respect to those, where the support has

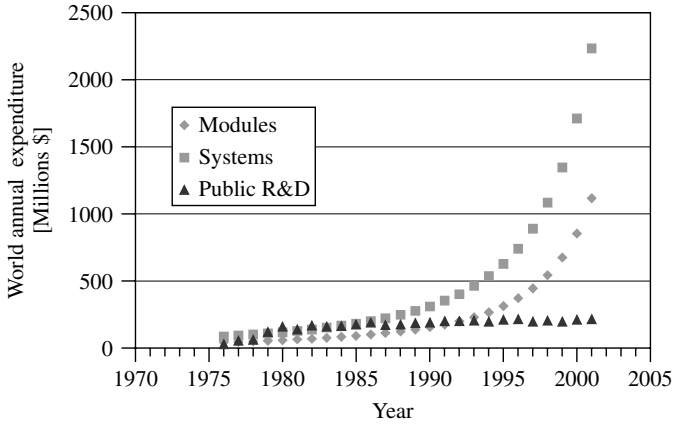

Figure 1.4 Public funding for R&D (triangles) compared to module (diamonds) and system (squares) sales. (This curve is drawn from the data of Eckhart *et al*. in Chapter 24, "Financing PV Growth", in this book)

been stronger. This should be taken into account while making decisions about energy policy and public or private financing.

The critical question then is: Should the support be focused in R&D, or is PV technology already mature enough (as many claim) to focus on the cost reduction via the economy of scale permitted by the larger volume of production required by a subsidized market? This point will be discussed latter in this chapter.

5. *Photovoltaics is polluting just like all high-technology or high-energy industries only with different toxic emissions*:

   One of the most valuable characteristics of photovoltaics is its well-deserved image as an environmentally clean and "green" technology. This healthy image obviously results from the cleaner operation of a PV electricity generator compared to a fossil-fuel fired generator, but this must also extend to the manufacturing process itself as well as the recycling of discarded modules. Manufacturing of PV modules on a large scale requires the handling of large quantities of hazardous or potentially hazardous materials (e.g. heavy metals, reactive chemical solutions, toxic gases). Let it be stated at the beginning that the present Si-based PV technology which dominates the market has few environmental concerns and is considered totally safe to the public.

   The PV industry is very aware of the value of its clean "green" image and has worked hard over the years to establish and maintain high standards of environmental responsibility [6, 7]. Conferences on PV Safety and Environmental Issues have been held since the late 1980s and their proceedings have been published [8, 9]; the PV Environmental Health Safety Assistance Center at Brookhaven National Laboratory in New York, USA provides worldwide leadership in risk analysis and safety recommendations for the PV industry [10].

   Safe handling procedures for some of the materials and processes were already well established from the integrated circuit or glass coating industries. But in the case of unique materials and processes, safety procedures had to be developed by the PV industry. This is especially true of the thin-film technologies [11]. The PV industry recognized early that being proactive and designing safety into the process, from the

beginning, was the responsible thing to do and would ultimately result in reduced costs. The international nature of the PV industry introduces some variability in the standards which must be met.

Hazards can be classified by whether they affect workers at a PV manufacturing plant, customers with photovoltaics on or near their homes, or the public who consumes air and water near the PV plant. The population with greatest potential health risks are employees in PV manufacturing. Very little risk is associated with the public or the PV owner or installer. Among the most heavily studied issues unique to the PV industry is the potential toxicity of semiconductor CdTe and the safe usage of hydride gases AsH_3, SiH_4, GeH_4, PH_3, B_2H_6, and H_2Se, which are used in the growth of GaAs, a-Si, a-SiGe, and $Cu(InGa)Se_2$ layers. There has been considerable research and risk analysis of CdTe as a PV material [12–14]. The general conclusion is that CdTe in modules does not pose a risk to the public. Similarly, procedures and hardware ensuring safe usage of the hydride gases listed above have been well established in both the electronics and PV industries [15].

Environmental monitoring of the workplace for hazardous levels in the air or on surfaces, and biological monitoring of the employee for evidence of exposure should be routine. Once the module is manufactured, the only way for the public to be exposed to hazardous materials existing in some kind of modules is by absorbing them via ingestion or inhalation. Accordingly, accidental human absorption is not at all likely. Even in event of a house fire, studies have shown that PV modules do not release any potentially hazardous materials [16].

A related issue is what to do with thin film PV modules at the end of their projected 25- to 30-year life. An excellent strategy is to recycle the modules. This solves two problems at once, namely, keeping potentially hazardous materials out of the environment and reducing the need for additional mining and/or refining of new materials. Semiconductor vendors have indicated a willingness to accept used modules, and to extract and purify the CdTe, CdS, or $Cu(InGa)Se_2$ for resale and reuse [17, 18].

Thus, we can say with confidence that photovoltaics is nearly the cleanest and safest technology with which to generate electricity. It is especially true of the present Si technology.

6. *PV modules never recover all of the energy required in making them, thus they represent a net energy loss*:

The focus of photovoltaics is on generating energy (specifically electrical energy) with many beneficial characteristics as noted in Table 1.1. Among those who envision photovoltaics having an increasingly larger role in producing the world's electricity, there is awareness that photovoltaics must produce much more energy than was required to produce the PV system. Otherwise, it would be a net energy loss not a net energy source. The "energy payback" has been widely studied. It is described in terms of how many years the PV system must operate to produce the energy required for its manufacture. After the payback time, all of the energy produced is truly new energy.

This topic is discussed in Chapter 21. An excellent review has been given by Alsema [19]. In general, results of several studies have arrived at some general conclusions. Specific payback times have ranged from 3 to 5 years for crystalline Si and 1 to 4 years for thin films. For crystalline Si, forming the crystalline Si wafers is

the major energy requirement. For thin films, the semiconductor layers are 100 times thinner, and deposited at ~1000°C lower temperature, so their energy requirement is negligible, in comparison. Instead, it is the energy embodied in the glass or stainless steel substrate, which is the major energy sink. Also, a seemingly insignificant component, the cosmetic Al frame around the module, is responsible for a surprisingly large fraction of energy. In fact, this can be the dominant energy sink for thin-film a-Si or $Cu(InGa)Se_2$ modules [20, 21]. Although thin-film modules have a shorter energy payback, they also have lower efficiency, which means a larger BOS is needed to support the larger number of modules. Thus, a larger amount of energy is embodied in the BOS for thin-film photovoltaics compared to crystalline Si photovoltaics.

The case of concentrators is less studied, but again the use of semiconductor is reduced and the BOS becomes more important than even for the thin films because the concentrating structures are very massive. However, their efficiency is higher. In summary, we can guess that in this case the situation will be similar to the case of thin films.

1.4 HISTORY OF PHOTOVOLTAICS

The history of photovoltaics goes back to the nineteenth century, as shown in Table 1.2. The first functional, intentionally made PV device was by Fritts [22] in 1883. He melted Se into a thin sheet on a metal substrate and pressed a Au-leaf film as the top contact. It was nearly 30 cm^2 in area. He noted, "the current, if not wanted immediately, can be either stored where produced, in storage batteries, ... or transmitted a distance and there used." This man foresaw today's PV technology and applications over a hundred years ago. The modern era of photovoltaics started in 1954 when researchers at Bell Labs in the USA accidentally discovered that *pn* junction diodes generated a voltage when the room lights were on. Within a year, they had produced a 6% efficient Si *pn* junction solar cell [23]. In the same year, the group at Wright Patterson Air Force Base in the US published results of a thin-film heterojunction solar cell based on Cu_2S/CdS also having 6% efficiency [24]. A year later, a 6% GaAs *pn* junction solar cell was reported by RCA Lab in the US [25]. By 1960, several key papers by Prince [26], Loferski [27], Rappaport and Wysoski [28], Shockley (a Nobel laureate) and Queisser [29], developed the fundamentals of *pn* junction solar cell operation including the theoretical relation between band gap, incident spectrum, temperature, thermodynamics, and efficiency. Thin films of CdTe were also producing cells with 6% efficiency [30]. By this time, the US space program was utilizing Si PV cells for powering satellites. Since space was still the primary application for photovoltaics, studies of radiation effects and more radiation-tolerant devices were made using Li-doped Si [31]. In 1970, a group at the Ioffe Institute led by Alferov (a Nobel laureate), in the USSR, developed a heteroface GaAlAs/GaAs [32] solar cell which solved one of the main problems that affected GaAs devices and pointed the way to new device structures. GaAs cells were of interest due to their high efficiency and their resistance to the ionizing radiation in outer space. The year 1973 was pivotal for photovoltaics, in both technical and nontechnical areas. A significant improvement in performance occurring in 1973 was the "violet cell" having an improved short wavelength response leading to a 30% relative increase in efficiency over state-of-the-art Si cells [33]. GaAs heterostructure cells were also developed at IBM in

Table 1.2 Notable events in the history of photovoltaics

- 1839 Becquerel (FR) discovered photogalvanic effect in liquid electrolytes
- 1873 Smith (UK) discovered photoconductivity of solid Se
- 1877 Adams and Day (UK) discover photogeneration of current in Se tubes; the first observation of PV effect in solids
- 1883 Fritts (US) makes first large area solar cell using Se film
- 1954 First 6% efficient solar cells reported: Si (Bell Lab, USA) and Cu_2S/CdS (Air Force, USA)
- 1955 Hoffman Electronics (USA) offers 2% efficient Si PV cells at $1500/W
- 1958 NASA Vanguard satellite with Si backup solar array
- 1959 Hoffman Electronics (USA) offers 10% efficient Si PV cells
- 1963 Sharp Corp (JP) produces first commercial Si modules
- 1966 NASA Orbiting Astronomical Observatory launched with 1 kW array
- 1970 First GaAs heterostructure solar cells by Alferov, Andreev *et al.* in the USSR
- 1972 First PV conference to include a session on terrestrial applications (IEEE)
- 1973 A big year in photovoltaics: Worldwide oil crisis spurs many nations to consider renewable energy including photovoltaics; Cherry Hill Conference in USA (established photovoltaics' potential and legitimacy for government research funding); World's first solar powered residence (University of Delaware, USA) built with Cu_2S (not c-Si!) solar modules
- 1974 Project Sunshine initiated in Japan to foster growth of PV industry and applications; Tyco (USA) grows 2.5 cm wide Si ribbon for photovoltaics, first alternative to Si wafers
- 1975 First book dedicated to PV science and technology by Hovel (USA)
- 1980 First thin-film solar cell >10% using Cu_2S/CdS (USA)
- 1981 350 kW Concentrator array installed in Saudi Arabia
- 1982 First 1 MW utility scale PV power plant (CA, USA) with Arco Si modules on 2-axis trackers
- 1984 6 MW array installed in Carrisa Plains CA, USA [35]
- 1985 A big year for high-efficiency Si solar cells: Si solar cell >20% under standard sunlight (UNSW, Australia) [36] and >25% under 200X concentration (Stanford Univ. USA) [37]
- 1986 First commercial thin-film power module, the a-Si G4000 from Arco Solar (USA)
- 1987 Fourteen solar powered cars complete the 3200 km World Solar Challenge race (Australia) with the winner averaging 70 kph
- 1994 GaInP/GaAs 2-terminal concentrator multijunction >30% (NREL, USA) [38]
- 1995 "1000 roofs" German demonstration project to install photovoltaics on houses, which triggered the present favorable PV legislation in Germany, Japan and other countries
- 1996 Photoelectrochemical "dye-sensitized" solid/liquid cell achieves 11% (EPFL, Switzerland) [39]
- 1997 Worldwide PV production reaches 100 MW per year
- 1998 Cu(InGa)Se_2 thin-film solar cell reaches 19% efficiency (NREL, US) [40] comparable with multicrystalline Si. First concentrating array for space launched on Deep Space 1 by US (5 kW using high efficiency GaInP/GaAs/Ge triple junction cells)
- 1999 Cumulative worldwide installed photovoltaics reaches 1000 MW
- 2000 Olympics in Australia highlight wide range of PV applications, and the awarding of the first Bachelor of Engineering degrees in Photovoltaics and Solar Engineering (UNSW, Australia)
- 2002 Cumulative worldwide installed photovoltaics reaches 2000 MW. It took 25 years to reach the first 1000 MW and only 3 years to double it; production of crystalline Si cells exceeds 100 MW per year at Sharp Corp. (Japan). BP Solar ceases R&D and production of a-Si and CdTe thin-film modules in USA ending >20 years of effort

the USA having 13% efficiency [34]. Also in 1973, a crucial nontechnical event occurred called the *Cherry Hill Conference*, named after the town in New Jersey, USA, where a group of PV researchers and heads of US government scientific organizations met to evaluate the scientific merit and potential of photovoltaics. The outcome was the decision that photovoltaics was worthy of government support, resulting in the formation of the US Energy Research and Development Agency, the world's first government group whose mission included fostering research on renewable energy, which ultimately became the US Dept. of Energy. Finally, in October 1973, the first World Oil Embargo was instituted by the Persian Gulf oil producers. This sent shock waves through the industrialized world, and most governments began programs to encourage renewable energy especially solar energy. Some would say this ushered in the modern age of photovoltaics and gave a new sense of urgency to research and application of photovoltaics in terrestrial applications.

In the 1980s, the industry began to mature, as emphasis on manufacturing and costs grew. Manufacturing facilities for producing PV modules from Si wafer *pn* junction solar cells were built in the USA, Japan, and Europe. New technologies began to move out of the government, university and industrial laboratories, and into precommercialization or "pilot" line production. Companies attempted to scale up the thin-film PV technologies like a-Si and $CuInSe_2$, which had achieved $>10\%$ efficiency for small area (1 cm^2) devices made with carefully controlled laboratory scale equipment. Much to their disappointment, they found that this was far more complicated than merely scaling the size of the equipment. Most large US semiconductor companies, gave up their R/D efforts (IBM, General Electric, Motorola) lacking large infusions of private or government support to continue. One common result was the purchase of American companies and their technologies by foreign companies. In 1990, the world's largest solar manufacturer was Arco Solar (CA, USA), owned by oil company Atlantic Richfield, which had c-Si and thin-film a-Si in production and thin-film $CuInSe_2$ in precommercialization. They were sold to the German firm Siemens and renamed Siemens Solar (in 2001, the Dutch company Shell Solar would buy Siemens, becoming another large internationally based company with multiple PV technologies in production). Also in 1990, Energy Conversion Devices (MI, USA) formed a joint venture called United Solar Systems Corp. with the Japanese manufacturer Canon to commercialize ECD's roll-to-roll triple-junction a-Si technology. In 1994, Mobil Solar Energy (MA, USA), which had developed a process for growing solar cells on Si ribbon (called the Edge defined film growth or EFG process) instead of more costly wafers, was sold to the German company ASE and renamed ASE Americas. The British solar company BP Solar acquired patents to electrodeposition of thin-film CdTe solar cells in 1989, when it's parent company purchased the American oil giant Standard Oil of Ohio. At the same time, it acquired the patents of the University of New South Wales (Australia) to fabricate the Laser-Grooved Buried-Grid (LGBG) cells, which became the most efficient silicon cells in fabrication. In 1996, it signed a license agreement with the Polytechnic University of Madrid (Spain) to exploit the Euclides concentration technology that used their LGBG cells as concentrator cells. In 1999, BP Solar acquired Solarex from Enron (another huge fossil-fuel energy company) that had crystalline and amorphous Si solar cell technology. Thus, BP Solar established themselves with manufacturing interests in all three technology options (standard Si wafers, thin films

and concentrators).[1] Meanwhile, the Japanese PV industry began to take off. Production of c-Si modules and intensive research on thin-film technology in Japan led to many innovative device designs, improved materials processing, and growing dominance in the world PV market.

Along with the maturing of the solar cell technology, the BOS needed to grow. Many products like inverters, which convert the DC power into AC power, and sun trackers had only limited application outside of a PV power system, so once again there was only limited technical and financial resources for development. In many system evaluations, the inverter was repeatedly identified as the weak link in terms of reliability and AC power quality [41]. Their costs have not fallen nearly as fast as those for the PV modules. While much effort and resources had been focused on the solar cell cost and performance, little attention had been paid to installation and maintenance costs. It was quickly discovered that there was room for much improvement.

An early development that helped many companies was to sell PV cells for consumer-sized, small-scale power applications. The solar-powered calculator, pioneered by Japanese electronics companies as a replacement for battery-powered calculators in the early 1980s, is the best-known example. This led to the early use of thin-film a-Si PV cells for various applications. Another example was solar-powered outdoor lighting. These novel consumer applications, where portability and convenience were more valued than low price, allowed the PV companies to maintain some small income while continuing to develop power modules.

Another application was the rural electrification of remote villages in an attempt to help roughly one-third of the world's citizens to gain access to a modest amount of modern communication and lighting. Most of these PV installations were very small, on the order of 10 to 40 W per household (100 times smaller than the "needs" of a modern home in the developed world.) Most of these installations were funded by some international aid agency. Reviews and follow-up studies of these programs have indicated very large failure rates, primarily due to lack of technical infrastructure [42], training, cultural misunderstandings, design of the payment structure, and other nontechnical reasons [43]. Rarely have the PV modules failed. Even with subsidies from the international agencies, the high initial cost of ownership ($100–1000) was still a major barrier in much of the world where this represents a year's income for a family [44].

On the opposite end of the size scale were the MW-size PV plants installed by utilities in developed countries in the 1980s to evaluate their potential in two applications: as a peak-load-reduction technology, where the photovoltaics provides additional power primarily to meet the peak demand during the afternoon [45]; or as distributed generators, to reduce transmission and distribution losses [46]. Several American utilities investigated these applications, to assess the technical as well as financial benefits for photovoltaics in utility scale applications. Other novel configurations of grid-tied PV

[1] While this book was going to press in November 2002, BP Solar suddenly announced the closure of its two thin-film manufacturing efforts in the United States (a-Si in Virginia and CdTe in California) in order to focus more resources on its multicrystalline Si wafer PV production. This was a great disappointment to all those who worked so hard to establish these thin-film technologies and facilities, which were among the most advanced thin-film PV products in the world.

systems were evaluated as so-called "demand side management" options where the on-site distributed photovoltaics is used to reduce demand rather than increase supply [47]. Although American utilities lost interest in PV in the late 90s due to deregulation, grid-connected applications in Europe and Japan began to grow rapidly, primarily owing to strong government support. Both small- and large-scale grid connected PV installations are blossoming in these countries [48, 49].

Yet another important development in the application of PV in the late 1990s, was building integrated PV (BIPV [50]), where PV cells are incorporated into a standard building product, such as a window or a roof shingle, or into an architectural feature like an exterior sun awning or semitransparent skylight. In this way, the cost of the PV is partially offset by the cost of the building materials, which would have been required anyway, so the incremental cost of the photovoltaics is much lower. BIPV is discussed in Chapter 22. The success of grid-connected residential or BIPV commercial applications has been possible because several countries led by Germany have established high rates to pay for the PV electricity produced by solar installations in private houses. In this scheme, the installation owner receives \$0.5/kWh for the electricity they feed into the public electric grid (as of 2001). But the owner buys the electricity consumed in their own house at the normal cost of ~\$0.1/kWh from the grid. Additionally, German banks provided generous loans for purchasing the installation. Similar concepts are used in Spain, the Netherlands, and other countries in Europe. But, the success has been still bigger in Japan where homebuilders receive a rebate from the government for about 30% of the PV system cost. Then, their electric bill is determined by the utility using the "net metering" where the customer pays only the net difference between what they used and what they generated. Rebates and net metering are available in some, but not all, states in the USA as of 2002. Interestingly, government support of photovoltaics in Japan has been decreasing while the market for PV homes has continued showing an impressive growth rate.

1.5 PV COSTS, MARKETS AND FORECASTS

In the first 20 years of PV research, from the mid 1960s to the mid 1980s, the main focus was to make the product more efficient so it produced more power. Impressive gains in cell and module efficiency were made. Costs also fell dramatically as solar cells moved from pilot scale to semiautomated production.

Although the important figure of merit for cost is \$/kWh, typically \$/W_P is often used. Modules are rated in Watts of peak power (W_P). This is the power the module would deliver to a perfectly matched load when the module is illuminated with 1 kW/m^2 of luminous power of a certain standard spectrum while the cell temperature is fixed at 25°C. (By the way, these "standard test conditions" or STC rarely occur in real outdoor applications! See Chapter 16 for a complete discussion of testing conditions and Chapter 20 for real outdoor conditions.).

Figure 1.5 shows costs (\$/W_P) and production measured in MW_P over the commercial history of photovoltaics. Up until about year 2000, these values represent mostly c-Si solar cell technology. These two curves are typical of most new technologies. Initially, prices are high since volume production is low, so development and start-up

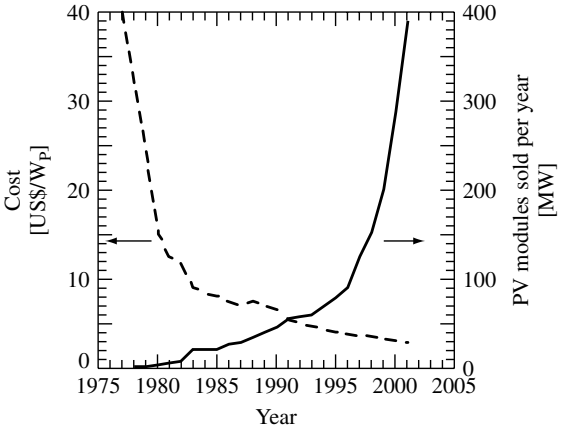

Figure 1.5 Historical trends of cost per Watt for solar cells and volume of production. Data from various sources. Beware: these costs are for PV modules not completed systems, which typically increase by a factor of 2 to 3

costs are spread over the relatively few units sold. The high price excludes most buyers except unique niche applications (i.e. remote telecommunications transmitters, where the unique properties of photovoltaics makes it the most appropriate source of electricity) government-sponsored programs (i.e. satellites, weather monitoring stations, military outposts and also human development programs in remote areas including water pumping), and curious wealthy pioneers (i.e. private homes in the mountains for environmentally concerned millionaires). As volume production increases, costs fall as economies of scale take over. The technology is now within economic reach of wider markets and demand grows rapidly as people with moderate incomes can afford the product. Eventually, the decrease in price slows, and it becomes harder to improve the cost and performance of a given product. But each small decrease in cost opens up larger markets and applications. Once a certain price is reached, a massive new market will open up with ample opportunity for investors to finance new manufacturing capacity.

This relation between cumulative production of PV modules in MW_P (M) and price in $/$W_P$ (p) can be described by an experience curve, which is characterized by a parameter E called the experience exponent [51, 52] or

$$\frac{p(t)}{p_0} = \left[\frac{M(t)}{M_0}\right]^{-E} \tag{1.1}$$

where M_0 and p_0 are the cumulative market and the price at an arbitrary initial time $t = 0$ (that we can take at the beginning of the early commercialization). The experience curve for photovoltaics is shown in Figure 1.6 where lowest price per W_P for a given year is plotted against the cumulative module production up to that year. When graphed as a log–log plot, it is the slope that is of significance since it defines the experience factor given as $1-2^{-E}$. This quantity indicates how much costs are reduced for every doubling of cumulative production. Figure 1.6 presents an exponent $E = 0.30$ which gives an experience factor of 0.19. Thus, prices have fallen 19% for every doubling in

cumulative production over the past 30 years. If the trend continues, the price of $\$1/W_P$ will be reached when the cumulative production reaches 10^5 MW_P.

It should be said that while the annual growth in sales of photovoltaics is quite spectacular, averaging 33% per year from 1995 to 2000, the experience factor of 0.19 is rather mediocre. For example, for semiconductor memories it is about 0.32, although for wind power it is only 0.15. PV technology has not reduced prices very effectively. This supports the idea that R&D must be supported to look for innovative options able to reduce prices beyond the safe path of the experience curve (additional argument for myth 4).

When this cumulative market will be reached can be determined, if we know the demand elasticity *S*. Technically, this is the logarithmic derivative of the annual market with respect to the price (changed of sign) and shows that one percent of price decrement will produce *S* percent of market increase. This parameter allows us to determine when in the future a certain level of price is reached [52].

Based on this, the installed PV power is given in Figure 1.7 for reasonable values of the demand elasticity. We can observe a fast initial growth, followed by a period of moderate growth. This second period is determined by the investment that society is willing to invest in this expensive energy technology. Extreme curves of the shaded area correspond to the expenditure for photovoltaics of the case that 0.05% (lower curve) and the 0.2% (upper curve) of the GDP of the industrialized countries is invested every year in PV electricity. As a reference, about 0.3% of the industrialized countries GNP is being given today as aid for development.

In 1992, a study (the RIGES scenario [54]) was presented to the Rio Summit analyzing the possibility of reducing the CO_2 emissions while maintaining a high economic growth rate in the developing countries. The dots represent the amount of photovoltaics to attain the RIGES requirements. In other words, the dots are the amount of installed photovoltaics required to be environmentally relevant and socially advanced. Note that

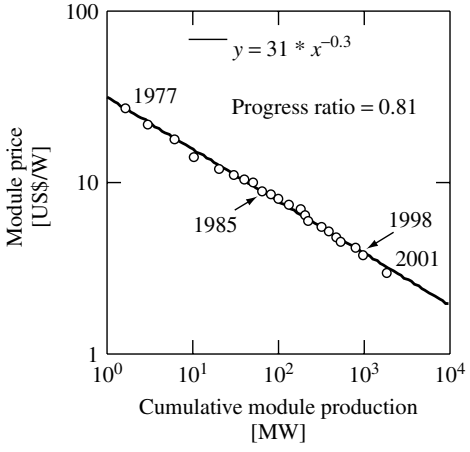

Figure 1.6 Experience curve for photovoltaics from 1976 until 1998 [53]. Straight line is fit indicating an experience factor of $1 - 2^{-0.3} = 0.19$

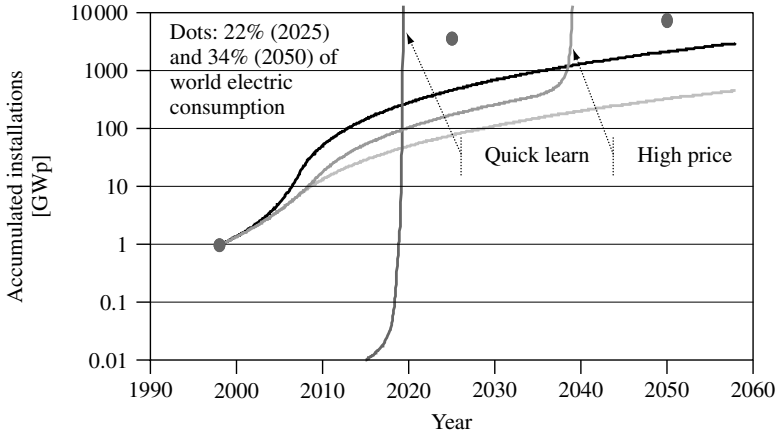

Figure 1.7 Long-term forecast of cumulative installed peak PV power. The dashed area represents the expected cumulative installed capacity for a range of assumptions associated with the demand elasticity. PV prices (not shown) will not be competitive in the period shown unless the conventional electricity doubles in price (in constant dollars). However, photovoltaics will be competitive if some innovation develops and is commercialized with a "quick learn" experience factor like that of the microelectronic memories (0.32). Dots represent the level of electricity penetration to reach environmental goals (see text)

the goal for 2050 is to produce the 34% of the total world electricity production; by no means a niche market to be produced by a cottage industry!

It is observed that with the present low experience factor, the environmental goals are not achieved. Nevertheless, this forecast predicts that the PV industry will be very large by the middle of the century.

The curve labeled high price refers to the case where conventional electricity prices are doubled. In this case, photovoltaics will reach price competitiveness with the existing electricity before the middle of the century (the almost-vertical line means photovoltaics is cheaper than conventional electricity but realistic growth will occur more slowly). Perhaps a hidden but practical conclusion of this analysis is that support to the PV industry will result in an additional element of security in the supply of electricity. Energy security is of increasing interest for the public officials as well as for citizens.

The preceding cases correspond to the situation governed by a constant experience factor. No technological breakthrough is considered. What would be the situation if a breakthrough were produced? A breakthrough technology would be characterized by a higher experience factor and should be able to reduce costs by experience faster than present PV technology. The curve labeled quick learning in Figure 1.7 shows the case of a technology with the experience factor of the microelectronic memories. Note that in very few years (after real commercialization starts) it would be able to reach competition with conventional electricity.

However, note that this success is based on reaching a certain cumulative market (in this exercise 10 000 MW) despite the higher price of this technology at its early stage as compared to the competing PV technology. This is a commonly occurring situation and

must be taken into account by investors. Comparison must not be made between prices of different alternatives at the same moment in time but for equal cumulated market. In other words, we must compare the price of an option today with that of its more mature competitor in some moment of the past and we must also consider the experience factor. In other words, sometimes a product that at a given moment is more expensive than its competition can become cheaper sooner because it bears internally the seed for lower cost and comparable performance. But, of course, not every more-expensive novel product bears this seed. This is the risky nature of entrepreneurship.

We conclude, and this is our position concerning the controversy pointed out in myth 4, that basic R&D in photovoltaics must be looking for breakthroughs if we want photovoltaics to fulfill the goals that society requests. At the same time, support to the market will help create a sizeable industry that will be able to commercialize breakthroughs worldwide. In any case we are not talking of a cottage industry. The PV industry has the potential of becoming a major electricity supplier in the twenty-first century and to constitute a powerful industry able to abate environmental stresses, to facilitate the human development of the poorest, and to constitute an element of safety in our electric supply.

1.6 WHAT ARE THE GOALS OF TODAY'S PV RESEARCH AND MANUFACTURING?

Chapters 5 to 15 in this book focus on individual technologies and will give specific examples of where the research and manufacturing effort is concentrating to reduce costs and improve performance. But several trends are common to all. These are listed in Table 1.3.

Since the overall goal is to produce a low cost PV *system*, we need more than low-cost-efficient solar cells, we need a low cost efficient system including mounting hardware, power conditioning electronics, fuses, cables, storage, tracking, and so on. Less research and development has gone into these areas than into PV solar cells and modules.

Table 1.3 Goals of current solar cell research and manufacturing

- Use less semiconductor material by making thinner cells or
- Use less expensive semiconductor materials. These tend to be less pure and less perfect.
- Improve solar cell performance with less expensive, less perfect semiconductors
- Even with this poorer material keep a high production yield, that is, reduce the number of cells or modules rejected by the quality control.
- Increase material utilization by reducing waste in semiconductor and cell fabrication
- Increase solar cell flux on the solar cells by using concentrators without increasing cost or optical losses too much. In this way, less semiconductor material is used.
- Increase solar radiation utilization by absorbing more of the spectrum efficiently
- Increase speed and throughput of manufacturing processes
- Simplify processing steps (this reduces fabrication costs and increases the yield) and reduce equipment costs
- Reduce costs and improve reliability of BOS (auxiliary elements).

1.7 GLOBAL TRENDS IN PERFORMANCE AND APPLICATIONS

Figure 1.8 shows the trends in efficiency achieved over the past 20 years for all the major PV technologies. These results are for small area "champion cells", the one-of-a-kind result that establishes the potential of a given material system and device technology. The highest efficiency is for the most expensive and complex devices, based on III–V technologies like GaAs and GaInP, consisting of multiple devices with different optical and electrical properties, grown on top of each other. They are discussed in Chapter 9. These multijunction (MJ) cells outperform other cell technologies for three reasons. They are made from very perfect and high-purity crystalline materials, they can capture either a wider range of the solar spectrum or the same range more efficiently than other devices, and they are operated with high concentration factors, using lenses, which increases the efficiency for reasons discussed in Chapter 3. Not surprisingly, they are also extremely expensive.

The workhorse of the PV industry is still Si as discussed in Chapters 5, 6, and 7. Si wafers in the form of either single crystal Si or multicrystalline (also called polycrystalline) Si accounts for 90% of the PV market. Although champion single crystal (c-Si) and multicrystalline Si (multi-Si) cells have been recorded with 25% and 20% efficiency, respectively (both made at UNSW in Australia), the difference in module performance between the two Si-wafer technologies is much smaller. They have typically 14% and 12% efficiency in commercial modules, respectively. Despite three decades of research and manufacturing, clever scientists and engineers are still finding ways to improve the performance of Si-wafer photovoltaics. They are also finding ways of reducing the cost.

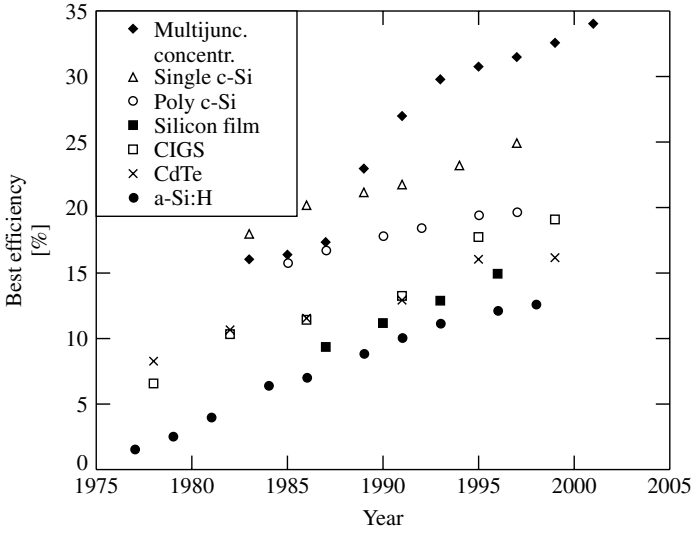

Figure 1.8 Best small area (0.5–5 cm^2) efficiency for various cell technologies measured under standard laboratory test conditions. MJ concentrators are double junctions before 1995, and triple junctions after. a-Si represents stabilized efficiency after extended light soaking and are MJ after 1990 (see Chapter 12)

Among these attempts are the developments of silicon sheets, which avoid the wafering of bulky Si ingots, a very expensive and wasteful process. Ribbon sheets have already reached a noticeable fraction of the market with two companies: RWE in Germany/USA (leading) and Evergreen Solar in the USA.

Continuing down the efficiency axis we come to the three leading thin-film PV contenders, $Cu(InGa)Se_2$ (CIGS) (Chapter 13), CdTe (Chapter 14), and a-Si (Chapter 12), in that order. The main motivation for interest in thin-film photovoltaics has always been the possibility of lower cost, not higher performance. Their champion cell performance has always been a factor of about 2 lower than Si-wafer technologies until ~2000, when $Cu(InGa)Se_2$ cells with efficiencies of 19% were reported, putting them in potentially close competition with multi-Si, although there are vast differences in the manufacturing experience base between $Cu(InGa)Se_2$ (no base) and multi-Si (large base). The benefits and challenges of thin-film PV technologies are discussed in detail in Section 1.9. Finally, we note that the category of "Si film" solar cells in Figure 1.8 is a special case of solar cells developed entirely by one company (Astropower in the USA), in which they are attempting to achieve the high performance of polycrystalline Si with the low-cost approach of thin films. More information about thin-film Si technology is given in Chapter 8.

The results in Figure 1.8 clearly show that there are many promising technologies in terms of their possibility of achieving rather high efficiency. But the reality is that, as seen in Figure 1.9, almost 90% of the world's PV power modules are either single c-Si or multi c-Si. The evolution shows a trend away from c-Si towards the multicrystalline-Si technology with the market share of Si sheet also increasing. About 10% of worldwide PV sales are a-Si/a-Si or a-Si/a-SiGe multijunctions and the remaining <1% is $Cu(InGa)Se_2$, CdTe, and concentrators. The multijunction concentrators based on GaInP/GaAs cells have yet to find commercial application on Earth but nonconcentrating GaInP/GaAs cells are commonly used for space missions where their high efficiency is more important than their high cost. High performance GaInP-based technology is discussed in Chapter 9 and PV space power is described in Chapter 10.

Who is making all the PV modules? Figure 1.10 shows the breakdown by the three major geographic regions of Europe, Japan, and the United States. Note that this is a logarithmic scale, indicating very steady growth for the past decade of 20 to 30%. Production in 2001 was actually 36% higher than in 2000. The USA has had steady growth and led the world in photovoltaics between 1992 and 1998 when Europe and Japan

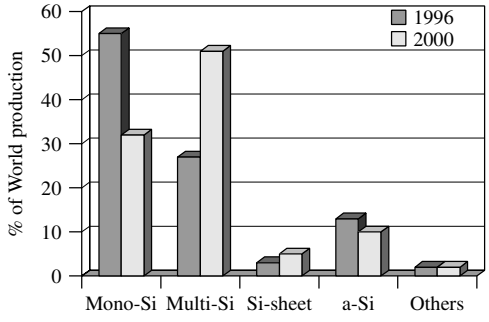

Figure 1.9 Distribution of the PV market by technologies

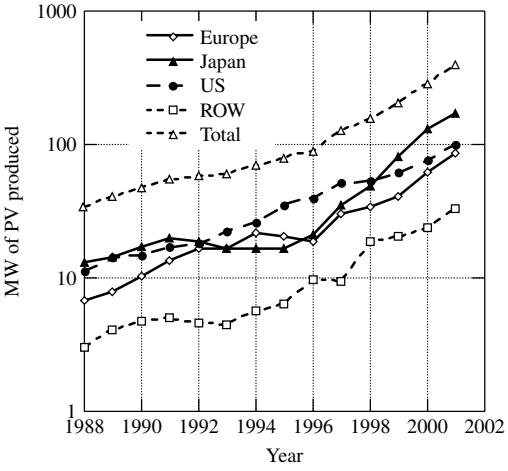

Figure 1.10 World production of PV modules

had static manufacturing growth. Then in 1998, progressive and supportive government policies in many European countries and in Japan resulted in a substantial increase in production. These policies were driven partly by a strong commitment to CO_2 reduction as proscribed by the Kyoto Protocol. European production is dominated by Spain closely followed by Germany, and to a lesser extent France, Italy, and The Netherlands. Note that these figures do not indicate the final residence of the PV module, only its place of birth. For example, a large fraction of PV modules made in the US (∼70%) and Spain (∼80%) are in fact exported.

We present in Figure 1.11 the top ten PV manufacturers in 2001 [55]. The list is headed by the Japanese electronics company, Sharp, followed in the third position

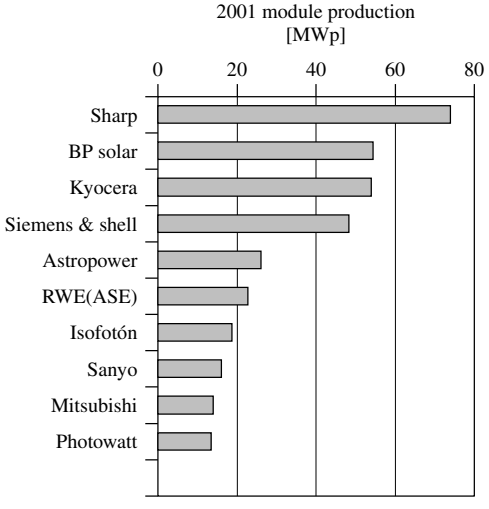

Figure 1.11 The top ten PV cell manufacturers in 2001

by Kyocera, another Japanese company. The second place is held by the UK-based oil multinational BP Solar with c-Si and multi-Si plants in United States, Spain, Australia, and India. BP Solar also had two thin-film technologies in commercialization in the United States, namely a-Si and CdTe, (see footnote in Section 1.4). The biggest PV manufacturer in the USA today is Shell Solar (formerly Siemens Solar) but is held by European capital. As of this writing, of all the companies in Figure 1.11, only Astropower (US), Isofoton (Spanish), and Photowatt (French but held by Canadian investors) focus their business exclusively on photovoltaics. The others are either divisions or subsidiaries of large companies with diverse manufacturing interests.

Figure 1.3 showed the worldwide trend for various applications. Growth has been driven by distributed, grid-connected PV applications since 1996, mostly in Europe and Japan, as discussed above. There is steady growth in use of photovoltaics for diesel hybrid and communication. These are off-grid applications, typically in remote locations. Previously, operating a diesel generator 24 h a day or replacing large battery packs was the only alternative. PV diesel hybrids can be cost-effective in these cases [56].

Note that Figure 1.3 shows that large-scale, centralized solar power plants are almost nonexistent. These huge "solar electric farms" were envisioned in the early days of photovoltaics to be built in sunny arid deserts, where land was essentially worthless for other uses (note, that photovoltaics operates without water in contrast to conventional thermal power plants). These huge facilities would replace conventional power plants, at least for daytime power. The world's largest centralized PV power plant to date was installed in central California between 1984 and 1985. The operation and performance over several years was reported [57], including operation and maintenance costs [58]. After several years of operation, the installation was disassembled and the modules were sold individually on the market. Presently, the largest centralized PV power plant is 3 MW in Serre, Italy [59]. There have been several other large-scale PV installations, and their installation techniques, labor, and operation costs have been well documented. In particular, the 0.4 MW a-Si plant in California, USA [60] and the 0.48 MW concentration plant [61] in Tenerife, Spain are notable because they do not use the ubiquitous unconcentrated c-Si technology.

1.8 CRYSTALLINE SILICON PROGRESS AND CHALLENGES

Figure 1.9 showed that c-Si, as either single or multicrystalline wafers or ribbons, was responsible for almost 90% of worldwide PV production in 2001. How did its dominance occur?

First, there was a tremendous worldwide scientific and technical infrastructure for Si starting in the 1960s. Huge government and industrial investments were made in programs for understanding the chemical and electronic properties of Si, how to grow it with the required purity and crystalline structure, and to create the equipment needed to perform all the processing steps. The motivation was not just idle scientific curiosity, but rather the competitive drive to manufacture increasingly complex integrated circuit chips, which created first the analog then the digital electronic revolutions leading to our current information, entertainment, and telecommunications industries. The promise of wealth and market dominance led public and private organizations to unlock many

secrets of Si technology. The silicon band gap, of 1.1 eV, is almost optimum to make a good solar converter, as explained in Chapters 3 and 4. The PV industry could utilize the preceding gains for their own application without having to re-create this scientific and technological infrastructure. In addition, Si is one of the most abundant minerals in the Earth's crust. Thus, there was no physical limitation to providing a huge fraction of the Earth's electricity needs with the known Si reserves.

However, for mechanical reasons (it is brittle), silicon requires relatively thick cells, with a typical wafer thickness of about 300 μm. Therefore, some of the electrons pumped by the photons to the conduction band have to travel large distances, on the order of the thickness, to be extracted by the front face through the selective contact to this band (the *pn* junction). Consequently, a good material with high chemical purity and structural perfection is required to fight the natural tendency of the conduction-band electrons to return to the valence band. This loss process is called *recombination*. To avoid this loss, the electrons must be highly mobile, as they are in perfect silicon. Impurities and imperfections must be avoided as they can absorb the extra energy of the conduction-band electrons and convert it into heat, thus eliminating the free electron from traveling through the circuit by immediately restoring it to the valence band energy. Producing heat, which is desirable in solar thermal panels, where this heat is transferred to a fluid, is undesirable in PV modules, where we try to recover the solar energy as electricity, of much higher value.

Metallurgical Grade (MG) Silicon is obtained by reduction of quartz with coke in an arc furnace. Then it is strongly purified by a method developed by and named after the Siemens Company consisting of the fractional distillation of chlorosilanes, which are obtained from the reaction of HCl with Si. Finally, silanes are reduced with hydrogen at high temperatures to produce hyperpure silicon, usually called *Semiconductor Grade* (SG) *Silicon* or just *polysilicon* (it is called *polysilicon* because it has many grains of crystalline Si, typically of about 1 mm).

The polysilicon now has the desired chemical purity (unwanted impurities below the parts per billion (ppb) level, or less than one impurity atom for every 10^{12} Si atoms, for some impurity atoms), but its structural quality is deficient. The structural quality is improved by melting the polysilicon ($>1400^{\circ}$C) and "freezing" or allowing it to solidify very slowly around a rotating crystalline seed, usually by the Czochralski (Cz) method. In this way, a cylindrical single crystalline ingot is obtained of about 25 cm diameter and of 100 cm length. In this step, a very small number of atoms of boron are introduced in the melt to allow the appropriate metallic contacts deposited later to be selective to the valence-band electrons. This forms the *p*-type side of the *pn* junction.

The ingot is now cut in wafers with a saw. For this a very long wire (up to 500 Km) is wound many times on rotating drums cuts with slurry the silicon ingot into wafers. However, the process is slow and about half of the silicon is lost in the sawdust. The challenge here is to cut the wafers thinner so as to make more profit from the silicon. Wafers of 150 μm instead of the standard 300 μm are used in some companies. The techniques and challenges related to crystal growth and sawing are described in detail in Chapter 6.

The wafer is now etched slightly to remove the saw damage and to condition (texture) the surface for better light absorption. Then the conduction-band selective contacts

are made by introducing atoms of phosphorus to one surface of the wafer, making it the *n*-type partner in the *pn* junction. This is done by locating the wafers in a phosphorus rich atmosphere at high temperature so that these atoms penetrate slightly (~0.2 μm) into the silicon wafer.

Then metallic grids are printed on the boron and phosphorus-doped zones (some tricks, sometimes proprietary, are used to separate boron- and phosphorus-doped regions properly) and the solar cell is thus finished. The grids make it easier to collect the electricity without resistance losses and are commonly applied with low cost screen-printing methods. But a solar cell is brittle and produces low voltage (about 0.5 V) so that some 36 cells (or multiples of this number) are interconnected with tinned copper ribbons and encapsulated in a sandwich formed of a sheet of tempered glass, an embedding polymer that surrounds the solar cells, and a back sealing plastic layer. The reason for multiples of 36 cells is so that their output voltage ~15 V will be compatible with most DC battery charging applications.

The lowest (publicly offered) module selling prices in 2002 were about $\$3/W_P$. The breakdown of costs, as given in Chapter 6 are presented in Figure 1.12. The wafer itself represents about 65% of the module cost, approximately equally divided between purification, crystallization, and sawing. This hyperpure silicon is found today as a scrap or waste product from the microelectronics industry at a price of ~$50/kg. The increase of the PV market in the 1990s has nearly exhausted this market. Additional supplies are coming from the former Soviet Union, whose microelectronic industry has disappeared due to western competition. The Siemens method is considered ultimately too expensive for photovoltaics, but the purity it provides seems necessary for the fabrication of solar cells. Attempts in the 1980s to fabricate a low-cost solar silicon (SolSil) did not succeed due in part to the scarce interest generated by the small markets of the time. Today, new attempts are being made. These might include purification in the MG silicon production steps and in the crystal growth steps avoiding the expensive chlorination procedure and using the molten step of the crystal growth for further purification, or alternately, reducing the chlorosilanes in the molten phase prior to the crystal growth. It is not clear whether they can achieve the needed purity level. Even if feasible it is uncertain whether such wafers would be less expensive than the standard Siemens process or some simplified versions of it. There are fears that a shortage of hyperpure polycrystalline silicon availability might seriously hinder the growth in cell production demanded by the market. Chapter 5

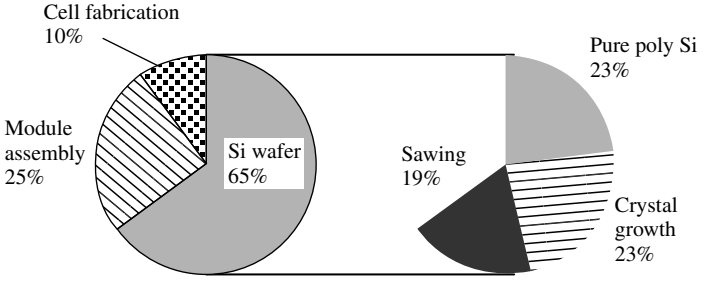

Figure 1.12 Breakdown of costs in the fabrication of a Si-wafer-based PV module. The right side presents the wafer costs

describes in detail the problems and challenges associated with silicon production and purification.

An important advance in solar cell fabrication was the demonstration that solar cells with high efficiency can be fabricated from wafers containing hundreds of large-grain (1–10 mm) multicrystals, called multicrystalline (multi-Si) or polycrystalline (poly-Si), although this later term is less favored because it may cause confusion with the feedstock (polysilicon). The multi-Si growth procedure is much faster and the wafer is cheaper. The loss of efficiency of a few percent (absolute) caused by the random orientation of crystalline grains in a multi-Si wafer compared to a single c-Si wafer is balanced by the lower cost so that the price per watt peak is the same on a module basis. But the simplicity of the multi-Si wafer-growing equipment and process is producing a clear trend towards the use of the multicrystalline option as seen in Figure 1.9.

An interesting option in Si solar cell manufacturing is the growth of ribbons [62, 63]. Ribbons do not require the expensive sawing process. However, the growth of the ribbon crystal is slower because they usually grow in the plane perpendicular to the ribbon surface, with very small area (the ribbon width times the thickness). In contrast, wafers grow in the plane of the wafer surface whose area is the wafer area. The standard ingot solidification process is a very effective purification process due to the preferential segregation of impurities to the molten silicon. However, in ribbon Si the plane of solidification moves faster (although with very small area), so the segregation is less effective. In summary, the ribbon cells are almost as good as the multicrystalline bulk-grown cells and possibly cheaper. Challenges lie in increasing the growth speed and the resulting cell efficiency.

Although the solar cell manufacturing process represents a relatively small fraction of the total cell cost, it strongly affects the overall cost in $\$/W_P$ because it determines the cell and module efficiency. This efficiency depends on the quality of the wafer or ribbon utilized but it also greatly depends on the cell process itself.

As a matter of fact, an efficiency of 25% has been achieved for laboratory cells in a long complex process where every possible efficiency-improving detail has been implemented to produce a complicated but nearly ideal device structure. This is explained in Chapter 7. However, most factories use some variation of the wafer and cell fabrication process described above, including the screen-printing process, that leads to 15% single crystal cells or 13% multicrystal cells. In modules, these efficiencies are reduced to 14% or 12%, mainly due to the redefinition of area that now includes the module frame. This process is considered the best compromise between costs and performance.

The existence of the large efficiency gap between laboratory and commercial cells, together with the increasing markets, suggest that novel, high efficiency commercial cell processes will appear in the next years. Some companies (BP Solar or Sanyo, for instance) are already on this path and have different processes leading to 17 to 18% cells in production. It is worth noting, that the ribbon technology is incompatible (see Chapter 7) with the ubiquitous screen-printing processing, so that a new processing, which may not be so cheap, is required to fabricate cells with this material.

An additional factor very seriously affecting the cell cost is the production yield. In the fabrication of any semiconductor device, not every unit introduced into the production

line is successfully completed. In good single crystal Si cells, the manufacturing yield is 95%. Many supposedly cheap technologies find their Achilles' heel in the low yield.

Finally, the module fabrication requires interconnecting and encapsulating the cells. These steps also have room for some cost reduction. The use of cheaper materials may help somewhat, as well as better automation, better module interconnection, and integration designs.

1.9 THIN FILM PROGRESS AND CHALLENGES

One might ask "why develop a totally different semiconductor technology for photovoltaics when Si is so well established?". The simplest answer is "to achieve lower cost and improved manufacturability at larger scales than could be envisioned for Si wafer-based modules." In fact, we have already defended our belief that Si technology, very important in the next decades, will not be able to reach the ultimate goals required for mass worldwide penetration of photovoltaics (Section 1.5). What were the disadvantages of c-Si that led to the early investigation and eventual commercialization of alternatives? It was recognized early in the development of photovoltaics that Si crystals were expensive and slow to grow. It was also recognized that of all the viable semiconductors, Si would require the greatest thickness to absorb sunlight, due to its unique optical properties. Si is the most weakly absorbing semiconductor used for solar cells because it has an indirect band gap while most of the other semiconductors have a direct band gap (see Chapter 3 for a more complete explanation of direct and indirect band gaps). Therefore, at least ten times more crystalline Si is needed to absorb a given fraction of sunlight compared to other semiconductors like GaAs, CdTe, $Cu(InGa)Se_2$, and even other forms of Si such as a-Si. Thicker semiconductor material means higher material volume but also a higher quality material because of the longer paths that the high-energy electrons excited by the photons must travel before they are delivered to the external circuit to produce useful work. All this leads, as seen before, to high material cost. In addition, we mention that, presently, much of the Si-PV industry relies on buying scrap material from the electronics industry. As photovoltaics' demand grows, the supply of scrap material might become insufficient (see Chapter 5).

It was recognized almost as early as c-Si PV cells were developed in the 1950s that other semiconductors could make good solar cells. Most of them exist in a form called thin films. When they are fabricated into useful devices, they are so thin that they must be deposited on a foreign material called a substrate for mechanical support like a layer of paint on a piece of wood or the reflective metal coating on glass to form a mirror. A framework for analyzing the material properties, device structures, and manufacturing issues unique to thin-film solar cells (TFSC) was developed [64] since they differ considerably from Si wafers. Throughout the 1970s, progress in Cu_2S/CdS solar cells led to the development of new theories to explain the device performance, new methods of materials processing, and new concepts in semiconductor device manufacturing [65, 66]. Between 1981 and 82, four thin-film technologies demonstrated the ability to cross the magical 10% efficiency barrier, thus becoming candidates for serious consideration: Cu_2S/CdS [67], a-Si [68], $CuInSe_2$/CdS [69], and CdTe/CdS [70]. (It is an inexplicable fact in this business that 10% efficiency seems to suddenly confer respectability and status to any PV technology.) Of these four TFSC technologies, Cu_2S/CdS would soon be

rejected for commercialization due to fundamental and fatal stability problems related to electrochemical decomposition [71]. In contrast, a-Si has a minor stability problem that is not catastrophic and has not been a major barrier to further development and production as discussed in Chapter 12. No fundamental stability problem has been found with $Cu(InGa)Se_2$ and CdTe modules. Consequently, significant industrial and government-sponsored research and development resources have been directed worldwide at TFSC technology. This has led to steady progress in champion cell efficiencies as seen in Figure 1.8.

The main advantage of TFSC is that they will eventually have lower costs than c-Si-wafer PV technology when they are produced in sufficiently large volumes to offset the initial capital investment. The lower costs of TFSC derive from the following characteristics: they are typically 100 times thinner than Si wafers ($\sim$1–3 μm for all the semiconductor layers) deposited onto relatively low-cost substrates such as glass, metal foils, and plastics; they are deposited continuously over large areas at much lower temperature (200 to 500°C vs $\sim$1400°C for c-Si); they can tolerate higher impurities (thus needing less expensive purification of raw materials); and they are easily integrated into a monolithic interconnected module. For a reference, the semiconductors in typical TFSC are 10 times thinner than a human hair. TFSC are either polycrystalline with small $\sim$1 μm sized grains such as $Cu(InGa)Se_2$ or CdTe, or else amorphous like a-Si. This is a consequence of being deposited at temperatures too low to allow perfect crystalline bond formation. TFSCs typically consist of 5 to 10 different layers whose functions include reducing resistance, forming the *pn* junction, reducing reflection losses, and providing a robust layer for contacting and interconnection between cells. Some of the layers are only $\sim$20 atoms thick (10 nm), yet they may be a meter wide! This requires excellent process control. The manufacturing process is designed such that they are deposited sequentially on moving substrates as in a continuous process line. This minimizes handling and facilitates automation, including laser scribing, to isolate and interconnect individual cells on the module, called monolithic integration.

With all the advantages of TFSCs, why does c-Si or multi-Si still dominate 90% of the world market? This brings us to the disadvantages of TFSC: they have lower efficiencies (so far), and they have a much less-developed knowledge and technology base compared to c-Si. Consequently, under-capitalized companies have had to struggle to develop not only an understanding of the materials and devices but also the equipment and processing to manufacture them. The thin-film PV industry has had to develop the technologies all by itself with considerably less financial resources than the Si industry had. They were not able to adopt a mature technology like the Si PV community did from the Si electronics industry.

What are the strengths and remaining challenges for the TFSC industry? We will review the salient characteristics of the three leaders: a-Si, $Cu(InGa)Se_2$/CdS, and CdTe/CdS.

Amorphous Si (Chapter 12) is deposited from hydride gases such as SiH_4 using plasma to decompose the gas. This is called *plasma-enhanced CVD* (PECVD) and allows for large areas to be coated rather uniformly and with excellent control. However, the utilization of gases is only around 10 to 30%, meaning much of the source material is

wasted. The material has 1 to 10% hydrogen bonded to the Si, and is often designated as *a-Si:H*. The H atoms passivate a large number of the defects resulting from the incomplete bonding of the Si atoms. The atomic structure has no long-range order like all other crystalline or polycrystalline materials. This can be an advantage. Films are typically deposited between 150 to 300°C, the lowest temperature of any of the TFSC materials, allowing the use of lower-cost, low-temperature substrates. a-Si solar cells are deposited on glass, stainless steel foil, or plastic. The last two substrates are flexible allowing for "roll-to-roll" manufacturing where all the layers are deposited as the roll moves through their process zone. The *pn* junction is formed by doping the thin contact layers as they grow with dopant gases containing the boron or phosphorous atoms. All practical a-Si modules contain multiple junction devices where two or three junctions are grown on top of each other. This allows for more efficient utilization of the sunlight. The total thickness, including multiple junctions and all the contact layers, is less than 1 μm excluding the substrate. The highest reported efficiency was 15% for a triple junction, which degraded to about 13% before stabilizing. While a-Si TFSCs cells may have slightly poorer performance compared to other TFSCs when tested under laboratory conditions (Figure 1.8), they have a unique feature that improves their relative performance outside in real conditions; namely, their efficiency is temperature-independent while for all other PV technologies, c-Si or thin-film, the efficiency decreases as the module heats up as in real outdoor conditions. This can result in those other modules losing 2 to 4% (absolute) of their rated output in the summer time and helps a-Si look more favorable. The three major challenges for a-Si technology are: 1) to improve the efficiency from today's 6 to 8% up to 10 to 12%; 2) minimize or eliminate the self-limited degradation which reduces efficiency by 2 to 3% (absolute); and 3) to increase the deposition rate of the layers and the utilization of the gases to allow for faster, lower-cost manufacturing.

Polycrystalline layers of $Cu(InGa)Se_2$ (Chapter 13) alloys have produced the highest efficiency TFSC devices and modules. TFSCs based on $CuInSe_2$ (no Ga) achieved 12 to 15% efficiency but were limited by the low band gap. Alloying with Ga and/or S increases the band gap and increases the efficiency of delivering the electrons to the circuit (as discussed in Section 1.2). While many deposition methods have been explored in the laboratory, there are two different processes under commercial development. Co-evaporation forms the alloy by simultaneous evaporation of the Cu, In, Ga, and Se from sources onto a heated substrate. The other process is called *selenization*, because layers of Cu, In, and Ga are deposited by various means onto a substrate, then heated in the presence of Se from a gas such as H_2Se or a Se vapor, thus contributing the fourth constituent of the alloy. Substrate temperatures typically reach 500 to 600°C during some stage of the growth. Substrates of Mo-coated glass are typically used although metal foils or plastic are being investigated. The $Cu(InGa)Se_2$-films are *p*-type, typically 1 to 3 μm thick and have crystallites or grains on the order of 1 μm. The *pn* junction is formed by depositing an *n*-type layer of CdS, ZnO, or other new materials under development to replace the CdS. The highest reported cell efficiency is presently 19% and several companies have reported modules with >10% efficiency. However, progress has been largely empirical since little fundamental understanding of the materials or devices is available. A very active area of research is developing methods to incorporate other alloys to increase the band gap even further. The three major challenges for $Cu(InGa)Se_2$-related technology are: 1) to control the composition (Ga, S, Se, or Na) of the alloy through the film in a

manufacturing environment on a moving substrate; 2) to find alternative junction partners to replace CdS; and 3) to find new alloys or new deposition methods to give high performance devices with higher band gap alloys.

Polycrystalline layers of CdTe (Chapter 14) have been investigated for photovoltaics since the 1970s. In contrast to limited process options for a-Si or $Cu(InGa)Se_2$, there are over 10 methods to deposit the CdTe films that have produced CdTe solar cells exceeding 10% efficiency. Four have reached precommercialization: spray pyrolysis (SP), electrodeposition (ED), vapor deposition (VD) and close spaced sublimation (CSS). Some take place in liquid baths that are barely warm $\sim 50^{\circ}C$ with CdTe deposition rates of μm/hr (ED) while others take place in vacuum systems at temperatures high enough to soften glass $\sim 600^{\circ}C$ with CdTe deposition rates of μm/min (CSS). There seem to be three critical steps, however, that all efficient CdTe solar cells require. First, they need a post-deposition anneal in the presence of Cl and O_2 at around $400^{\circ}C$. This chemical/thermal treatment enlarges the grains, passivates the grain boundaries, and improves the electronic quality of the CdTe. Second, all CdTe layers need a surface treatment before applying a contact. This treatment can be a wet or dry process and prepares the CdTe surface by etching away unwanted oxides and leaving a Te-rich layer needed to make a low-resistance contact. Third, all high efficiency devices have a Cu-containing material somewhere in their CdTe contact process but again, there are many ways this can be achieved. Whichever process is used to deposit the CdTe, it has been found that the entire device process is highly coupled since processing steps strongly influence previous layers. This is partially due to the CdTe grain boundaries which act like paths for interdiffusion.

The *pn* junction is formed by first depositing an *n*-type layer of CdS on a transparent conductive oxide substrate followed by the CdTe layer and appropriate chemical annealing. Once the solar cell is made, the CdTe films are slightly *p*-type, typically, 2 to 8 μm thick and have crystallites or grains on the order of 1 μm. The highest reported efficiency for a CdTe/CdS device is presently 16%. Some CdTe modules have been in outdoor field-testing for over five years with negligible degradation, yet other CdTe devices degrade during accelerated life testing indoors. Of the three leading TFSC technologies, CdTe may have the most challenges. The dual role of Cu must be resolved; it seems to be required to produce a high-efficiency device but it is also implicated in long-term stability problems. The various optimizing treatments need to be better understood so they can be simplified and transferred into production. CdTe modules may be more sensitive to atmospheric interaction (O_2, H_2O) requiring better encapsulation methods. Finally, safe and cost-effective Cd usage in the workplace followed by recycling at the end of the module's life need to be determined.

In fact, technically astute investors know that other factors can be more important than efficiency in selecting a technology for development. This point is made loud and clear by examining the relative performance of the three major TFSC technologies – $Cu(InGa)Se_2$, CdTe, and a-Si – in Figure 1.8. Note that a-Si has always had the lowest efficiency. Yet, of the three, it was a-Si that has been commercialized much earlier and more widely. It enjoys by far a much greater manufacturing capacity. As of 2001 [72], a-Si accounted for almost 9% (34 MW) of the world PV power module production, while CdTe and $Cu(InGa)Se_2$ power modules together accounted for less than 0.3% (1 MW), despite a-Si champion-cell-stabilized efficiency lagging the others by several percent. In

reality, typical production modules of a-Si and CdTe are in the 7 to 8% range while Cu(InGa)Se_2 is 9 to 10%.

Why has so much capital been invested to develop a-Si technology over CdTe and Cu(InGa)Se_2? A major factor was that a-Si had a stronger worldwide scientific research base, which ensured that the relation between deposition conditions and fundamental material and device properties were well characterized. In contrast, CdTe and Cu(InGa)Se_2 are "orphans" because they have no real application outside of photovoltaics. Therefore, the entire knowledge base and technical infrastructure had to be developed mostly by underfunded industrial groups and a small number of university and government research labs. This shows that translating research-grade champion cell performance into production modules coming off-the-line day after day is a very challenging task. Figure 13.23 in Chapter 13 shows the time delay in translating efficiency achieved in the lab for a small area cell to a prototype large area module for the Cu(InGa)Se_2 technology. Delays of six to eight years are typical. To conclude, the highest efficiency technology is not always going to be the best choice for a low-cost, high-yield process, at least not until much of the technical background is in place.

Recognizing that the ideal PV technology would have some of the merits of c-Si but be deposited as a thin film a few microns thick, several groups have elected to try to achieve the "best of both worlds" by developing thin films of multi-Si deposited on a substrate. This is the subject of Chapter 8. At present, the best thin-film multi-Si solar cells have the same efficiency as their $CuInGaSe_2$, CdTe, or a-Si based predecessors. This is partly because multi-Si thin-film photovoltaics also inherits some of the problems of both c-Si and thin films. In particular, passivation of grain boundaries and surfaces seems to be a major problem, yet many of the well-established passivation methods from c-Si are not applicable to multi-Si thin films.

But there are new thin-film technologies such as the dye-sensitized solar cell that operate on a very different principle than an all-solid-state solar cell, almost more like photosynthesis than photovoltaics. This fascinating new solid–liquid technology, not free of challenges either, is described in Chapter 15.

1.10 CONCENTRATION PV SYSTEMS

If solar cells are expensive, focusing concentrated sunlight onto fewer solar cells was considered from the earliest times as a way of reducing costs. For example, instead of a typical 100 cm^2 solar cell absorbing 100 cm^2 worth of sunlight, one could focus the sunlight from 100 cm^2 onto a 1 cm^2 of solar cell, thus reducing the solar cell cost by 99% while still utilizing the same amount of sunlight. This neglects the cost of the optical focusing elements and other special equipment needed for concentrator technology. Of course, two conditions were required. One is that the optical surface collecting the light and redirecting it to the cells had to be cheaper than the cell area it replaced and the second is that the efficiency of the cells under concentrated sunlight should not decrease substantially. The first condition is generally fulfilled if we consider only the optical surfaces. However, keeping the cells constantly in focus requires a moving structure to keep the optics pointing at the sun as it moves across the sky, which adds cost to the system. As for the cell efficiency, there are fundamental reasons (see Chapter 3) why

it should increase with increasing luminous flux. However, in practice, ohmic resistance losses caused by the handling of large currents limits the efficiency increase. Thus, cells for concentrator applications must be carefully designed to minimize such losses and therefore they become more expensive. Yet, the small area of cells used in a concentration system, or alternatively, the large amount of electric power produced by each cell, allows for paying higher costs for the cells, and therefore allows them to incorporate many refinements in order to make such cells very efficient.

One factor that reduces the system efficiency is the loss associated with the optical hardware used to concentrate the light. Additionally, only the direct sunbeam is collected since scattered (diffuse) light is not focused. This again reduces the electric output by at least 15%. However, this last reduction is compensated for in many sunny locations by the fact that the tracking system always aims the cell directly at the sun (at least for two-axis tracking systems). In contrast, with the more typical stationary modules, the output power varies like the cosine of the angle of the sun, so this is very low in morning and late afternoon, when the sun is at an oblique shallow angle relative to the module (equations describing the sun's motion and the relative illumination on a module versus time of day or time of year is given in Chapter 20). Accounting for these gains and losses, it is generally found that concentrator efficiency today tends to be somewhat higher than flat module efficiency and this tendency will increase in the future with the adoption of higher efficiency cells. It is also believed that concentrators should ultimately be cheaper than flat module silicon solar cells. However, this statement has not been confirmed in practice due to the lack of a real market, apart from a few purchases for demonstration purposes.

Actually, concentrators are appropriate for relatively large installations while the PV market has evolved so far in smaller installations such as grid-connected houses, remote homes, or telecommunication applications whose size is seldom bigger than 5 kW. Therefore, only very few companies fabricate concentrator cells today, and their prices are very high because they have large general costs for very small production volumes. However, the situation may change. The general increase of the PV markets will probably stimulate the appearance of niches better adapted to concentrators.

The difficulty of developing concentrators must not be underestimated. Combining the requirement for high performance with the low cost is a formidable challenge. In particular, the optics must be low cost, yet permit highly accurate focussing, high optical efficiency, and equal illumination in all cells. The tracking structure must be cheap and accurate, cells must be efficient and not too expensive, and finally the cooling and current extraction must be effective and cheap. Chapter 11 deals in detail with concentrator issues.

1.11 BALANCE OF SYSTEMS

A photovoltaic system consists of more than PV modules composed of solar cells. In addition, it requires elements that are generically known together as "*Balance Of System*" (BOS). The BOS is, typically, composed of the battery, the control unit and the inverter, the mechanical support structure, the electric cabling, and protection devices such as fuses, grounding rods, and disconnect switches. We present in Figure 1.13 the cost of a PV stand-alone installation with storage, as presented in Chapter 2.

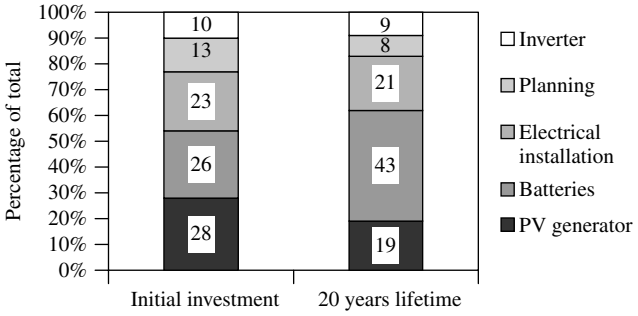

Figure 1.13 Breakdown of costs of a stand-alone PV installation with an optimum size storage. Differences in the initial investment and the life cycle investment are due to replacement of batteries during the 20 year life

We can see that in this case the PV modules represent approximately a quarter of the cost, while the cost of the batteries exceed that of the PV modules, especially when their periodic replacement over 20 years is included. This makes a very important and little appreciated point: even if we could make PV modules for free, the life cycle cost of the stand-alone system in Figure 1.13 would only be reduced by 25%! Clearly, batteries must be examined more closely. It is fortunate that many important applications do not require battery storage and therefore are free from this major cost burden.

Batteries are in most cases the lead-acid type. While automobile batteries are optimized for providing strong current for a short period to start the car, the ideal batteries for PV systems are so-called "deep cycle" batteries that can yield a large fraction of their charge (deep discharge cycle) and must operate with high efficiency and long duration. Yet, many PV applications use standard "shallow discharge" auto batteries due to their ubiquitous availability and lower initial cost (due to massive worldwide markets and applications) to the detriment of the long-term PV system cost. Some of the modern batteries such as those based on lithium ion or lithium polymer used in laptop computers or mobile phones could be used in solar applications but they are too expensive and are not significantly better than properly managed lead-acid batteries. This is studied in detail in Chapter 18. As said before, the relatively high cost of the batteries is further increased when we consider the costs over the PV system's life cycle since the batteries have to be replaced every four to eight years due to their relatively short lifetime. Therefore, good maintenance procedures to increase the battery lifetime are important but not always applied. Alternative methods of storage exist but they will not replace lead-acid battery, at least, not in the next ten years.

The battery charge controller is essential for the long life of the battery. It is an electronic device that prevents overcharging and excessive discharging, both of which can dramatically shorten the battery's life. In large systems, equilibration of the battery charging (so that all battery cells charge equally) should also be incorporated. In hybrid systems, which combine photovoltaics and a diesel or wind generator, the control unit must connect and disconnect the different generators according to a plan. Also, loads can be categorized, so that in case of low battery charge and low PV output, some loads can be disconnected while some essential ones are maintained active.

In many cases, battery storage is not necessary. For PV-powered water pumping, the water is pumped and stored while the sun is shining. For the grid-connected homes (one the fastest growing applications) and office buildings, the photovoltaics produces energy during the day and the grid supplies the energy during the night or on cloudy days, thus eliminating the need for batteries, simplifying system design, and reducing BOS costs. In PV-powered generating plants, the electricity is produced while the sun shines. The success of grid-connected PV applications is very sensitive to price competition with conventional electricity (even if the PV electricity is subsidized, as it occurs in Europe and Japan). Luckily the expensive batteries do not hamper this competition.

PV modules produce direct current (DC) which is suitable for directly charging batteries or powering a small number of special products. However, most appliances run on alternating current (AC). Consequently, an inverter must be used to convert the DC into AC. Inverters are widely used for many industrial applications. They are fabricated in large quantities as uninterruptible power supplies (UPS), to convert the DC electricity stored in batteries into AC electricity in the case of grid failure. They are used in hospitals and other installations where electricity failure is not tolerable. Small UPSs are often used in computers that must operate continuously. The PV inverter has an additional and important role: to vary the electrical operating point of the PV array to maintain its output at the maximum value, that is, the variable bias point at which the PV array produces highest power extraction. Changes of temperature and insolation change the voltage where maximum power extraction occurs. The electronics of the inverter typically include maximum power tracking. The inverters used in photovoltaics and the rest of the power conditioning electronics are explained in Chapter 19. Inverters have often been the source of poor reliability in early systems. Feedback to manufacturers and more robust components has greatly reduced these problems.

Because of the cost, the electronics for power conditioning is sometimes considered as a serious hindrance in the development of photovoltaics. However, we think the appearance of a significant market will reduce costs to reasonable limits. One fresh approach is to have a small inverter on the back of every module instead of a centralized inverter for the entire system. This modular approach has many advantages and is being put into production in USA [73] and Germany [74], but at present it is more expensive and will be so unless mass production reduces costs with respect to the theoretically cheaper bigger inverters.

The system-mounting structure is also important, in particular, in concentrating systems. In fact, this is the second most important cost element in concentrating PV systems, after the modules. In contrast, the power conditioning cost is comparable to many other small costs associated with the plant construction. This can be seen in Figure 1.14, where we present the breakdown of costs for a TFSC ($CuInSe_2$, an ancestor of today's $Cu(InGa)Se_2$) flat module central plant and a concentrating central plant. Both sets of calculations are based on the same criteria for the two technologies involved (but based on realistic but futuristic assumptions) and presented in Chapter 21.

The plant cost is about twice the module cost: more for concentrators, less for "flat-plate" modules. Notice, that the cost of land is absolutely negligible land (provided the plant is built where land prices are low). It has to be stressed again that modules at the costs in the figure are not yet achievable.

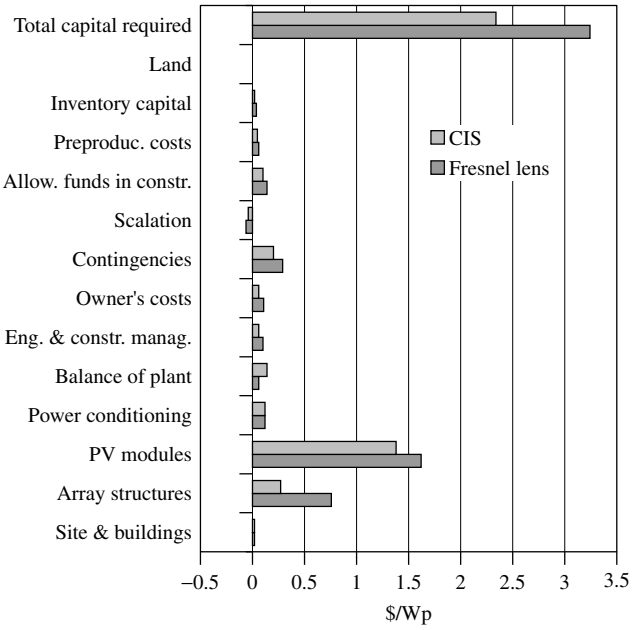

Figure 1.14 Calculated breakdown of costs of the construction of a PV central plant based on two anticipated technologies. Above, CIS flat module cells; below, Fresnel lens concentrator with Si cells operating at 500 suns. (Data from Whisnant *et al*. in Chapter 21)

We present in Figure 1.15 a calculation of costs of different types of modules in an advanced manufacturing process calculated with the same procedure. Again, the origin of this is Chapter 21, devoted to cost calculations. Although cost calculations for the $Cu(InGa)Se_2$ technology is not available, their costs are not expected to be too different to those of a-Si. Indeed, the cost model in Chapter 21 includes many more parameters and assumptions and the results depend on such choices. Nevertheless, according to the model, the common c-Si Cz module (with efficiency of about 14 to 15%) is clearly more expensive than any one of the other options (provided they have a minimal efficiency of 5 to 7%). Dendritic web technology refers to one form of Si ribbon technology that is starting to find a place in the market.

Using again the cost model in Chapter 21 we can calculate the cost of the electricity generated. Table 1.4 shows the difference of electric output of the two equally rated plants.[2] Obviously, the yearly efficiency (referred to as the *module aperture area*) is different. Furthermore, they both present different capacity factors as defined by the ratio of the produced energy (in kWh or MWh) to the rated power (in kWp or MWp) times the total number of hours in a year (365×24). To calculate the electricity cost (in \$/kWh), one term is the financial cost of all the expenditures and another much smaller one is the operation and maintenance costs (very small as stated at the beginning). The price per kWh must be compared to the typical average price of \$0.05/kWh for conventional

[2] Figure 1.15 and Table 1.4 present cost data scaled to 1985 or 1990 equivalent dollars, as does discussion and results in Chapter 21. Although quantitatively "out of date", they are still quite useful for relative comparison.

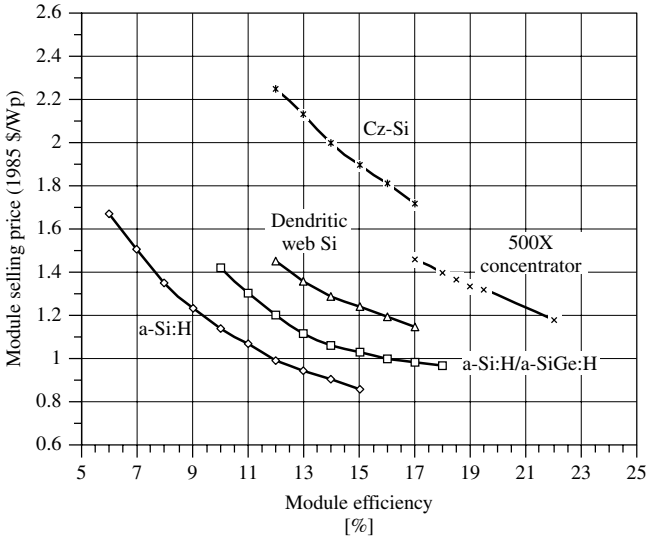

Figure 1.15 Effect of cell technology and efficiency on module price. (Source: Whisnant *et al.* in Chapter 21)

Table 1.4 Annual performance and energy cost summary for central station plants. Calculations for constant 1990$, for a 50 Mw_p plant in Central California, USA. Source Whisnant *et al.*, Chapter 21

	Fresnel lens concentrator	CIS Flat-plate
Energy output (MWh)	140 100	112 000
Capacity factor	32.0%	25.8%
Annual energy efficiency	18.8%	9.9%
Annual expenses (10^6)		
Capital charge	16.69	11.95
Operation & maintenance expense	0.61	0.18
Total	17.30	12.13
30-YR Levelized energy cost ($/kWh)		
Capital charge	0.119	0.106
Operation & maintenance costs	0.004	0.002
Total ($/kWh)	0.123	0.106

electricity. Photovoltaics is more than twice as expensive. However, this cost can be attractive for a part of the electricity generated by a utility, such as when it meets peak power demand.

For the end-user, the cost of the conventional electricity can be very similar to the one in the table. The cost of installing a PV grid-connected system in a house or building is not much more expensive than the centralized power plant presented in the table but the marketing cost of this distributed residential product will increase the final installation cost. It is to be stressed, that the costs used here are merely an indication

of the relative significance of various factors. These assumptions and model parameters may not apply to some immature or as-yet undeveloped technologies. Yet, these exercises can be useful to decision makers, especially if complemented by sensitivity studies (as in Chapter 21).

As a final comment, the costs presented in this section are final costs calculated by a detailed account of all the elements utilized in a plant or module and an estimation of the performances achieved. In contrast, the costs in Section 1.5 are based on fundamental economic laws that are found empirically to occur regardless of technological details, yielding costs as a function of the time. Thus, the costs, as calculated in the present section, may be considered as a point of that curve, to occur somewhere in the future.

Of course, all components in the system have some parasitic power loss. Yearly average AC efficiencies of 10% are common in a well-managed grid-connected system with modules starting at 14%. Much of this loss can be attributed to temperature: cells operate at 20 to 30°C over the ambient which reduces their efficiency and output since efficiency decreases with temperature (except for a-Si). Additionally, 8 to 10% relative losses are expected for the DC–AC conversion in the inverter. Round trip battery losses (charge–discharge) in stand-alone applications can be an additional relative 10 to 20%.

1.12 FUTURE OF EMERGING PV TECHNOLOGIES

The solar resource is huge although its energy density is rather low. However, it is not so low as to lose any hope of massive utilization but it is not high enough to make it easy.

Obviously, the proper strategy for recovering a dispersed resource is to do it with high efficiency at a low cost per area. But the standard PV-effect, as described in this chapter, only delivers to the external circuit with high efficiency those charge carriers generated by the few photons with energy close to the band gap. The excess energy of photons whose energy is greater than the band gap is typically wasted as heat. Even worse, all of the energy of the photons whose energy is below the band gap is wasted since they are not absorbed and therefore generate no charge carriers.

Thus, as described in detail in Chapter 4, the maximum efficiency that can be obtained under the best conditions from a single junction solar cell is in the range of 40%. The best efficiency so far obtained for single-junction solar cells is 27.6%, with GaAs research-type cells [75] under concentrated sunlight of 255 suns, that is, of 255 times the unconcentrated standard power density (i.e. at 255 kW/m^2). Typical commercial silicon cell efficiency is ~15% measured at standard conditions (input optical power density of 1 kW/m^2, 25°C and standard terrestrial solar spectrum).

One way of extracting more power from the sun is to use stacks of cells of semiconductors having different band gaps. Higher band gap semiconductors are located on top of the stack allowing photons of energy less than their band gap to pass through, where they can be absorbed by inner cells of lower band gap. The limit efficiency of these stacks, as presented in Chapter 4, with infinite number of cells of different band gap is 86%, as compared with the 40% of the single band gap cells. Efficiencies up to 32% (under standard unconcentrated terrestrial solar spectrum) have been achieved for a monolithic three band gap stacked cells of GaInP/GaAs/Ge [76].

The interest in multijunction cells has been reawakened by the requirements of space cells, where price is less relevant than the performance in many cases (Chapter 10). However, they can be used in terrestrial applications provided they are operating at very high concentration. There is a trend to develop cells operating at 1000 suns. Efficiencies up to 26% with a single band gap GaAs solar cell [77] and of over 29% with a double band gap GaInP/GaAs cells [78] have been achieved (Chapter 9). Also, the development of low-cost concentrators able to operate at 1000 suns is a subject of current research [79]. The prospects are very promising because such technologies predict in the long-term to produce electricity competitive with conventional sources. A cost estimate is presented in Table 1.5. In the 1-J no learning case, the costs are similar to those in Table 1.4. However, in the learning case the costs are, in extremely good locations (EGL), very competitive with conventional electricity, provided that we achieve very high efficiencies. In this calculation, the experience factor for the cells is the same as in microelectronics; for the rest of the elements the learning curve is same as the present one for modules [80].

The role of the experience factor has been stressed when describing Figures 1.6 and 1.7. Conventional cells have a relatively low experience factor, we think, because they are limited in the maximum efficiency they can reach. Multijunction cells, in contrast, have a much higher efficiency limit and therefore they can progress in efficiency for a longer time. This is one reason to attribute to them a faster experience factor.

Multijunction cells are also crucial to the success of the thin-film photovoltaics. In the a-Si thin-film PV technology, the highest cell and module efficiencies being reported for the past decade are for triple junctions as described in Chapter 12. The use of multijunction cells in thin films might lead to a faster learning curve and hence reduced costs. The band gap of various polycrystalline alloys of $Cu(InGa)Se_2$, $Cu(InAl)Se_2$, Cu(InGa)(SeS), or CdZnTe can be varied with alloying. The theoretical efficiency of a tandem device with a 1.6 to 1.8 eV band gap top cell and a 1.0 to 1.2 eV band gap bottom cell exceeds 30%. In all cases, the top cell must provide the majority of the power.

Table 1.5 Costs for very high-efficiency 1000 suns-concentrating systems [80] for one junction (1-J) and four junctions (4-J) cells. NDI stands for Normal Direct Irradiation. EGL stands for extremely good location with NDI = 2700 $W \cdot m^{-2} \cdot year^{-1}$. "No learning" means with present costs (2002) while "learning" means they are reduced by a learning curve with experience factor of 0.32

Cost element	1-J, no learning	4-J, learning
Cells ($ per cm^2 cell area)	13.4	4.43
Module ($ per aperture area)	265	113
Cell efficiency (%)	23.1	45
Module efficiency (%)	19.0	37.1
Plant price ($ per m^2 aperture area)	526	271
Madrid NDI ($W \cdot m^{-2} \cdot year^{-1}$)	1826	1826
Performance ratio	0.606	0.606
Electricity costs in Madrid ($ per kWh)	0.186	0.050
Electricity costs in EGL ($ per kWh)	0.131	0.035

Yet, in all these alloy systems, material quality and device performance degrades substantially for band gaps exceeding 1.4 to 1.6 eV, depending on the materials (see Chapter 13). A very productive area for research will be to either improve these materials when they are produced with high band gaps or to develop new alloys. Any multijunction process must be sequentially compatible from beginning to end.

Besides the multijunction effort, other concepts are in place for attempting a better utilization of the solar spectrum, such as the Intermediate Band (IB) concept [81], which is described further in Chapter 4. A band, with electron states in the center of the band gap, would permit the passage of electrons from the valence band to the conduction band by means of two low-energy photons, one pumping electrons from the valence to the intermediate band and the other pumping the electron from this band to the conduction band. This concept presents a potential behavior which is somewhat better than the multijunction cell stack with two semiconductors. Nanotechnology is a means of producing this intermediate band [82], and the basic effect sketched above seems to have been proved already by using quantum dots [83]. Quantum dots are droplets of one material in a host of another material of higher band gap. The droplets are very small and exhibit quantum effects among which is the appearance of intermediate bands or levels. Alloys might also be found with intermediate band [84], but no practical realization of this concept has been shown so far. Other new type devices, although not easy to realize today, are also envisioned. The theoretical basis of all these new devices can be found in Chapter 4.

Finally, solar cells have been constructed which do not operate on the photovoltaic effect but on charge transfer between molecular orbitals, as in photosynthesis. Their potential for efficient absorption of the spectrum depends on "tuning" the chemistry of organic dyes, as described in Chapter 15. Presently the subject of much research, dye-sensitized solar cells have achieved $>10\%$ efficiency but have many challenges regarding stability and manufacturability.

1.13 CONCLUSIONS

Photovoltaics constitutes a new form of producing electric energy that is environmentally clean and very modular. In stand-alone installations, it must use storage or another type of generator to provide electricity when the sun is not shining. In grid-connected installations storage is not necessary: in the absence of sunlight, electricity is provided from other (conventional) sources.

PV electricity is highly appreciated by the public. It is unique for many applications of high social value such as providing electricity to people who lack it in remote areas. Often, international donor agencies are providing the funding, as many of the users are very poor. Photovoltaics is very suitable as the power supply for remote communication equipment. Its use is increasing rapidly to produce electricity in grid-connected houses and buildings in industrialized countries, despite a 5 to 10 times higher cost than conventional electricity. Often, publicly funded programs are required to enable photovoltaics to compete by partially offsetting its higher costs.

Largely, because of grid-connected PV applications such as homes and businesses, the expansion of the PV market has been very rapid in the last years of the twentieth

century and it is expected to continue during the next few years of the twenty-first century. Then, the growth will probably continue at a slower pace unless new technological advances are developed and commercialized. In that case, growth could accelerate.

Photovoltaics is poised to become a large global high-tech industry, manufacturing and selling modules in nearly every country. Governments and entrepreneurs should be aware of this. Public R&D support has always been generous. It must continue to be so for those countries that want to maintain leadership in this technology. Partial subsidization of PV installations is permitting an unprecedented development of the PV industry and will also help the industry of the countries involved in this endeavor to take the lead.

Crystalline Si technology, both monocrystalline and multicrystalline is today clearly dominant, with about 90% of the market. It will remain dominant at least for the next ten years. The trend is towards the multicrystalline option. Si is one of the most abundant elements in the Earth's crust but the purified Si used in today's solar cells is obtained primarily as off-grade poly-Si and scrap wafers from the microelectronic industry. Soon it will not be enough for the growing PV industry. Thus, some concerns exist regarding a shortage of the purified silicon for the PV industry. However, it is doubtful that Si technology will be able to reach competition with conventional electricity. Consequently, low-cost alternatives and high-efficiency novel concepts, many already in development, are needed.

Thin-film technology is one of the candidates to take over from Si technology in the long-term. There are many technological options regarding thin-film materials and methods of deposition but their primary claim to the throne currently occupied by Si is that they can be ultimately produced at much lower cost.

Concentration of sunlight is another candidate for mass penetration of photovoltaics, although it will not be easily accepted for the grid-connected houses, one of the most promising applications today. Concentrators will probably find incipient niche markets in big stand-alone applications or as small, central-power plants during the present decade.

Finally, new materials and device designs based on III-V semiconductor alloys, such as GaInP allowing more efficient use of the solar spectrum are now being developed for space applications. With the use of concentrators, they may be of interest for terrestrial applications, with the potential of reaching competitive costs with conventional electricity. Other options, such as quantum dots and dye-sensitized solar cells, are still in the initial research phase. They must compete not only with the ubiquitous Si but also with the other options, mentioned above for funding for further development.

Thus, photovoltaics possesses a panoply of novel technologies that almost ensures that alternatives will be available when the current Si wafer technology cannot reach prices low enough to compete with conventional electricity. If this happens, a strong industry and infrastructure – first developed for the Si technology – will be able to seamlessly take this new PV technology and apply it worldwide. In any case, the present "subsidies" to research or application must be considered as public investment in a policy with strong public support and long-term human benefits.

The widespread contribution of PV electricity in electric grids will require a new type of grid management that can accept small generators as well as small consumers. On

the other hand, hybrid forms of electricity generation, including photovoltaics, will play an important role in the future development of stand-alone applications and minigrids. The general cost reduction will make photovoltaics available to more and more people in developing countries helping their development with little degradation of air quality associated with fossil-fuel generators.

In summary, it is very likely that photovoltaics will become in the next half century an important source of world electricity. Public support and global environmental concerns will keep photovoltaics viable, visible, and vigorous both in new technical developments and user applications. Nations which encourage photovoltaics will be leaders in this shining new technology, leading the way to a cleaner, more equitable twenty-first century, while those that ignore or suppress photovoltaics will be left behind in the green, economic energy revolution.

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3

The Physics of the Solar Cell

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3.1 INTRODUCTION

Semiconductor solar cells are fundamentally quite simple devices. Semiconductors have the capacity to absorb light and to deliver a portion of the energy of the absorbed photons to carriers of electrical current – electrons and holes. A semiconductor diode separates and collects the carriers and conducts the generated electrical current preferentially in a specific direction. Thus, a solar cell is simply a semiconductor diode that has been carefully designed and constructed to efficiently absorb and convert light energy from the sun into electrical energy. A simple conventional solar cell structure is depicted in Figure 3.1. Sunlight is incident from the top on the front of the solar cell. A metallic grid forms one of the electrical contacts of the diode and allows light to fall on the semiconductor between the grid lines and thus be absorbed and converted into electrical energy. An antireflective layer between the grid lines increases the amount of light transmitted to the semiconductor. The semiconductor diode is fashioned when an n-type semiconductor and a p-type semiconductor are brought together to form a metallurgical junction. This is typically achieved through diffusion or implantation of specific impurities (dopants) or via a deposition process. The diode's other electrical contact is formed by a metallic layer on the back of the solar cell.

All electromagnetic radiation, including sunlight, is composed of particles called photons, which carry specific amounts of energy determined by the spectral properties of their source. Photons also exhibit a wavelike character with the wavelength, λ, being related to the photon energy, E_λ, by

$$E_\lambda = \frac{hc}{\lambda} \tag{3.1}$$

where $\hbar$ is Plank's constant and c is the speed of light. Only photons with sufficient energy to create an electron–hole pair, that is, those with energy greater than the semiconductor

Handbook of Photovoltaic Science and Engineering. Edited by A. Luque and S. Hegedus
 ISBN: 0-471-49196-9

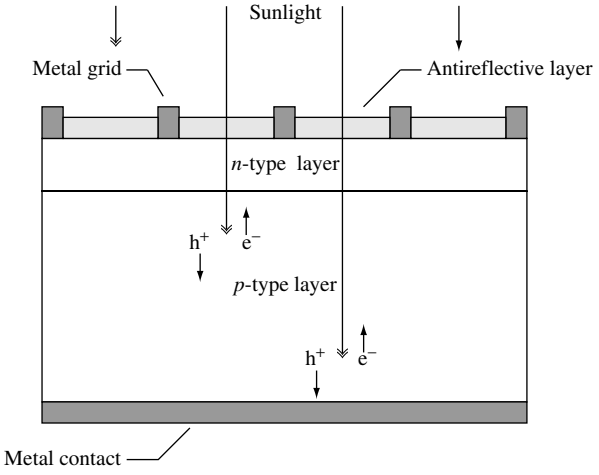

Figure 3.1 A schematic of a simple conventional solar cell. Creation of electron–hole pairs, e^- and h^+, respectively, is depicted

band gap (E_G), will contribute to the energy conversion process. Thus, the spectral nature of sunlight is an important consideration in the design of efficient solar cells.

The sun has a surface temperature of 5762 K and its radiation spectrum can be approximated by a black-body radiator at that temperature. Emission of radiation from the sun, as with all black-body radiators, is isotropic. However, the Earth's great distance from the sun (approximately 93 million miles) means that only those photons emitted directly in the direction of the Earth contribute to the solar spectrum as observed from Earth. Therefore, for practical purposes, the light falling on the Earth can be thought of as parallel streams of photons. Just above the Earth's atmosphere, the radiation intensity, or Solar Constant, is about 1.353 kW/m^2 [1] and the spectral distribution is referred to as an *air mass zero* (AM0) radiation spectrum. The Air Mass is a measure of how absorption in the atmosphere affects the spectral content and intensity of the solar radiation reaching the Earth's surface. The Air Mass number is given by

$$\text{Air Mass} = \frac{1}{\cos\theta} \tag{3.2}$$

where θ is the angle of incidence ($\theta = 0$ when the sun is directly overhead). The Air Mass number is always greater than or equal to one at the Earth's surface. An easy way to estimate the Air Mass has been given by Green [1] as

$$\text{Air Mass} = \sqrt{1 + (S/H)^2} \tag{3.3}$$

where S is the length of a shadow cast by an object of height H. A widely used standard for comparing solar cell performance is the AM1.5 spectrum normalized to a total power density of 1 kW/m^2. The spectral content of sunlight at the Earth's surface also has a diffuse (indirect) component owing to scattering and reflection in the atmosphere and surrounding landscape and can account for up to 20% of the light incident on a solar

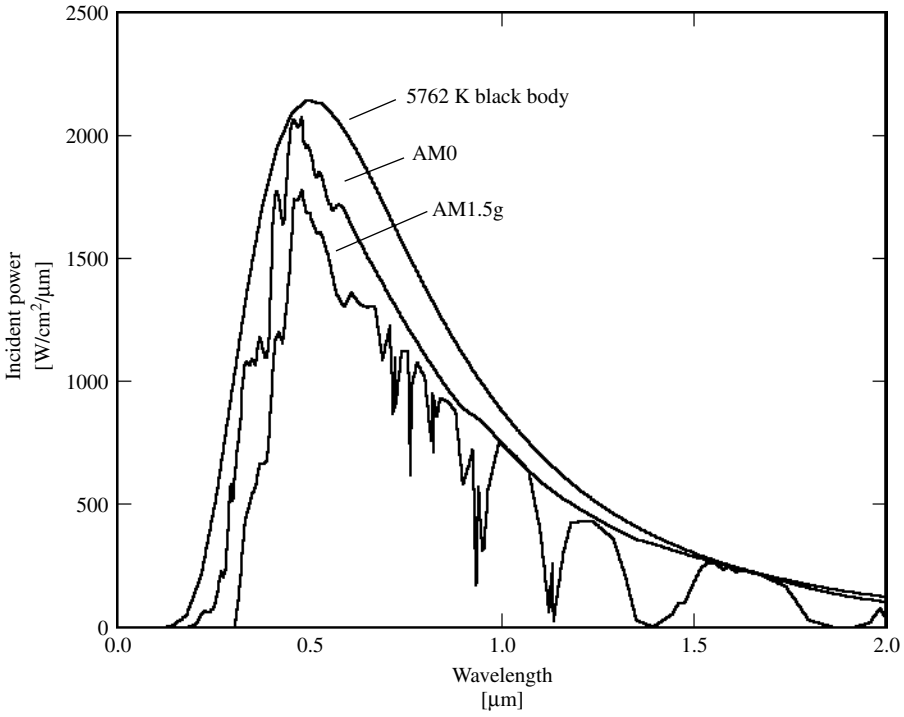

Figure 3.2 The radiation spectrum for a black body at 5762 K, an AM0 spectrum, and an AM1.5 global spectrum

cell. The Air Mass number is therefore further defined by whether or not the measured spectrum includes the diffuse component. An AM1.5g (global) spectrum includes the diffuse component, while an AM1.5d (direct) does not. Black body ($T = 5762$ K), AM0, and AM1.5g radiation spectrums are shown in Figure 3.2. The Air Mass and solar radiation are described in more detail in Chapters 16 and 20.

The physical principles underlying the operation of solar cells are the subject of this chapter. First, a brief review of the fundamental properties of semiconductors is given that includes an overview of semiconductor band structure and carrier generation, recombination, and transport. Next, the electrostatic properties of the *pn*-junction diode are reviewed, followed by a description of the basic operating characteristics of the solar cell, including the derivation (based on the solution of the minority-carrier diffusion equation) of an expression for the current–voltage characteristic of an idealized solar cell. This is used to define the basic solar cell figures of merit, namely, the open-circuit voltage, V_{OC}; the short-circuit current, I_{SC}; the fill factor, FF; the conversion efficiency, η; and the collection efficiency, η_C. Much of the discussion here centers on how carrier recombination is the primary factor controlling solar cell performance. Finally, some additional topics relevant to solar cell operation, design, and analysis are presented. These include the relationship between band gap and efficiency, the solar cell spectral response, parasitic resistive effects, temperature effects, a brief introduction to some modern cell design concepts, and a short overview of detailed numerical modeling of solar cells.

3.2 FUNDAMENTAL PROPERTIES OF SEMICONDUCTORS

An understanding of the operation of semiconductor solar cells requires familiarity with some basic concepts of solid-state physics. Here, an introduction is provided to the essential concepts needed to examine the physics of solar cells. More complete and rigorous treatments are available from a number of sources [2–6].

Solar cells can be fabricated from a number of semiconductor materials, most commonly silicon (Si) – crystalline, polycrystalline, and amorphous. Solar cells are also fabricated from GaAs, GaInP, Cu(InGa)Se_2, and CdTe, to name but a few. Solar cell materials are chosen largely on the basis of how well their absorption characteristics match the solar spectrum and their cost of fabrication. Silicon has been a common choice due to the fact that its absorption characteristics are a fairly good match to the solar spectrum, and silicon fabrication technology is well developed as a result of its pervasiveness in the semiconductor electronics industry.

3.2.1 Crystal Structure

Electronic grade semiconductors are very pure crystalline materials. Their crystalline nature means that their atoms are aligned in a regular periodic array. This periodicity, coupled with the atomic properties of the component elements, is what gives semiconductors their very useful electronic properties. An abbreviated periodic table of the elements is given in Table 3.1.

Note that silicon is in column IV, meaning that it has four valence electrons, that is, four electrons that can be shared with neighboring atoms to form covalent bonds with those neighbors. In crystalline silicon, the atoms are arranged in a *diamond lattice* (carbon is also a column IV element) with tetrahedral bonding – four bonds from each atom where the angle between any two bonds is 109.5°. Perhaps surprisingly, this arrangement can be represented by two interpenetrating face-centered cubic (*fcc*) unit cells where the second *fcc* unit cell is shifted one-fourth of the distance along the body diagonal of the first *fcc* unit cell. The lattice constant, ℓ, is the length of the edges of the cubic unit cell. The entire lattice can be constructed by stacking these unit cells. A similar arrangement, the *zincblende* lattice, occurs in many binary III–V and II–VI semiconductors such as GaAs (a III–V compound) and CdTe (a II–VI compound). For example, in GaAs, one interpenetrating *fcc* unit cell is composed entirely of Ga atoms and the other entirely of As atoms. Note that the average valency is four for each compound, so that there are four bonds to and from each atom with each covalent bond involving two valence electrons. Some properties of semiconductors are dependent on the orientation of the crystal

Table 3.1 Abbreviated periodic table of the elements

I	II	III	IV	V	VI
		B	C	N	O
		Al	Si	P	S
Cu	Zn	Ga	Ge	As	Se
Ag	Cd	In	Sn	Sb	Te

lattice, and casting the crystal structure in terms of a cubic unit cell makes identifying the orientation easier using Miller indices.

3.2.2 Energy Band Structure

Of more consequence to the physics of solar cells, however, is how the periodic crystalline structure of the semiconductor establishes its electronic properties. An electron moving in a semiconductor material is analogous to a particle confined to a three-dimensional box that has a complex interior structure due primarily to the potential fields surrounding the component atom's nucleus and tightly bound core electrons. The dynamic behavior of the electron can be established from the electron wave function, ψ, which is obtained by solving the time-independent Schrödinger equation

$$\nabla^2\psi + \frac{2m}{\hbar^2}[E - U(\vec{r})]\psi = 0 \tag{3.4}$$

where m is electron mass, h is the reduced Planck constant, E is the energy of the electron, and $U(\vec{r})$ is the periodic potential energy inside the semiconductor. Solving this quantum-mechanical equation is beyond the scope of this work, but suffice it to say that the solution defines the band structure (the allowed electron energies and the relationship between the electron's energy and momentum) of the semiconductor and, amazingly, tells us that the quantum mechanically computed motion of the electron in the crystal is, to a good approximation, like that of an electron in free space if its mass, m, is replaced by an effective mass, m^*, in Newton's law of motion from classical mechanics

$$F = m^* a \tag{3.5}$$

where F is the applied force and a is the acceleration of the electron. A simplified energy band structure is illustrated in Figure 3.3. The allowed electron energies are plotted against the crystal momentum, $p = \hbar k$, where k is the wave vector (represented here as a scalar for simplicity) corresponding to the wave function solutions of the Schrödinger equation. Only the energy bands of immediate interest are shown – energy bands below the valence band are presumed to be fully occupied by electrons and those above the conduction band are presumed to be empty. The electron effective mass is thus defined as

$$m^* \equiv \left[\frac{\mathrm{d}^2E}{\mathrm{d}p^2}\right]^{-1} = \left[\frac{1}{\hbar^2}\frac{\mathrm{d}^2E}{\mathrm{d}k^2}\right]^{-1} \tag{3.6}$$

Notice that the effective mass is not constant within each band. In addition, near the top of the valence band, the effective mass is actually negative. Electrons (*) fill the states from bottom to top and the states near the top of the valence band are empty (o) due to some electrons being thermally excited into the conduction band. These empty states can conveniently be regarded as positively charged carriers of current called *holes* with a positive effective mass. It is conceptually much easier to deal with a relatively few number of holes that have a positive effective mass since they will behave like classical positively charged particles. The top of the valence band and the bottom of the conduction band are approximately parabolic in shape and therefore the electron effective mass (m_n^*)

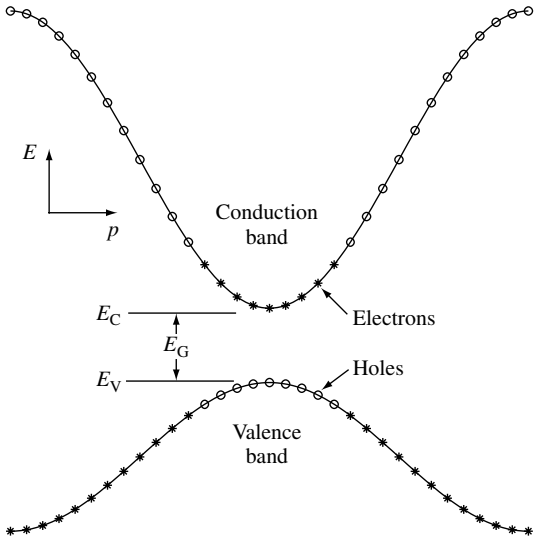

Figure 3.3 A simplified energy band diagram at $T > 0$ K for a direct band gap (E_G) semiconductor. Electrons near the maxima in valence band have been thermally excited to the empty states near the conduction-band minima, leaving behind holes. The excited electrons and remaining holes are the negative and positive mobile charges that give semiconductors their unique transport properties

near the bottom of the conduction band is a constant, as is the hole effective mass (m_p^*) near the top of the valence band. This is a very practical assumption that greatly simplifies the analysis of semiconductors.

When the minimum of the conduction band occurs at the same value of the crystal momentum as the maximum of the valence band, as it does in Figure 3.3, the semiconductor is a *direct band gap* semiconductor. When they do not align, the semiconductor is said to be an *indirect band gap* semiconductor. This is especially important when the absorption of light by a semiconductor is considered later in this chapter.

Even amorphous materials exhibit a similar band structure. Over short distances, the atoms are arranged in a periodic manner and an electron wave function can be defined. The wave functions from these small regions overlap in such a way that a *mobility gap* can be defined with electrons above the mobility gap defining the conduction band and holes below the gap defining the valence band. Unlike crystalline materials, however, there are a large number of localized energy states within the mobility gap (band tails and dangling bonds) that complicate the analysis of devices fabricated from these materials. Amorphous silicon (a-Si) solar cells are discussed in Chapter 12.

3.2.3 Conduction-band and Valence-band Densities of State

Now that the dynamics of the electron motion in a semiconductor has been approximated by a negatively charged particle with mass m_n^* in the conduction band and by a positively charged particle with mass m_p^* in the valence band, it is possible to calculate the density

of states in each band. This again involves solving the time-independent Schrödinger equation for the wave function of a particle in a box, but in this case the box is empty. All the complexities of the periodic potentials of the component atoms have been incorporated into the effective mass. The density of states in the conduction band is given by

$$g_{\mathrm{C}}(E) = \frac{m_n^* \sqrt{2m_n^*(E - E_{\mathrm{C}})}}{\pi^2 \hbar^3} \mathrm{cm}^{-3}\,\mathrm{eV}^{-1} \tag{3.7}$$

while the density of states in the valence band is given by

$$g_{\mathrm{V}}(E) = \frac{m_p^* \sqrt{2m_p^*(E_{\mathrm{V}} - E)}}{\pi^2 \hbar^3} \mathrm{cm}^{-3}\,\mathrm{eV}^{-1} \tag{3.8}$$

3.2.4 Equilibrium Carrier Concentrations

When the semiconductor is in thermal equilibrium (i.e. at a constant temperature with no external injection or generation of carriers), the Fermi function determines the ratio of filled states to available states at each energy and is given by

$$f(E) = \frac{1}{1 + \mathrm{e}^{(E - E_{\mathrm{F}})/kT}} \tag{3.9}$$

where E_{F} is the Fermi energy, k is Boltzmann's constant, and T is the Kelvin temperature. As seen in Figure 3.4, the Fermi function is a strong function of temperature. At absolute zero, it is a step function and all the states below E_{F} are filled with electrons and all those above E_{F} are completely empty. As the temperature increases, thermal excitation will leave some states below E_{F} empty, and the corresponding number of states above E_{F} will be filled with the excited electrons.

The equilibrium electron and hole concentrations (#/cm^3) are therefore

$$n_o = \int_{E_{\mathrm{C}}}^{\infty} g_{\mathrm{C}}(E) f(E)\,\mathrm{d}E = \frac{2N_{\mathrm{C}}}{\sqrt{\pi}} F_{1/2}((E_{\mathrm{F}} - E_{\mathrm{C}})/kT) \tag{3.10}$$

$$p_o = \int_{-\infty}^{E_{\mathrm{V}}} g_{\mathrm{V}}(E)[1 - f(E)]\,\mathrm{d}E = \frac{2N_{\mathrm{V}}}{\sqrt{\pi}} F_{1/2}((E_{\mathrm{V}} - E_{\mathrm{F}})/kT) \tag{3.11}$$

where $F_{1/2}(\xi)$ is the Fermi–Dirac integral of order 1/2,

$$F_{1/2}(\xi) = \int_0^{\infty} \frac{\sqrt{\xi'}\,\mathrm{d}\xi'}{1 + \mathrm{e}^{\xi' - \xi}} \tag{3.12}$$

The conduction-band and valence-band effective densities of state (#/cm^3), N_{C} and N_{V}, respectively, are given by

$$N_{\mathrm{C}} = 2\left(\frac{2\pi m_n^* kT}{h^2}\right)^{3/2} \tag{3.13}$$

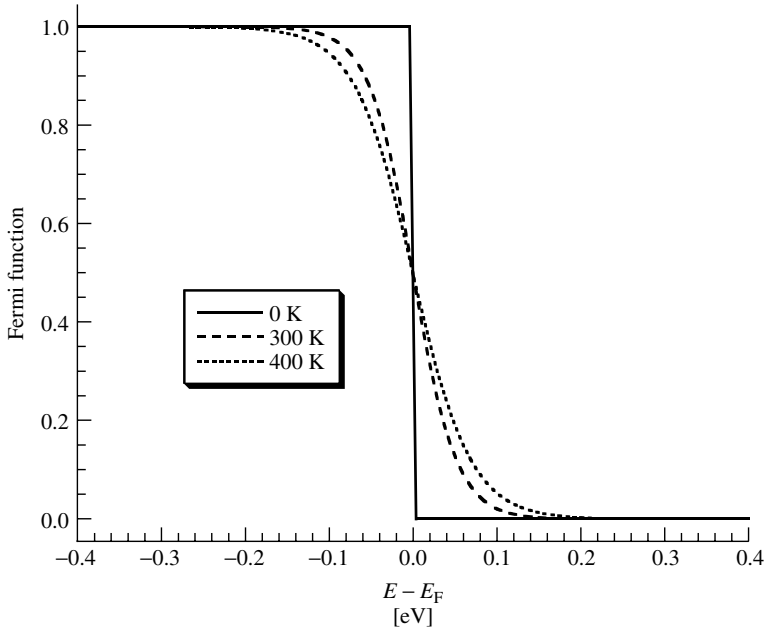

Figure 3.4 The Fermi function at various temperatures

and

$$N_{\mathrm{V}} = 2\left(\frac{2\pi m_p^* kT}{h^2}\right)^{3/2}. \tag{3.14}$$

When the Fermi energy, E_{F}, is sufficiently far ($>3\ kT$) from either bandedge, the carrier concentrations can be approximated (to within 2%) as [7]

$$n_o = N_{\mathrm{C}} \mathrm{e}^{(E_{\mathrm{F}}-E_{\mathrm{C}})/kT} \tag{3.15}$$

and

$$p_o = N_{\mathrm{V}} \mathrm{e}^{(E_{\mathrm{V}}-E_{\mathrm{F}})/kT} \tag{3.16}$$

and the semiconductor is said to be *nondegenerate*. In nondegenerate semiconductors, the product of the equilibrium electron and hole concentrations is independent of the location of the Fermi energy and is just

$$p_o n_o = n_{\mathrm{i}}^2 = N_{\mathrm{C}} N_{\mathrm{V}} \mathrm{e}^{(E_{\mathrm{V}}-E_{\mathrm{C}})/kT} = N_{\mathrm{C}} N_{\mathrm{V}} \mathrm{e}^{-E_{\mathrm{G}}/kT}. \tag{3.17}$$

In an undoped (intrinsic) semiconductor in thermal equilibrium, the number of electrons in the conduction band and the number of holes in the valence band are equal; $n_o = p_o = n_{\mathrm{i}}$, where n_{i} is the intrinsic carrier concentration. The intrinsic carrier concentration can be computed from (3.17), giving

$$n_{\mathrm{i}} = \sqrt{N_{\mathrm{C}} N_{\mathrm{V}}} \mathrm{e}^{(E_{\mathrm{V}}-E_{\mathrm{C}})/2kT} = \sqrt{N_{\mathrm{C}} N_{\mathrm{V}}} \mathrm{e}^{-E_{\mathrm{G}}/2kT}. \tag{3.18}$$

The Fermi energy in an intrinsic semiconductor, $E_i = E_F$, is given by

$$E_i = \frac{E_V + E_C}{2} + \frac{kT}{2} \ln\left(\frac{N_V}{N_C}\right) \tag{3.19}$$

which is typically very close to the middle of the band gap. The intrinsic carrier concentration is typically very small compared to the densities of states and typical doping densities ($n_i \approx 10^{10}$ cm^{-3} in Si) and intrinsic semiconductors behave very much like insulators; that is, they are not very useful as conductors of electricity.

The number of electrons and holes in their respective bands, and hence the conductivity of the semiconductor, can be controlled through the introduction of specific impurities, or dopants, called *donors* and *acceptors*. For example, when semiconductor silicon is doped with phosphorous, one electron is donated to the conduction band for each atom of phosphorous introduced. From Table 3.1, it can be seen that phosphorous is in column V of the periodic table of elements and thus has five valence electrons. Four of these are used to satisfy the four covalent bonds of the silicon lattice and the fifth is available to fill an empty state in the conduction band. If silicon is doped with boron (valency of three, since it is in column III), each boron atom accepts an electron from the valence band, leaving behind a hole. All impurities introduce additional localized electronic states into the band structure, often within the forbidden band between E_C and E_V, as illustrated in Figure 3.5. If the energy of the state, E_D, introduced by a donor atom is sufficiently close to the conduction bandedge (within a few kT), there will be sufficient thermal energy to allow the extra electron to occupy a state in the conduction band. The donor state will then be positively charged (ionized) and must be considered when analyzing the electrostatics of the situation. Similarly, an acceptor atom will introduce a negatively charged (ionized) state at energy E_A. The controlled introduction of donor and acceptor impurities into a semiconductor allows the creation of the n-type (electrons are the primary source of electrical conduction) and p-type (holes are the primary source of electrical conduction) semiconductors, respectively. This is the basis for the construction of all semiconductor devices, including solar cells. The number of ionized donors and acceptors are given by [7]

$$N_D^+ = \frac{N_D}{1 + g_D e^{(E_F - E_D)/kT}} = \frac{N_D}{1 + e^{(E_F - E_D')/kT}} \tag{3.20}$$

and

$$N_A^- = \frac{N_A}{1 + g_A e^{(E_A - E_F)/kT}} = \frac{N_A}{1 + e^{(E_A' - E_F)/kT}} \tag{3.21}$$

where g_D and g_A are the donor and acceptor site degeneracy factors. Typically, $g_D = 2$ and $g_A = 4$. These factors are normally combined into the donor and the acceptor energies so that $E_D' = E_D - kT \ln g_D$ and $E_A' = E_A + kT \ln g_A$. Often, the donors and acceptors are assumed to be completely ionized so that $n_o \simeq N_D$ in n-type material and $p_o = N_A$ in p-type material. The Fermi energy can then be written as

$$E_F = E_i + kT \ln \frac{N_D}{n_i} \tag{3.22}$$

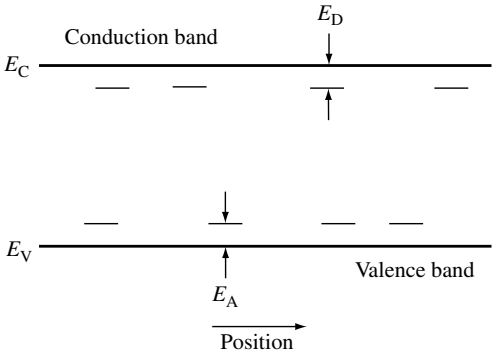

Figure 3.5 Donor and acceptor levels in a semiconductor. The nonuniform spatial distribution of these states reinforces the concept that these are localized states

in n-type material and as

$$E_F = E_i - kT \ln \frac{N_A}{n_i} \tag{3.23}$$

in p-type material.

When a very large concentration of dopants is introduced into the semiconductor, the dopants can no longer be thought of as a minor perturbation to the system. Their effect on the band structure must be considered. Typically, this so-called heavy doping effect manifests itself as a reduction in the band gap, E_G, and thus an increase in the intrinsic carrier concentration, as can be seen from equation (3.18). This band gap narrowing (BGN) [8] is detrimental to solar cell performance and solar cells are typically designed to avoid this effect, though it may be a factor in the heavily doped regions near the solar cell contacts.

3.2.5 Light Absorption

The creation of electron–hole pairs via the absorption of sunlight is fundamental to the operation of solar cells. The excitation of an electron directly from the valence band (which leaves a hole behind) to the conduction band is called *fundamental absorption*. Both the total energy and momentum of all particles involved in the absorption process must be conserved. Since the photon momentum, $p_\lambda = h/\lambda$, is very small compared to the range of the crystal momentum, $p = h/\ell$, the photon absorption process must, for practical purposes, conserve the momentum of the electron.[1] The absorption coefficient for a given photon energy, $h\nu$, is proportional to the probability, P_{12}, of the transition of an electron from the initial state E_1 to the final state E_2, the density of electrons in the initial state, $g_V(E_1)$, and the density of available final states, and is then summed over

[1] The wavelength of sunlight, λ, is on the order of a micron (10^{-4} cm), while the lattice constant is a few angstroms (10^{-8} cm). Thus, the crystal momentum is several orders of magnitude larger than the photon momentum.

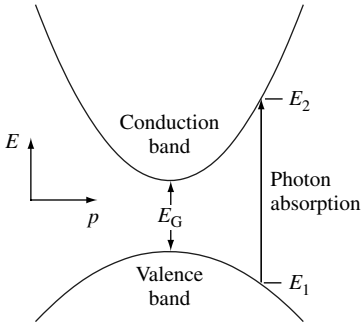

Figure 3.6 Photon absorption in a direct band gap semiconductor for an incident photon with energy $h\nu = E_2 - E_1 > E_G$

all possible transitions between states where $E_2 - E_1 = h\nu$ [9],

$$\alpha(h\nu) \propto \sum P_{12} g_V(E_1) g_C(E_2), \tag{3.24}$$

assuming that all the valence-band states are full and all the conduction-band states are empty. Absorption results in creation of an electron-hole pair since a free electron is excited to the conduction band leaving a free hole in the valence band.

In direct band gap semiconductors, such as GaAs, GaInP, CdTe, and Cu(InGa)Se_2, the basic photon absorption process is illustrated in Figure 3.6. Both energy and momentum must be conserved in the transition. Every initial electron state with energy E_1 and crystal momentum p_1 in the valence band is associated with a final state in the conduction band at energy E_2 and crystal momentum p_2. Since the electron momentum is conserved, the crystal momentum of the final state is the same as the initial state, $p_1 \approx p_2 = p$.

Conservation of energy dictates that the energy of the absorbed photon is

$$h\nu = E_2 - E_1 \tag{3.25}$$

Since we have assumed parabolic bands,

$$E_V - E_1 = \frac{p^2}{2m_p^*} \tag{3.26}$$

and

$$E_2 - E_C = \frac{p^2}{2m_n^*} \tag{3.27}$$

Combining equations (3.25), (3.26), and (3.27) yields

$$h\nu - E_G = \frac{p^2}{2}\left(\frac{1}{m_n^*} + \frac{1}{m_p^*}\right) \tag{3.28}$$

and the absorption coefficient for direct transitions is [9]

$$\alpha(h\nu) \approx A^*(h\nu - E_G)^{1/2}, \tag{3.29}$$

where A^* is a constant. In some semiconductor materials, quantum selection rules do not allow transitions at $p = 0$ but allow them for $p \neq 0$. In such cases [9]

$$\alpha(h\nu) \approx \frac{B^*}{h\nu}(h\nu - E_G)^{3/2}, \tag{3.30}$$

where B^* is a constant.

In indirect band gap semiconductors like Si and Ge, where the valence-band maximum occurs at a different crystal momentum than the conduction-band minimum, conservation of electron momentum necessitates that the photon absorption process involve an additional particle. Phonons, the particle representation of lattice vibrations in the semiconductor, are suited to this process because they are low-energy particles with relatively high momentum. This is illustrated in Figure 3.7. Notice that light absorption is facilitated by either phonon absorption or phonon emission. The absorption coefficient, when there is phonon absorption, is given by

$$\alpha_a(h\nu) = \frac{A(h\nu - E_G + E_{ph})^2}{e^{E_{ph}/kT} - 1} \tag{3.31}$$

and by

$$\alpha_e(h\nu) = \frac{A(h\nu - E_G - E_{ph})^2}{1 - e^{-E_{ph}/kT}} \tag{3.32}$$

when a phonon is emitted [9]. Because both processes are possible,

$$\alpha(h\nu) = \alpha_a(h\nu) + \alpha_e(h\nu). \tag{3.33}$$

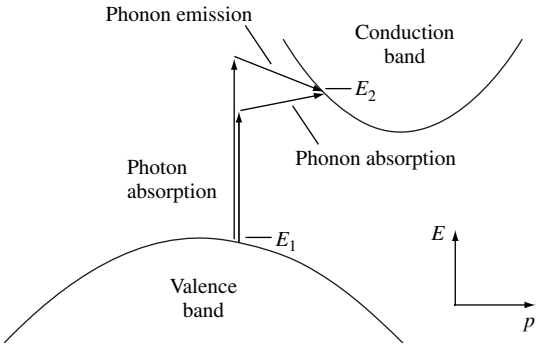

Figure 3.7 Photon absorption in an indirect band gap semiconductor for a photon with energy $h\nu < E_2 - E_1$ and a photon with energy $h\nu > E_2 - E_1$. Energy and momentum in each case are conserved by the absorption and emission of a phonon, respectively

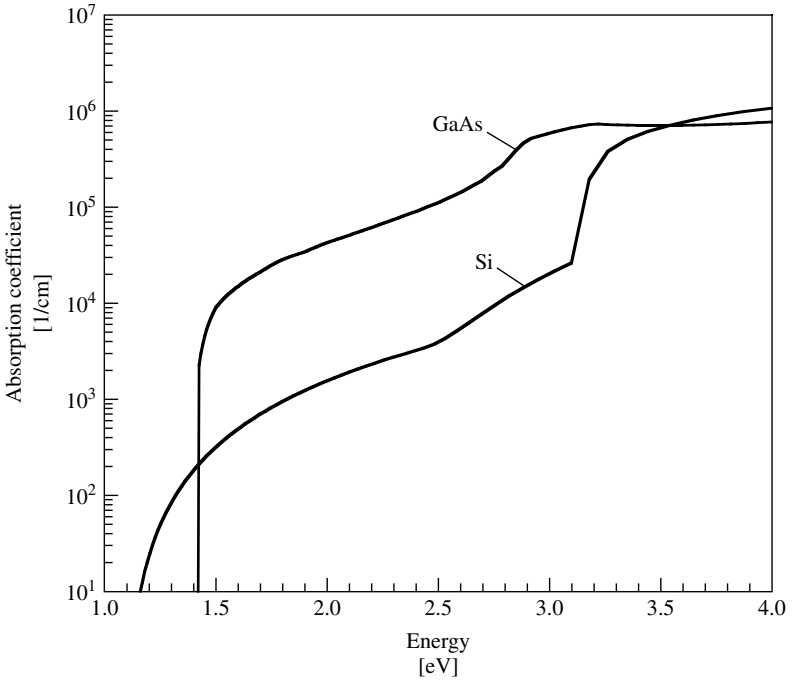

Figure 3.8 Absorption coefficient as a function of photon energy for Si (indirect band gap) and GaAs (direct band gap) at 300 K. Their band gaps are 1.12 and 1.4 eV, respectively

Since both a phonon and an electron are needed to make the indirect gap absorption process possible, the absorption coefficient depends not only on the density of full initial electron states and empty final electron states but also on the availability of phonons (both emitted and absorbed) with the required momentum. Thus, compared to direct transitions, the absorption coefficient for indirect transitions is relatively small. As a result, light penetrates more deeply into indirect band gap semiconductors than direct band gap semiconductors. This is illustrated in Figure 3.8 for Si, an indirect band gap semiconductor, and GaAs, a direct band gap semiconductor. Similar spectra are shown for other semiconductors elsewhere in this handbook.

In both direct band gap and indirect band gap materials, a number of photon absorption processes are involved, though the mechanisms described above are the dominant ones. A direct transition, without phonon assistance, is possible in indirect band gap materials if the photon energy is high enough (as seen in Figure 3.8 for Si at about 3.3 eV). Conversely, in direct band gap materials, phonon-assisted absorption is also a possibility. Other mechanisms may also play a role in defining the absorption process in semiconductors. These include absorption in the presence of an electric field (the Franz–Keldysh effect), absorption aided by localized states in the forbidden gap, and degeneracy effects when a significant number of states in the conduction band are not empty and/or when a significant number of state in the valence band are not full, as can happen in heavily doped materials (BGN) and under high-level injection (the Burstein–Moss shift). The net absorption coefficient is then the sum of the absorption coefficients due to all absorption

processes or

$$\alpha(h\nu) = \sum_{\mathrm{i}} \alpha_{\mathrm{i}}(h\nu). \tag{3.34}$$

In practice, measured absorption coefficients or empirical expressions for the absorption coefficient are used in analysis and modeling. The rate of creation of electron–hole pairs (# of electron–hole pairs per cm^3 per second) as a function of position within a solar cell is

$$G(x) = (1 - s) \int_{\lambda} (1 - r(\lambda)) f(\lambda) \alpha(\lambda) \mathrm{e}^{-\alpha x} \, \mathrm{d}\lambda \tag{3.35}$$

where s is the grid-shadowing factor, $r(\lambda)$ is the reflectance, $\alpha(\lambda)$ is the absorption coefficient, $f(\lambda)$ is the incident photon flux (number of photons incident per unit area per second per wavelength), and the sunlight is assumed to be incident at $x = 0$. Here, the absorption coefficient has been cast in terms of the light's wavelength through the relationship $h\nu = hc/\lambda$. The photon flux, $f(\lambda)$, is obtained by dividing the incident power density at each wavelength by the photon energy.

Free-carrier absorption, in which electrons in the conduction band absorb the energy of a photon and move to an empty state higher in the conduction band (correspondingly for holes in the valence band), is typically only significant for photons with $E < E_{\mathrm{G}}$ since the free-carrier absorption coefficient increases with increasing wavelength,

$$\alpha_{fc} \propto \lambda^{\gamma} \tag{3.36}$$

where $1.5 < \gamma < 3.5$ [9]. Thus, in single-junction solar cells, it does not affect the creation of electron–hole pairs and can be ignored (although free-carrier absorption can be exploited to probe the excess carrier concentrations in solar cells for the purpose of determining recombination parameters [10]). However, free-carrier absorption is a consideration in tandem solar cell systems in which a wide band gap (E_{G1}) solar cell is stacked on top of a solar cell of smaller band gap ($E_{\mathrm{G2}} < E_{\mathrm{G1}}$). Photons with energy too low to be absorbed in the top cell ($h\nu < E_{\mathrm{G1}}$) will be transmitted to the bottom cell and be absorbed there (if $h\nu > E_{\mathrm{G2}}$). Of course, more solar cells can be stacked as long as $E_{\mathrm{G1}} > E_{\mathrm{G2}} > E_{\mathrm{G3}} \ldots$, and so on. The number of photons transmitted to the next cell in the stack will be reduced by whatever amount of free-carrier absorption occurs. Tandem cells are discussed more completely in Chapters 9 and 12.

3.2.6 Recombination

When a semiconductor is taken out of thermal equilibrium, for instance by illumination and/or injection of current, the concentrations of electrons (n) and holes (p) tend to relax back toward their equilibrium values through a process called *recombination* in which an electron falls from the conduction band to the valence band, thereby eliminating a valence-band hole. There are several recombination mechanisms important to the operation of solar cells – recombination through traps (defects) in the forbidden gap, radiative (band-to-band) recombination, and Auger recombination – that will be discussed here. These three processes are illustrated in Figure 3.9.

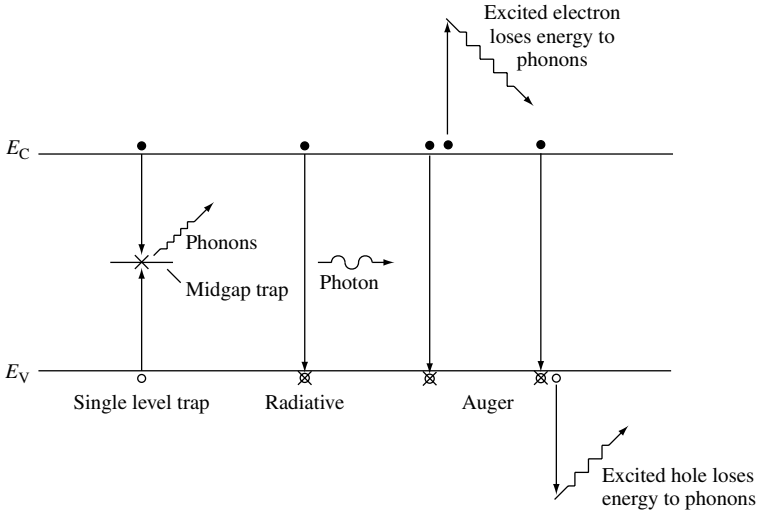

Figure 3.9 Recombination processes in semiconductors

The net recombination rate per unit volume per second through a single level trap (SLT) located at energy $E = E_T$ within the forbidden gap, also commonly referred to as *Shockley–Read–Hall recombination*, is given by [11]

$$R_{SLT} = \frac{pn - n_i^2}{\tau_{SLT,n}(p + n_i e^{(E_i - E_T)/kT}) + \tau_{SLT,p}(n + n_i e^{(E_T - E_i)/kT})} \tag{3.37}$$

where the carrier lifetimes are given by

$$\tau_{SLT} = \frac{1}{\sigma v_{th} N_T} \tag{3.38}$$

where σ is the capture cross section, v_{th} is the thermal velocity of the carriers, and N_T is the concentration of traps. The capture cross section can be thought of as the size of the target present to a carrier traveling through the semiconductor at velocity v_{th}. Small lifetimes correspond to high rates of recombination. If a trap presents a large target to the carrier, the recombination rate will be high (low carrier lifetime). When the velocity of the carrier is high, it has more opportunity within a given time period to encounter a trap and the carrier lifetime is low. Finally, the probability of interaction with a trap increases as the concentration of traps increases and the carrier lifetime is therefore inversely proportional to the trap concentration.

Some reasonable assumptions allow equation (3.37) to be simplified. If the material is p-type ($p \approx p_o \gg n_o$), in low injection ($n_o \leq n \ll p_o$), and the trap energy is near the middle of the forbidden gap ($E_T \approx E_i$), the recombination rate can be written as

$$R_{SLT} \approx \frac{n - n_o}{\tau_{SLT,n}}. \tag{3.39}$$

Notice that the recombination rate is solely dependent on the minority carrier (also called the limiting carrier). This is reasonable since there are far fewer minority carriers than majority carriers and one of each is necessary for there to be recombination.

If high-injection conditions prevail ($p \approx n \gg p_o, n_o$),

$$R_{\text{SLT}} \approx \frac{n}{\tau_{\text{SLT},p} + \tau_{\text{SLT},n}} \approx \frac{p}{\tau_{\text{SLT},p} + \tau_{\text{SLT},n}}. \tag{3.40}$$

In this case, the effective recombination lifetime is the sum of the two carrier lifetimes. While the recombination rate is high due to the large number of excess holes and electrons, the carrier lifetime is actually longer than in the case of low injection. This can be of significance in the base region of solar cells, especially concentrator cells (solar cells illuminated with concentrated sunlight), since the base is the least doped layer.

Radiative (band-to-band) recombination is simply the inverse of the optical generation process and is much more efficient in direct band gap semiconductors than in indirect band gap semiconductors. When radiative recombination occurs, the energy of the electron is given to an emitted photon – this is how semiconductor lasers and light emitting diodes (LEDs) operate. In an indirect band gap material, some of that energy is shared with a phonon. The net recombination rate due to radiative processes is given as

$$R_\lambda = \text{B}(pn - n_\text{i}^2). \tag{3.41}$$

If we have an n-type ($n \approx n_o \gg p_o$) semiconductor in low injection ($p_o \leq p \ll n_o$), the net radiative recombination rate can be written in terms of an effective lifetime, $\tau_{\lambda,p}$,

$$R_\lambda \approx \frac{p - p_o}{\tau_{\lambda,p}} \tag{3.42}$$

where

$$\tau_{\lambda,p} = \frac{1}{n_o \text{B}}. \tag{3.43}$$

A similar expression can be written for p-type semiconductors.

Auger recombination is somewhat similar to radiative recombination, except that the energy of transition is given to another carrier (in either the conduction band or the valence band), as shown in Figure 3.9. This electron (or hole) then relaxes thermally (releasing its excess energy and momentum to phonons). Just as radiative recombination is the inverse process to optical absorption, Auger recombination is the inverse process to *impact ionization*, where an energetic electron collides with a crystal atom, breaking the bond and creating an electron–hole pair. The net recombination rate due to Auger processes is

$$R_{\text{Auger}} = (\Lambda_n n + \Lambda_p p)(pn - n_\text{i}^2) \tag{3.44}$$

In an n-type material in low injection (and assuming Λ_n and Λ_p are of comparable magnitudes), the net Auger recombination rate becomes

$$R_{\text{Auger}} \approx \frac{p - p_o}{\tau_{\text{Auger},p}} \tag{3.45}$$

with

$$\tau_{\text{Auger},p} = \frac{1}{\Lambda_n n_o^2}. \tag{3.46}$$

A similar expression can be derived for minority electron lifetime in p-type material.

Each of these recombination processes occurs in parallel and there can be multiple and/or distributed traps[2] in the forbidden gap; thus the total recombination rate is the sum of rates due to each process

$$R = \left[\sum_{\text{traps } i} R_{\text{SLT},i}\right] + R_\lambda + R_{\text{Auger}}. \tag{3.47}$$

An effective minority-carrier lifetime for a doped material in low-level injection is given as

$$\frac{1}{\tau} = \left[\sum_{\text{traps } i} \frac{1}{\tau_{\text{SLT},i}}\right] + \frac{1}{\tau_\lambda} + \frac{1}{\tau_{\text{Auger}}}. \tag{3.48}$$

The distribution of traps in the energy gap for specific materials is given in other chapters.

Interfaces between two dissimilar materials, such as, those that occur at the front surface of a solar cell, have a high concentration defect due to the abrupt termination of the crystal lattice. These manifest themselves as a continuum of traps within the forbidden gap at the surface; electrons and holes can recombine through them just as with bulk traps. This is illustrated in Figure 3.10. Rather than giving a recombination rate per unit volume per second, surface traps give a recombination rate per unit area per second. A general expression for surface recombination is [11]

$$R_{\text{S}} = \int_{E_{\text{V}}}^{E_{\text{C}}} \frac{pn - n_{\text{i}}^2}{(p + n_{\text{i}}\text{e}^{(E_{\text{i}}-E_{\text{t}})/kT})/s_n + (n + n_{\text{i}}\text{e}^{(E_{\text{t}}-E_{\text{i}})/kT})/s_p} D_\Pi(E_{\text{t}})\,\text{d}E_{\text{t}} \tag{3.49}$$

where E_{t} is the trap energy, $D_\Pi(E_{\text{t}})$ is the surface state concentration (the concentration of traps is probably dependent on the trap energy), and s_n and s_p are surface recombination velocities, analogous to the carrier lifetimes for bulk traps. The surface recombination rate is generally written, for simplicity, as [11]

$$R_{\text{S}} = S_p(p - p_o) \tag{3.50}$$

in n-type material and as

$$R_{\text{S}} = S_n(n - n_o) \tag{3.51}$$

in p-type material. S_p and S_n are effective surface recombination velocities. It should be mentioned that these effective recombination velocities are not necessarily constants, though they are usually treated as such.

[2] It is unlikely that more than one trap will be involved in a single recombination event since the traps are spatially separated.

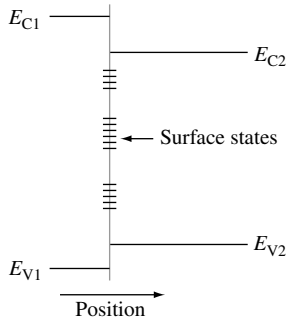

Figure 3.10 Illustration of surface states at a semiconductor surface or interface between dissimilar materials such as two different semiconductors (heterojunction) or a metal and a semiconductor (Schottky contact)

3.2.7 Carrier Transport

As has already been established, electrons and holes in a semiconductor behave much like a free particle of the same electronic charge with effective masses of m_n^* and m_p^*, respectively. Thus, they are subject to the classical processes of drift and diffusion. Drift is a charged particle's response to an applied electric field. When an electric field is applied across a uniformly doped semiconductor, the bands bend upward in the direction of the applied electric field. Electrons in the conduction band, being negatively charged, move in the opposite direction of the applied field and holes in the valence band, being positively charged, move in the same direction of the applied field (Figure 3.11) – in other words, electrons *sink* and holes *float*. This is a useful conceptual tool for analyzing the motion of holes and electrons in semiconductor devices. With nothing to impede their motion, the holes and electrons would continue to accelerate without bound. However, the semiconductor crystal is full of objects with which the carriers collide and are scattered. These objects include the component atoms of the crystal, dopant ions, crystal defects, and even other electrons and holes. On a microscopic scale, their motion is much like that of a ball in pinball machine, the carriers are constantly bouncing (scattering) off objects in the crystal, but generally moving in the direction prescribed by the applied electric field, $\vec{E} = -\nabla\phi$, where ϕ is the electrostatic potential. The net effect is that the carriers appear to move, on a macroscopic scale, at a constant velocity, v_{d}, the drift velocity. The drift velocity is directly proportional to the electric field

$$|\vec{v}_d| = |\mu\vec{E}| = |\mu\nabla\phi| \tag{3.52}$$

where μ is the carrier mobility. The carrier mobility is generally independent of the electric field strength unless the field is very strong, a situation not typically encountered in solar cells. The drift current densities for holes and electrons can be written as

$$\vec{J}_p^{\,\mathrm{drift}} = qp\vec{v}_{\mathrm{d},p} = q\mu_p p\vec{E} = -q\mu_p p\nabla\phi \tag{3.53}$$

and

$$\vec{J}_n^{\,\mathrm{drift}} = -qn\vec{v}_{\mathrm{d},n} = q\mu_n n\vec{E} = -q\mu_n n\nabla\phi. \tag{3.54}$$

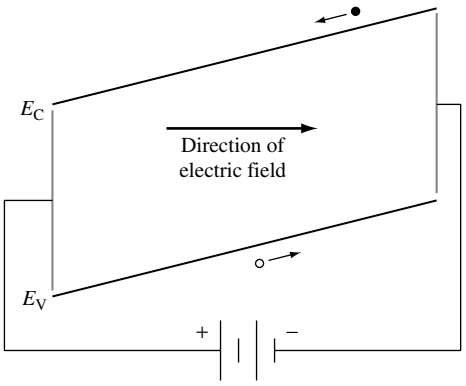

Figure 3.11 Illustration of the concept of drift in a semiconductor. Note that electrons and holes move in opposite directions. The electric field can be created by the internal built-in potential of the junction or by an externally applied bias voltage

The most significant scattering mechanisms in solar cells are lattice (phonon) and ionized impurity scattering. These component mobilities can be written as

$$\mu_L = C_L T^{-3/2} \tag{3.55}$$

for lattice scattering and as

$$\mu_I = \frac{C_I T^{3/2}}{N_D^+ + N_A^-} \tag{3.56}$$

for ionized impurity scattering. These can then be combined using Mathiessen's rule to give the carrier mobility [12]

$$\frac{1}{\mu} = \frac{1}{\mu_L} + \frac{1}{\mu_I}. \tag{3.57}$$

This is a first-order approximation that neglects the velocity dependencies of the scattering mechanisms. These two types of mobility can be distinguished experimentally by their different dependencies on temperature and doping. A better approximation is [12]

$$\mu = \mu_L \left[1 + \left(\frac{6\mu_L}{\mu_I} \right) \left(\mathrm{Ci}\left(\frac{6\mu_L}{\mu_I} \right) \cos\left(\frac{6\mu_L}{\mu_I} \right) + \left[\mathrm{Si}\left(\frac{6\mu_L}{\mu_I} \right) - \frac{\pi}{2} \right] \sin\left(\frac{6\mu_L}{\mu_I} \right) \right) \right], \tag{3.58}$$

where Ci and Si (not to be confused with the abbreviation for silicon) are the cosine and sine integrals, respectively.

When modeling solar cells, it is more convenient to use measured data or empirical formulas. Carrier mobilities in Si at 300 K are well approximated by [12]

$$\mu_n = 92 + \frac{1268}{1 + \left(\dfrac{N_D^+ + N_A^-}{1.3 \times 10^{17}} \right)^{0.91}} \mathrm{cm^2/V\text{-}s} \tag{3.59}$$

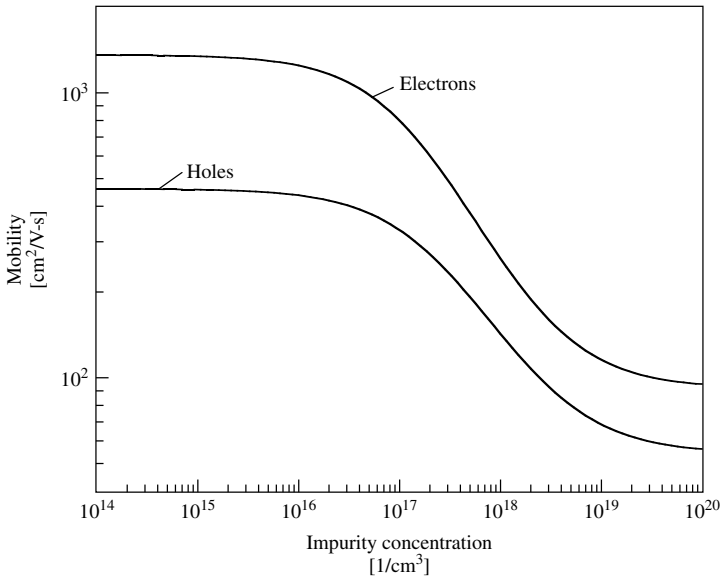

Figure 3.12 Electron and hole mobilities in silicon for $T = 300$ K

$$\mu_p = 54.3 + \frac{406.9}{1 + \left(\dfrac{N_{\mathrm{D}}^{+} + N_{\mathrm{A}}^{-}}{2.35 \times 10^{17}}\right)^{0.88}} \mathrm{cm}^2/\mathrm{V\text{-}s} \tag{3.60}$$

and are plotted in Figure 3.12. At low impurity levels, the mobility is governed by intrinsic lattice scattering, while at high levels the mobility is governed by ionized impurity scattering.

Electrons and holes in semiconductors tend, as a result of their random thermal motion, to move (diffuse) from regions of high concentration to regions of low concentration. Much like how the air in a balloon is distributed evenly within the volume of the balloon, carriers, in the absence of any external forces, will also tend to distribute themselves evenly. This process is called *diffusion* and the diffusion current densities are given by

$$\vec{J}_p^{\,\mathrm{diff}} = -q D_p \nabla p \tag{3.61}$$

$$\vec{J}_n^{\,\mathrm{diff}} = q D_n \nabla n \tag{3.62}$$

where D_p and D_n are the hole and electron diffusion coefficients, respectively. Note that they are driven by the gradient of the carrier densities.

In thermal equilibrium, there can be no net hole current and no net electron current – in other words, the drift and diffusion currents must exactly balance. In nondegenerate materials, this leads to the Einstein relationship

$$\frac{D}{\mu} = \frac{kT}{q} \tag{3.63}$$

and allows the diffusion coefficient to be directly computed from the mobility. Generalized forms of the Einstein relationship, valid for degenerate materials, are

$$\frac{D_n}{\mu_n} = \frac{1}{q} n \left[\frac{\mathrm{d}n}{\mathrm{d}E_\mathrm{F}} \right]^{-1} \tag{3.64}$$

and

$$\frac{D_p}{\mu_p} = \frac{-1}{q} p \left[\frac{\mathrm{d}p}{\mathrm{d}E_\mathrm{F}} \right]^{-1}. \tag{3.65}$$

The diffusion coefficient actually increases when degeneracy effects come into play.

The total hole and electron currents (vector quantities) are the sum of their drift and diffusion components

$$\vec{J}_p = \vec{J}_p^{\,\mathrm{drift}} + \vec{J}_p^{\,\mathrm{diff}} = q\mu_p p\vec{E} - qD_p \nabla p = -q\mu_p p \nabla\phi - qD_p \nabla p \tag{3.66}$$

$$\vec{J}_n = \vec{J}_n^{\,\mathrm{drift}} + \vec{J}_n^{\,\mathrm{diff}} = q\mu_n n\vec{E} + qD_n \nabla n = -q\mu_n n \nabla\phi + qD_n \nabla n \tag{3.67}$$

The total current is then

$$\vec{J} = \vec{J}_p + \vec{J}_n + \vec{J}_\mathrm{disp} \tag{3.68}$$

where $\vec{J}_\mathrm{disp}$ is the *displacement current* given by

$$\vec{J}_\mathrm{disp} = \frac{\partial \vec{D}}{\partial t}. \tag{3.69}$$

$\vec{D} = \varepsilon\vec{E}$ is the dielectric displacement field, where ε is the electric permittivity of the semiconductor. The displacement current is typically neglected in solar cells since they are static (dc) devices.

3.2.8 Semiconductor Equations

The operation of most semiconductor devices, including solar cells, can be described by the so-called semiconductor device equations, first derived by Van Roosbroeck in 1950 [13]. A generalized form of these equations is given here.

$$\nabla \cdot \varepsilon\vec{E} = q(p - n + N) \tag{3.70}$$

This is a form of Poisson's equation, where N is the net charge due to dopants and other trapped charges. The hole and electron continuity equations are

$$\nabla \cdot \vec{J}_p = q\left(G - R_p - \frac{\partial p}{\partial t}\right) \tag{3.71}$$

$$\nabla \cdot \vec{J}_n = q\left(R_n - G + \frac{\partial n}{\partial t}\right) \tag{3.72}$$

where G is the optical generation rate of electron–hole pairs. Thermal generation is included in R_p and R_n. The hole and electron current densities are given by

$$\vec{J}_p = -q\mu_p p\nabla(\phi - \phi_p) - kT\mu_p \nabla p \tag{3.73}$$

and

$$\vec{J}_n = -q\mu_n n\nabla(\phi + \phi_n) + kT\mu_n \nabla n. \tag{3.74}$$

Two new terms, ϕ_p and ϕ_n, have been introduced here. These are the so-called band parameters that account for degeneracy and a spatially varying band gap and electron affinity [14]. These terms were ignored in the preceding discussion and can usually be ignored in nondegenerate homostructure solar cells.

The intent here is to derive an analytic expression for the current–voltage characteristic of a simple solar cell, and so some simplifications are in order. It should be noted, however, that a complete description of the operation of solar cells can be obtained by solving the complete set of coupled partial differential equations, equations (3.70) through (3.74). The numerical solution of these equations is addressed later in this chapter.

3.2.9 Minority-carrier Diffusion Equation

In a uniformly doped semiconductor, the band gap and electric permittivity are independent of position. Since the doping is uniform, the carrier mobilities and diffusion coefficients are also independent of position. As we are mainly interested in the steady state operation of the solar cell, the semiconductor equations reduce to

$$\frac{\mathrm{d}\vec{E}}{\mathrm{d}x} = \frac{q}{\varepsilon}(p - n + N_\mathrm{D} - N_\mathrm{A}) \tag{3.75}$$

$$q\mu_p \frac{\mathrm{d}}{\mathrm{d}x}(p\vec{E}) - qD_p \frac{\mathrm{d}^2 p}{\mathrm{d}x^2} = q(G - R) \tag{3.76}$$

and

$$q\mu_n \frac{\mathrm{d}}{\mathrm{d}x}(n\vec{E}) + qD_n \frac{\mathrm{d}^2 n}{\mathrm{d}x^2} = q(R - G) \tag{3.77}$$

In regions sufficiently far from the pn-junction of the solar cell (quasi-neutral regions), the electric field is very small. When considering the minority carrier (holes in the n-type material and electrons in the p-type material) and low-level injection ($\Delta p = \Delta n \ll N_\mathrm{D}, N_\mathrm{A}$), the drift current can be neglected with respect to the diffusion current. Under low-level injection, R simplifies to

$$R = \frac{n_P - n_{Po}}{\tau_n} = \frac{\Delta n_P}{\tau_n} \tag{3.78}$$

in the p-type region and to

$$R = \frac{p_N - p_{No}}{\tau_p} = \frac{\Delta p_N}{\tau_p} \tag{3.79}$$

in the n-type region. Δp_N and Δn_P are the excess minority-carrier concentrations. The minority-carrier lifetimes, τ_n and τ_p, are given by equation (3.48). For clarity, the capitalized subscripts, "P" and "N", are used to indicate quantities in p-type and n-type regions, respectively, when it may not be otherwise apparent. Lower-case subscripts, "p" and "n", refer to quantities associated with minority holes and electrons, respectively. Equations (3.76) and (3.77) thus each reduce to what is commonly referred to as the *minority-carrier diffusion equation*. It can be written as

$$D_p \frac{\mathrm{d}^2 \Delta p_N}{\mathrm{d}x^2} - \frac{\Delta p_N}{\tau_p} = -G(x) \tag{3.80}$$

in n-type material and as

$$D_n \frac{\mathrm{d}^2 \Delta n_P}{\mathrm{d}x^2} - \frac{\Delta n_P}{\tau_n} = -G(x) \tag{3.81}$$

in p-type material. For example, Δn_P is the minority electron concentration in the p-type material. The minority-carrier diffusion equation is often used to analyze the operation of semiconductor devices, including solar cells.

3.3 *PN*-JUNCTION DIODE ELECTROSTATICS

Where an n-type semiconductor comes into contact with a p-type semiconductor, a *pn*-junction is formed. In thermal equilibrium there is no net current flow and by definition the Fermi energy must be independent of position. Since there is a concentration difference of holes and electrons between the two types of semiconductors, holes diffuse from the p-type region into the n-type region and, similarly, electrons from the n-type material diffuse into the p-type region. As the carriers diffuse, the charged impurities (ionized acceptors in the p-type material and ionized donors in the n-type material) are uncovered – that is, no longer screened by the majority carrier. As these impurity charges are uncovered, an electric field (or electrostatic potential difference) is produced, which limits the diffusion of the holes and electrons. In thermal equilibrium, the diffusion and drift currents for each carrier type exactly balance, so there is no net current flow. The transition region between the n-type and the p-type semiconductors is called the *space-charge region*. It is also often called the *depletion region*, since it is effectively depleted of both holes and electrons. Assuming that the p-type and the n-type regions are sufficiently thick, the regions on either side of the depletion region are essentially charge-neutral (often termed *quasi-neutral*). The electrostatic potential difference resulting from the junction formation is called the *built-in voltage*, V_{bi}. It arises from the electric field created by the exposure of the positive and the negative space charge in the depletion region.

The electrostatics of this situation (assuming a single acceptor and a single donor level) are governed by Poisson's equation

$$\nabla^2 \phi = \frac{q}{\varepsilon}(n_o - p_o + N_{\mathrm{A}}^- - N_{\mathrm{D}}^+) \tag{3.82}$$

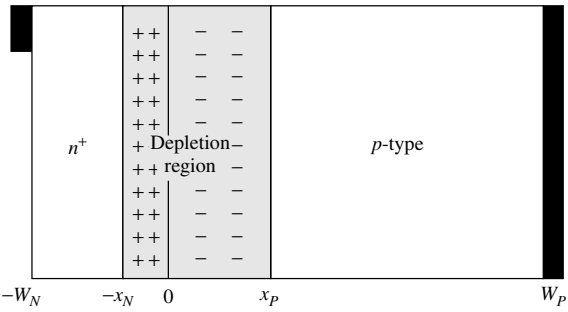

Figure 3.13 Simple solar cell structure used to analyze the operation of a solar cell. Free carriers have diffused across the junction ($x = 0$) leaving a space-charge or depletion region practically devoid of any free or mobile charges. The fixed charges in the depletion region are due to ionized donors on the n-side and ionized acceptors on the p-side

where ϕ is the electrostatic potential, q is magnitude of the electron charge, ε is the electric permittivity of the semiconductor, p_o is the equilibrium hole concentration, n_o is the equilibrium electron concentration, N_A^- is the ionized acceptor concentration, and N_D^+ is the ionized donor concentration. Equation 3.82 is a restatement of equation 3.70 for the given conditions.

This equation is easily solved numerically; however, an approximate analytic solution for an abrupt *pn*-junction can be obtained that lends physical insight into the formation of the space-charge region. Figure 3.13 depicts a simple one-dimensional (1D) *pn*-junction solar cell (diode), with the metallurgical junction at $x = 0$, which is uniformly doped N_D on the n-type side and N_A on the p-type side. For simplicity, it is assumed that the each side is nondegenerately doped and that the dopants are fully ionized.

Within the depletion region, defined by $-x_N < x < x_P$, it can be assumed that p_o and n_o are both negligible compared to $|N_A - N_D|$ so that equation (3.82) can be simplified to

$$\begin{aligned} \nabla^2\phi &= -\frac{q}{\varepsilon}N_D, \quad \text{for} - x_N < x < 0 \quad \text{and} \\ \nabla^2\phi &= \frac{q}{\varepsilon}N_A, \quad \text{for} \quad 0 < x < x_P \end{aligned} \tag{3.83}$$

Outside the depletion region, charge neutrality is assumed and

$$\nabla^2\phi = 0 \quad \text{for} \quad x \le -x_N \quad \text{and} \quad x \ge x_P. \tag{3.84}$$

This is commonly referred to as the *depletion approximation*. The regions on either side of the depletion regions are the quasi-neutral regions.

The electrostatic potential difference across the junction is the built-in voltage, V_{bi}, and can be obtained by integrating the electric field, $\vec{E} = -\nabla\phi$.

$$\int_{-x_N}^{x_P} \vec{E}\,dx = -\int_{-x_N}^{x_P} \frac{d\phi}{dx}dx = -\int_{V(-x_N)}^{V(x_P)} d\phi = \phi(-x_N) - \phi(x_P) = V_{bi} \tag{3.85}$$

Solving equations (3.83) and (3.84) and defining $\phi(x_P) = 0$, gives

$$\phi(x) = \begin{cases} V_{\text{bi}}, x \leq -x_N \\ V_{\text{bi}} - \dfrac{qN_{\text{D}}}{2\varepsilon}(x + x_N)^2, -x_N < x \leq 0 \\ \dfrac{qN_{\text{A}}}{2\varepsilon}(x - x_P)^2, 0 \leq x < x_P \\ 0, x \geq x_P \end{cases} \tag{3.86}$$

The electrostatic potential must be continuous at $x = 0$. Therefore, from equation (3.86),

$$V_{\text{bi}} - \frac{qN_{\text{D}}}{2\varepsilon}x_N^2 = \frac{qN_{\text{A}}}{2\varepsilon}x_P^2 \tag{3.87}$$

In the absence of any interface charge at the metallurgical junction, the electric field is also continuous at this point (really, it is the displacement field, $\vec{D} = \varepsilon\vec{E}$, but in this example, ε is independent of position), and

$$x_N N_{\text{D}} = x_P N_{\text{A}} \tag{3.88}$$

This is simply a statement that the total charge in either side of the depletion region exactly balance each other and therefore the depletion region extends furthest into the more lightly doped side.

Solving equations (3.87) and (3.88) for the depletion width, W_{D}, gives[3]

$$W_{\text{D}} = x_N + x_P = \sqrt{\frac{2\varepsilon}{q}\left(\frac{N_{\text{A}} + N_{\text{D}}}{N_{\text{A}}N_{\text{D}}}\right)V_{\text{bi}}}. \tag{3.89}$$

Under nonequilibrium conditions, the electrostatic potential difference across the junction is modified by the applied voltage, V, which is zero in thermal equilibrium. As a consequence, the depletion width is dependent on the applied voltage,

$$W_{\text{D}}(V) = x_N + x_P = \sqrt{\frac{2\varepsilon}{q}\left(\frac{N_{\text{A}} + N_{\text{D}}}{N_{\text{A}}N_{\text{D}}}\right)(V_{\text{bi}} - V)}. \tag{3.90}$$

As previously stated, the built-in voltage, V_{bi}, can be calculated by noting that under thermal equilibrium the net hole and electron currents are zero. The hole current density is

$$\vec{J}_p = q\mu_p p_o \vec{E} - qD_p \nabla p = 0. \tag{3.91}$$

[3] A somewhat more rigorous treatment of equation 3.89 would yield a factor of $2kT/q$ which is ~50 mV at 300 K, or

$$W_{\text{D}} = \sqrt{\frac{2\varepsilon}{q}\left(\frac{N_{\text{A}} + N_{\text{D}}}{N_{\text{A}}N_{\text{D}}}\right)(V_{\text{bi}} - 2kT/q)} \quad [3].$$

Thus, in 1D, utilizing the Einstein relationship, the electric field can be written as

$$\vec{E} = \frac{kT}{q}\frac{1}{p_o}\frac{\mathrm{d}p_o}{\mathrm{d}x} \tag{3.92}$$

Rewriting equation (3.85) and substituting equation (3.92) yields

$$V_{\mathrm{bi}} = \int_{-x_N}^{x_P} E\vec{\mathrm{d}}x = \int_{-x_N}^{x_P} \frac{kT}{q}\frac{1}{p_o}\frac{\mathrm{d}p_o}{\mathrm{d}x}\mathrm{d}x = \frac{kT}{q}\int_{p_o(-x_N)}^{p_o(x_P)} \frac{\mathrm{d}p_o}{p_o} = \frac{kT}{q}\ln\left[\frac{p_o(x_P)}{p_o(-x_N)}\right] \tag{3.93}$$

Since we have assumed nondegeneracy, $p_o(x_P) = N_{\mathrm{A}}$ and $p_o(-x_N) = n_{\mathrm{i}}^2/N_{\mathrm{D}}$. Therefore,

$$V_{\mathrm{bi}} = \frac{kT}{q}\ln\left[\frac{N_{\mathrm{D}}N_{\mathrm{A}}}{n_{\mathrm{i}}^2}\right]. \tag{3.94}$$

Figure 3.14 shows the equilibrium energy band diagram, electric field, and charge density for a simple abrupt *pn*-junction silicon diode in the vicinity of the depletion region. The conduction bandedge is given by $E_{\mathrm{C}}(x) = E_0 - q\phi(x) - \chi$, the valence bandedge

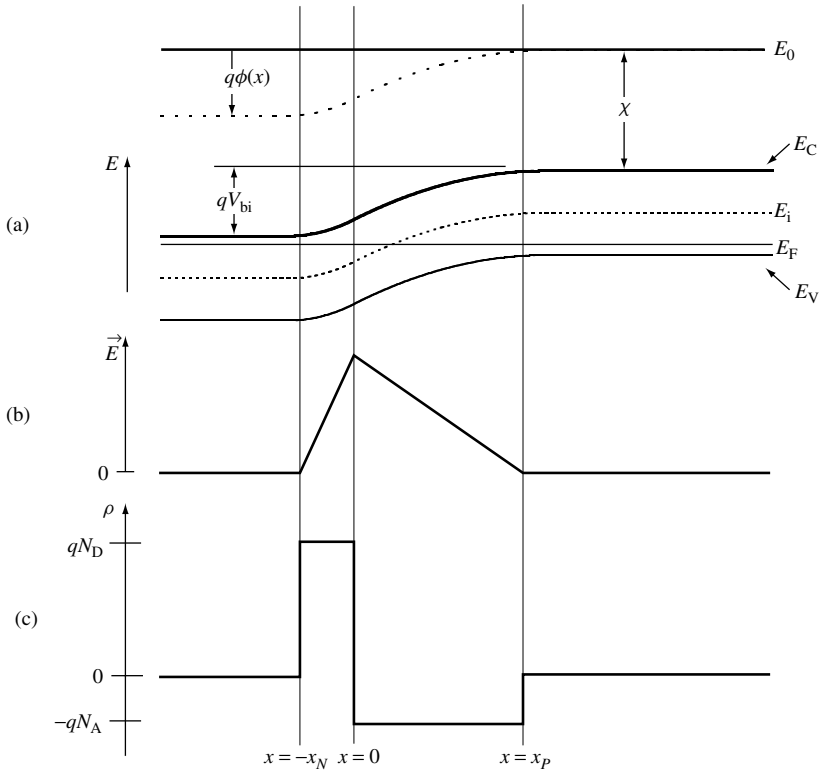

Figure 3.14 Equilibrium conditions in a solar cell: (a) energy bands; (b) electric field; and (c) charge density

by $E_V(x) = E_C(x) - E_G$, and the intrinsic energy by equation (3.19). E_0, defined as the vacuum energy, serves as a convenient reference point and is universally constant with position. An electron at the vacuum energy is, by definition, completely free of influence from all external forces. The electron affinity, χ, is the minimum energy needed to free an electron from the bottom of the conduction band and take it to the vacuum level. The electric field is a result of the uncovered ionized donors and acceptors and opposes the diffusion of electrons and holes in the quasi-neutral regions. The charge density plot illustrates the balance of charge between the two sides of the depletion region. In heterojunctions, both the band gap and the electron affinity are position-dependent – making the calculation of the junction electrostatics and energy band diagram more involved.

The basic solar cell structure has now been established (Figure 3.13). It is simply a *pn*-junction diode consisting of two quasi-neutral regions on either side of a depletion region with an electrical contact made to each quasi-neutral region. Typically, the more heavily doped quasi-neutral region is called the *emitter* (the *n*-type region in Figure 3.13) and the more lightly doped region is called the *base* (the *p*-type region in Figure 3.13). The base region is also often referred to as the *absorber region* since the emitter region is usually very thin and most of the light absorption occurs in the base. This basic structure will serve as the basis for deriving the fundamental operating characteristics of the solar cell.

3.4 SOLAR CELL FUNDAMENTALS

The basic current–voltage characteristic of the solar cell can be derived by solving the minority-carrier diffusion equation with appropriate boundary conditions.

3.4.1 Solar Cell Boundary Conditions

At $x = -W_N$, the usual assumption is that the front contact can be treated as an ideal ohmic contact. Hence,

$$\Delta p(-W_N) = 0. \tag{3.95}$$

However, since the front contact is usually a grid with metal contacting the semiconductor on only a small percentage of the front surface, modeling the front surface with an effective surface recombination velocity is more realistic. This effective recombination velocity models the combined effects of the ohmic contact and the antireflective passivation layer (SiO_2 in silicon solar cells). In this case, the boundary condition at $x = -W_N$ is

$$\frac{d\Delta p}{dx} = \frac{S_{F,\text{eff}}}{D_p}\Delta p(-W_N) \tag{3.96}$$

where $S_{F,\text{eff}}$ is the effective front surface recombination velocity. As $S_{F,\text{eff}} \to \infty$, $\Delta p \to 0$, and the boundary condition given by equation (3.96) reduces to that of an ideal ohmic contact (equation 3.95). In reality, $S_{F,\text{eff}}$ depends upon a number of parameters and is bias-dependent. This will be discussed in more detail later.

The back contact could also be treated as an ideal ohmic contact, so that

$$\Delta n(W_P) = 0. \tag{3.97}$$

However, solar cells are often fabricated with a *back-surface field* (BSF), a thin more heavily doped region at the back of the base region. The BSF keeps minority carriers away from the back ohmic contact and increases their chances of being collected and it can be modeled by an effective, and relatively low, surface recombination velocity. This boundary condition is then

$$\left.\frac{\mathrm{d}\Delta n}{\mathrm{d}x}\right|_{x=W_P} = -\frac{S_{\mathrm{BSF}}}{D_n}\Delta n(W_P), \tag{3.98}$$

where S_{BSF} is the effective surface recombination velocity at the BSF.

All that remains now is to determine suitable boundary conditions at $x = -x_N$ and $x = x_P$. These boundary conditions are commonly referred to as the *law of the junction*.

Under equilibrium conditions, zero applied voltage and no illumination, the Fermi energy, E_{F}, is constant with position. When a bias voltage is applied, it is convenient to introduce the concept of quasi-Fermi energies. It was shown earlier that the equilibrium carrier concentrations could be related to the Fermi energy (equations 3.15 and 3.16). Under nonequilibrium conditions, similar relationships hold. Assuming the semiconductor is nondegenerate,

$$p = n_{\mathrm{i}}\mathrm{e}^{(E_{\mathrm{i}}-F_P)/kT} \tag{3.99}$$

and

$$n = n_{\mathrm{i}}\mathrm{e}^{(F_N-E_{\mathrm{i}})/kT} \tag{3.100}$$

It is evident that under equilibrium conditions $F_P = F_N = E_{\mathrm{F}}$. Under nonequilibrium conditions, assuming that the majority carrier concentrations at the contacts retain their equilibrium values, the applied voltage can be written as

$$qV = F_N(-W_N) - F_P(W_P) \tag{3.101}$$

Since, in low-level injection, the majority carrier concentrations are constant throughout the quasi-neutral regions, that is, $p_P(x_P \le x \le W_P) = N_{\mathrm{A}}$ and $n_N(-W_N \le x \le -x_N) = N_{\mathrm{D}}$, $F_N(-W_N) = F_N(-x_N)$ and $F_P(W_P) = F_P(x_P)$. Then, assuming that both the quasi-Fermi energies remain constant inside the depletion region,

$$qV = F_N(x) - F_P(x) \tag{3.102}$$

for $-x_N \le x \le x_P$, that is, everywhere inside the depletion region. Using equations (3.99) and (3.100), this leads directly to the *law of the junction*, the boundary conditions used at the edges of the depletion region,

$$p_N(-x_N) = \frac{n_{\mathrm{i}}^2}{N_{\mathrm{D}}}\mathrm{e}^{qV/kT} \tag{3.103}$$

and

$$n_P(x_P) = \frac{n_i^2}{N_A} e^{qV/kT}. \tag{3.104}$$

3.4.2 Generation Rate

For light incident at the front of the solar cell, $x = -W_N$, the optical generation rate takes the form (see equation 3.35)

$$G(x) = (1 - s) \int_\lambda (1 - r(\lambda)) f(\lambda) \alpha(\lambda) e^{-\alpha(x + W_N)} \, d\lambda. \tag{3.105}$$

Only photons with $\lambda \leq hc/E_G$ contribute to the generation rate.

3.4.3 Solution of the Minority-carrier Diffusion Equation

Using the boundary conditions defined by equations (3.96), (3.98), (3.103), and (3.104) and the generation rate given by equation (3.105), the solution to the minority-carrier diffusion equation, equation (3.80), is easily shown to be

$$\Delta p_N(x) = A_N \sinh[(x + x_N)/L_p] + B_N \cosh[(x + x_N)/L_p] + \Delta p'_N(x) \tag{3.106}$$

in the n-type region and

$$\Delta n_P(x) = A_P \sinh[(x - x_P)/L_n] + B_P \cosh[(x - x_P)/L_n] + \Delta n'_P(x) \tag{3.107}$$

in the p-type region. The particular solutions due to $G(x)$, $\Delta p'_N(x)$, and $\Delta n'_P(x)$ are given by

$$\Delta p'_N(x) = -(1 - s) \int_\lambda \frac{\tau_p}{(L_p^2 \alpha^2 - 1)} [1 - r(\lambda)] f(\lambda) \alpha(\lambda) e^{-\alpha(x + W_N)} \, d\lambda \tag{3.108}$$

and

$$\Delta n'_P(x) = -(1 - s) \int_\lambda \frac{\tau_n}{(L_n^2 \alpha^2 - 1)} [1 - r(\lambda)] f(\lambda) \alpha(\lambda) e^{-\alpha(x + W_N)} \, d\lambda. \tag{3.109}$$

Using the boundary conditions set above, A_N, B_N, A_P, and B_P are easily obtained.

3.4.4 Terminal Characteristics

The minority-carrier current densities in the quasi-neutral regions are just the diffusion currents, since the electric field is negligible. Using the active sign convention for the current (since a solar cell is typically thought of as a battery) gives

$$\vec{J}_{p,N}(x) = -q D_p \frac{d\Delta p_N}{dx} \tag{3.110}$$

and

$$\vec{J}_{n,P}(x) = q D_n \frac{\mathrm{d}\Delta n_P}{\mathrm{d}x} \tag{3.111}$$

The total current is given by

$$I = A[J_p(x) + J_n(x)] \tag{3.112}$$

and is true everywhere within the solar cell (A is the area of the solar cell). Equations (3.110) and (3.111) give only the hole current in the n-type region and the electron current in the p-type region, not both at the same point. However, integrating equation (3.72), the electron continuity equation, over the depletion region, gives

$$\int_{-x_N}^{x_P} \frac{\mathrm{d}\vec{J}_n \mathrm{d}x}{\mathrm{d}x} \mathrm{d}x = \vec{J}_n(x_P) - \vec{J}_n(-x_N) = q \int_{-x_N}^{x_P} [R(x) - G(x)]\,\mathrm{d}x \tag{3.113}$$

$G(x)$ is easily integrated and the integral of the recombination rate can be approximated by assuming that the recombination rate is constant within the depletion region and is $R(x_m)$ where x_m is the point at which $p_\mathrm{D}(x_m) = n_\mathrm{D}(x_m)$ and corresponds to the maximum recombination rate in the depletion region. If recombination via a midgap single level trap is assumed, then, from equations (3.37), (3.99), (3.100), and (3.102), the recombination rate in the depletion region is

$$R_\mathrm{D} = \frac{p_\mathrm{D} n_\mathrm{D} - n_\mathrm{i}^2}{\tau_n(p_\mathrm{D} + n_\mathrm{i}) + \tau_p(n_\mathrm{D} + n_\mathrm{i})} = \frac{n_\mathrm{D}^2 - n_\mathrm{i}^2}{(\tau_n + \tau_p)(n_\mathrm{D} + n_\mathrm{i})} = \frac{n_\mathrm{D} - n_\mathrm{i}}{(\tau_n + \tau_p)} = \frac{n_\mathrm{i}(\mathrm{e}^{qV/2kT} - 1)}{\tau_\mathrm{D}} \tag{3.114}$$

where τ_D is the effective lifetime in the depletion region. From equation (3.113), $\vec{J}_n(-x_N)$, the majority carrier current at $x = -x_N$, can now be written as

$$\begin{aligned}\vec{J}_n(-x_N) &= \vec{J}_n(x_P) + q \int_{-x_N}^{x_P} G(x)\,\mathrm{d}x - q \int_{-x_N}^{x_P} R_\mathrm{D} \mathrm{d}x \\ &= \vec{J}_n(x_P) + q(1-s) \int_\lambda [1 - r(\lambda)] f(\lambda) [\mathrm{e}^{-\alpha(W_N - x_N)} - \mathrm{e}^{-\alpha(W_N + x_P)}]\,\mathrm{d}\lambda \\ &\quad - q \frac{W_\mathrm{D} n_\mathrm{i}}{\tau_\mathrm{D}} (\mathrm{e}^{qV/2kT} - 1)\end{aligned} \tag{3.115}$$

where $W_\mathrm{D} = x_P + x_N$. Substituting into equation (3.112), the total current is now

$$I = A \left[J_p(-x_N) + J_n(x_P) + J_\mathrm{D} - q \frac{W_\mathrm{D} n_\mathrm{i}}{\tau_\mathrm{D}} (\mathrm{e}^{qV/2kT} - 1) \right] \tag{3.116}$$

where

$$J_\mathrm{D} = q(1-s) \int_\lambda [1 - r(\lambda)] f(\lambda) (\mathrm{e}^{-\alpha(W_N - x_N)} - \mathrm{e}^{-\alpha(W_N + x_P)})\,\mathrm{d}\lambda \tag{3.117}$$

is the generation current from the depletion region and A is the area of the solar cell. The last term of equation (3.116) represents recombination in the space-charge region.

The solutions to the minority-carrier diffusion equation, equations (3.106) and (3.107), can be used to evaluate the minority-carrier current densities, equations (3.110) and (3.111). These can then be substituted into equation (3.116), which, with some algebraic manipulation, yields

$$I = I_{SC} - I_{o1}(e^{qV/kT} - 1) - I_{o2}(e^{qV/2kT} - 1) \tag{3.118}$$

where I_{SC} is the short-circuit current and is the sum of the contributions from each of the three regions: the n-type region (I_{SCN}), the depletion region ($I_{SCD} = AJ_D$), and the p-type region (I_{SCP})

$$I_{SC} = I_{SCN} + I_{SCD} + I_{SCP} \tag{3.119}$$

where

$$I_{SCN} = qAD_p \left[\frac{\Delta p'(-x_N)T_{p1} - S_{F,\text{eff}}\Delta p'(-W_N) + D_p \left.\dfrac{d\Delta p'}{dx}\right|_{x=-W_N}}{L_p T_{p2}} - \left.\frac{d\Delta p'}{dx}\right|_{x=-x_N} \right] \tag{3.120}$$

with

$$T_{p1} = D_p/L_p \sinh[(W_N - x_N/L_p] + S_{F,\text{eff}} \cosh[(W_N - x_N/L_p] \tag{3.121}$$

$$T_{p2} = D_p/L_p \cosh[(W_N - x_N)/L_p] + S_{F,\text{eff}} \sinh[(W_N - x_N)/L_p] \tag{3.122}$$

and

$$I_{SCP} = qAD_n \left[\frac{\Delta n'(x_P)T_{n1} - S_{BSF}\Delta n'(W_P) + D_n \left.\dfrac{d\Delta n'}{dx}\right|_{x=W_P}}{L_n T_{n2}} + \left.\frac{d\Delta n'}{dx}\right|_{x=x_P} \right] \tag{3.123}$$

with

$$T_{n1} = D_n/L_n \sinh[(W_P - x_P)/L_n] + S_{BSF} \cosh[(W_P - x_P)/L_n] \tag{3.124}$$

$$T_{n2} = D_n/L_n \cosh[(W_P - x_P)/L_n] + S_{BSF} \sinh[(W_P - x_P)/L_n] \tag{3.125}$$

I_{o1} is the dark saturation current due to recombination in the quasi-neutral regions,

$$I_{o1} = I_{o1,p} + I_{o1,n} \tag{3.126}$$

with

$$I_{o1,p} = qA\frac{n_i^2}{N_D}\frac{D_p}{L_p}\left\{ \frac{D_p/L_p \sinh[(W_N - x_N)/L_p] + S_{F,\text{eff}} \cosh[(W_N - x_N/L_p]}{D_p/L_p \cosh[(W_N - x_N)/L_p] + S_{F,\text{eff}} \sinh[(W_N - x_N)/L_p]} \right\} \tag{3.127}$$

and

$$I_{o1,n} = qA\frac{n_i^2}{N_A}\frac{D_n}{L_n} \times \left\{\frac{D_n/L_n \sinh[(W_P - x_P)/L_n] + S_{BSF}\cosh[(W_P - x_P)/L_n]}{D_n/L_n \cosh[(W_P - x_P)/L_n] + S_{BSF}\sinh[(W_P - x_P)/L_n]}\right\} \quad (3.128)$$

These are very general expressions for the dark saturation current and reduce to more familiar forms when appropriate assumptions are made, as will be seen later.

I_{o2} is the dark saturation current due to recombination in the space-charge region,

$$I_{o2} = qA\frac{W_D n_i}{\tau_D} \quad (3.129)$$

and is bias-dependent since the depletion width, W_D, is a function of the applied voltage (equation 3.89).

3.4.5 Solar Cell $I-V$ Characteristics

Equation (3.118), repeated here, is a general expression for the current produced by a solar cell.

$$I = I_{SC} - I_{o1}(e^{qV/kT} - 1) - I_{o2}(e^{qV/2kT} - 1) \quad (3.130)$$

The short-circuit current and dark saturation currents are given by rather complex expressions (equations 3.119, 3.128, and 3.129) that depend on the solar cell structure, material properties, and the operating conditions. A full understanding of solar cell operation requires detailed examination of these terms. However, much can be learned about solar cell operation by examining the basic form of equation (3.130). From a circuit perspective, it is apparent that a solar cell can be modeled by an ideal current source (I_{SC}) in parallel with two diodes – one with an ideality factor of "1" and the other with an ideality factor of "2", as shown in Figure 3.15. Note that the direction of the current source is opposed to the current flow of the diodes – that is, it serves to forward-bias the diodes.

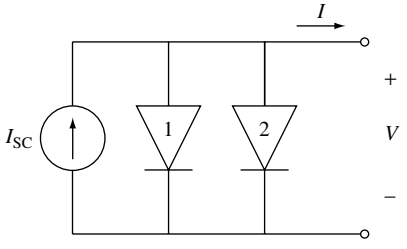

Figure 3.15 Simple solar cell circuit model. Diode 1 represents the recombination current in the quasi-neutral regions ($\propto e^{qV/kT}$), while diode 2 represents recombination in the depletion region ($\propto e^{qV/2kT}$)

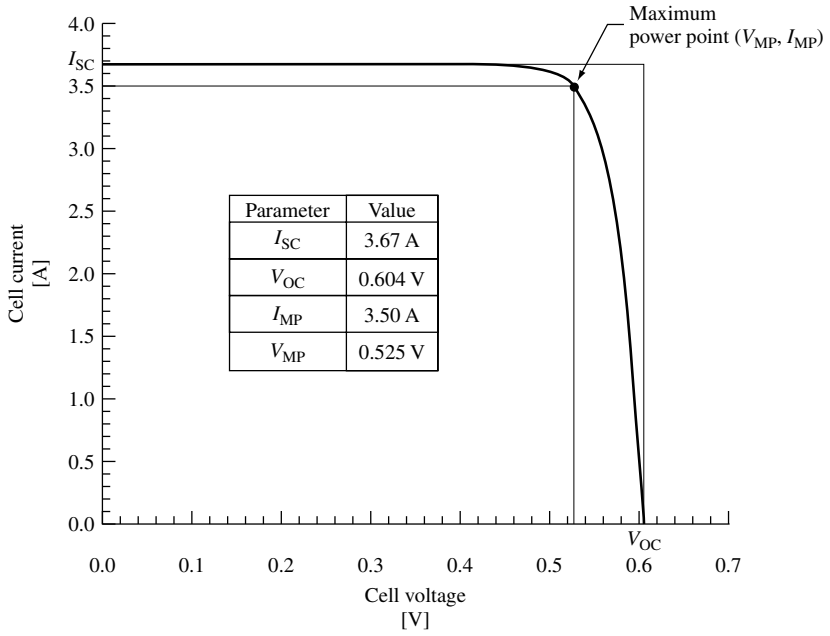

Figure 3.16 Current–voltage characteristic of the silicon solar cell defined by Table 3.2

The current–voltage ($I-V$) characteristic of a typical silicon solar cell is plotted in Figure 3.16 for the parameter values given in Table 3.2. For simplicity, the dark current due to the depletion region (diode 2) has been ignored (a reasonable and common assumption for a good silicon solar cell, especially at larger forward biases). It illustrates several important figures of merit for solar cells – the short-circuit current, the open-circuit voltage, and the fill factor. At small applied voltages, the diode current is negligible and the current is just the short-circuit current, I_{SC}, as can be seen when V is set to zero in equation (3.130). When the applied voltage is high enough so that the diode current (recombination current) becomes significant, the solar cell current drops quickly.

Table 3.2 shows the huge asymmetry between the n-emitter and the p-base in a typical solar cell. The emitter is $\sim$1000 times thinner, 10 000 times more heavily doped, and its diffusion length is $\sim$100 times shorter than the corresponding quantities in the base.

At open circuit ($I = 0$), all the light-generated current, I_{SC}, is flowing through diode 1, so the open-circuit voltage can be written as

$$V_{OC} = \frac{kT}{q} \ln \frac{I_{SC} + I_{o1}}{I_{o1}} \approx \frac{kT}{q} \ln \frac{I_{SC}}{I_{o1}}, \tag{3.131}$$

where $I_{SC} \gg I_{o1}$.

Of particular interest is the point on the $I-V$ curve where the power produced is at a maximum. This is referred to as the *maximum power point* with $V = V_{MP}$ and $I = I_{MP}$. As seen in Figure 3.18, this point defines a rectangle whose area, given by $P_{MP} = V_{MP} I_{MP}$, is the largest rectangle for any point on the $I-V$ curve. The maximum

Table 3.2 Si solar cell model parameters

Parameter	Value
A	100 cm^2
W_N	0.35 μm
N_D	1×10^{20} cm^{-3}
D_p	1.5 cm^2/V-s
$S_{F,eff}$	3×10^4 cm/s
τ_p	1 μs
L_p	12 μm
W_P	300 μm
N_A	1×10^{15} cm^{-3}
D_n	35 cm^2/V-s
S_{BSF}	100 cm/s
τ_n	350 μs
L_n	1100 μm

power point is found by solving

$$\left.\frac{\partial P}{\partial V}\right|_{V=V_{MP}} = \left.\frac{\partial (IV)}{\partial V}\right|_{V=V_{MP}} = \left.\left[I + V\frac{\partial I}{\partial V}\right]\right|_{V=V_{MP}} = 0 \tag{3.132}$$

for $V = V_{MP}$. The current at the maximum power point, I_{MP}, is then found by evaluating equation (3.130) at $V = V_{MP}$.

The rectangle-defined V_{OC} and I_{SC} provides a convenient means for characterizing the maximum power point. The fill factor, FF, is a measure of the *squareness* of the $I-V$ characteristic and is always less than one. It is the ratio of the areas of the two rectangles shown in Figure 3.16 or

$$FF = \frac{P_{MP}}{V_{OC} I_{SC}} = \frac{V_{MP} I_{MP}}{V_{OC} I_{SC}} \tag{3.133}$$

An empirical expression for the fill factor is [15]

$$FF = \frac{V_{OC} - \dfrac{kT}{q}\ln[qV_{OC}/kT + 0.72]}{V_{OC} + kT/q}. \tag{3.134}$$

Arguably, the most important figure of merit for a solar cell is its power conversion efficiency, η, which is defined as

$$\eta = \frac{P_{MP}}{P_{in}} = \frac{FFV_{OC}I_{SC}}{P_{in}} \tag{3.135}$$

The incident power, P_{in}, is determined by the properties of the light spectrum incident upon the solar cell. Further information regarding experimental determination of these parameters appears in Chapter 16.

Another important figure of merit is the collection efficiency, which can be defined relative to both optical and recombination losses as an *external* collection efficiency

$$\eta_{\mathrm{C}}^{\mathrm{ext}} = \frac{I_{\mathrm{SC}}}{I_{ph}} \tag{3.136}$$

where

$$I_{ph} = qA \int_{\lambda<\lambda_{\mathrm{G}}} f(\lambda)\, \mathrm{d}\lambda \tag{3.137}$$

is the maximum possible photocurrent that would result if all photons with $E > E_{\mathrm{G}}$ ($\lambda < \lambda_{\mathrm{G}} = hc/E_{\mathrm{G}}$) created electron–hole pairs that were collected. The collection efficiency can also be defined with respect to recombination losses as the internal collection efficiency

$$\eta_{\mathrm{C}}^{\mathrm{int}} = \frac{I_{\mathrm{SC}}}{I_{\mathrm{gen}}} \tag{3.138}$$

where

$$I_{\mathrm{gen}} = qA(1-s) \int_{\lambda<\lambda_{\mathrm{G}}} [1-r(\lambda)] f(\lambda)(1-\mathrm{e}^{-\alpha(W_N+W_P)})\, \mathrm{d}\lambda \tag{3.139}$$

is the light-generated current. This represents what the short-circuit current would be if every photon that is absorbed is collected and contributes to the short-circuit current. $I_{\mathrm{gen}} = I_{\mathrm{inc}}$ when there is no grid shadowing, no reflective losses, and the solar cell has infinite optical thickness.

3.4.6 Properties of Efficient Solar Cells

Using these figures of merit, the properties of a good (efficient) solar cell can be ascertained. From equation (3.135), it is clear that an efficient solar cell will have a high short-circuit current, I_{SC}, a high open-circuit voltage, V_{OC}, and a fill factor, FF, as close as possible to 1.

$I_{\mathrm{SC}} = \eta_{\mathrm{C}}^{\mathrm{int}} I_{\mathrm{gen}}$ is directly proportional to both the internal collection efficiency and the light-generated current, I_{gen}. The internal collection efficiency is solely dependent on the recombination in the solar cell and will approach 1 as $\tau \to \infty$ and $S \to 0$. To maximize I_{gen} (i.e. $I_{\mathrm{gen}} \to I_{\mathrm{inc}}$), the solar cell should be designed with a minimum amount of grid shadowing (s), minimum reflectance ($r(\lambda)$), and be optically thick enough such that nearly all the photons with $E > E_{\mathrm{G}}$ are absorbed.

The open-circuit voltage

$$V_{\mathrm{OC}} \approx \frac{kT}{q} \ln \frac{I_{\mathrm{SC}}}{I_{o1}} \tag{3.140}$$

is logarithmically proportional to the short-circuit current and to the reciprocal of the reverse saturation current, I_{o1} (the same is true for I_{o2}). Therefore, reducing the saturation

current will increase the open-circuit voltage. From equations (3.127) and (3.128), it is obvious that $I_{o1} \to 0$ as $\tau \to \infty$ and $S \to 0$.

From equation (3.134) it is clear that increasing V_{OC} will increase the fill factor, FF. Thus, the design and the operation of an efficient solar cell has two basic goals:

1) Minimization of recombination rates throughout the device.
2) Maximization of the absorption of photons with $E > E_G$.

It is evident that, despite the apparent complexity of the expressions describing the operation of solar cells, the basic operating principles are easy to understand. Electron–hole pairs are created inside the solar cell as a result of absorption of the photons incident on the solar cell from the sun. The objective is to collect the minority carriers before they are lost to recombination.

3.4.7 Lifetime and Surface Recombination Effects

The solar cell characteristics previously derived (equations 3.118 through 3.128) allow examination of the dependence of the solar cell performance on specific sources of recombination. Figure 3.17 shows how the base minority-carrier lifetime affects V_{OC}, I_{SC}, and the FF. Unless otherwise stated, the parameters of Table 3.2 are used to compute the solar cell performance. Short lifetimes mean that the diffusion length in the base is much less than the base thickness and carriers created deeper than about one diffusion length in the base are unlikely to be collected. When this is true ($L_n \ll W_P$), the contribution to the dark saturation current in the base (equation 3.128) becomes

$$I_{o1,n} = qA\frac{n_i^2}{N_A}\frac{D_n}{L_n} \tag{3.141}$$

and is commonly referred to as the *long-base approximation*. In this case, the BSF has no effect on the dark saturation current. On the other hand, when the base minority-carrier lifetime is long ($L_n \gg W_P$), the carriers readily come in contact with the BSF and the dark saturation current is a strong function of S_{BSF}

$$I_{o1,n} = qA\frac{n_i^2}{N_A}\frac{D_n}{(W_P - x_P)}\frac{S_{BSF}}{S_{BSF} + D_n/(W_P - x_P)} \tag{3.142}$$

When S_{BSF} is very large (i.e. no BSF), this reduces to the more familiar short-base approximation

$$I_{o1,n} = qA\frac{n_i^2}{N_A}\frac{D_n}{(W_P - x_P)}. \tag{3.143}$$

Figure 3.18 shows how S_{BSF} affects V_{OC}, I_{SC}, and the FF. Notice that the break point in the curves occurs when $S_{BSF} \approx D_n/W_P = 1000$ cm/s, as can be inferred from equation (3.142).

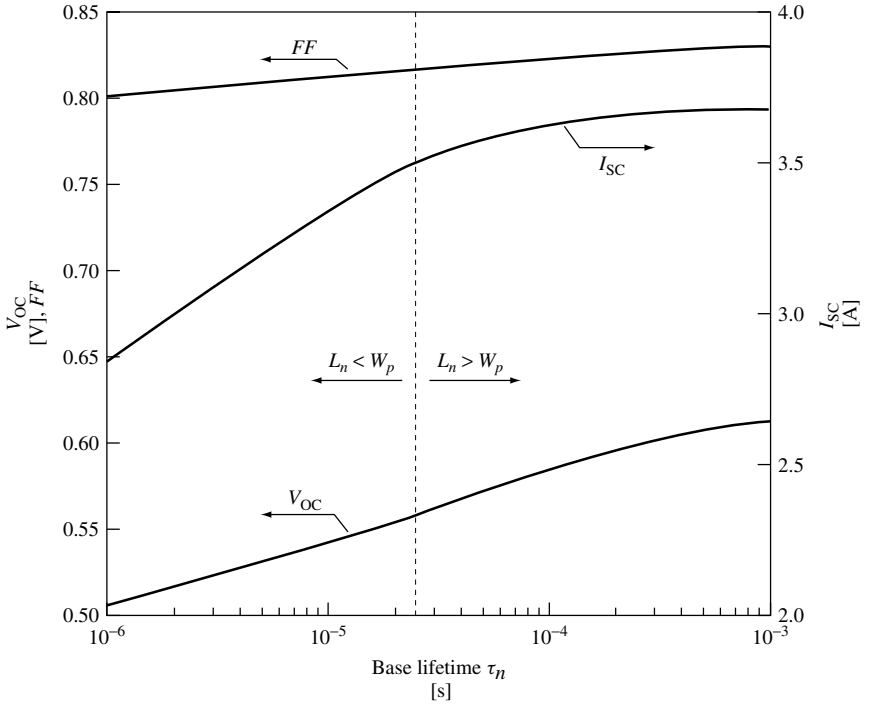

Figure 3.17 Effect of base lifetime on solar cell performance for the solar cell parameters in Table 3.2. The minority-carrier diffusion length ($L_n = \sqrt{D_n \tau_n}$) is equal to the base thickness (W_P) when $\tau_n = 25.7\ \mu s$

Front surface recombination for solar cells with contact grids on the front of the device is really an average over the front surface area of the relatively low surface recombination velocity between the grid lines and the very high surface recombination velocity of the ohmic contact. An expression for the effective front surface recombination velocity is given by [16]

$$S_{\text{F,eff}} = \frac{(1-s)S_{\text{F}}\overline{G}_N\tau_p\left(\cosh\dfrac{W_N}{L_p}-1\right)+p_o(e^{qV/A_okT}-1)\left[s\dfrac{D_p}{L_p}\dfrac{\cosh\dfrac{W_N}{L_p}}{\sinh\dfrac{W_N}{L_p}}+S_{\text{F}}\right]}{(1-s)\left[p_o(e^{qV/A_okT}-1)+\overline{G}_N\tau_p\left(\cosh\dfrac{W_N}{L_p}-1\right)\right]} \tag{3.144}$$

where S_{F} is the surface recombination velocity between the grid lines and $\overline{G}$ is the average generation rate in the emitter region. It is obvious that $S_{\text{F,eff}}$ is dependent upon the solar cell operation point. This is better seen in Table 3.3 where some special cases are illustrated (assuming $L_p \gg W_N$).

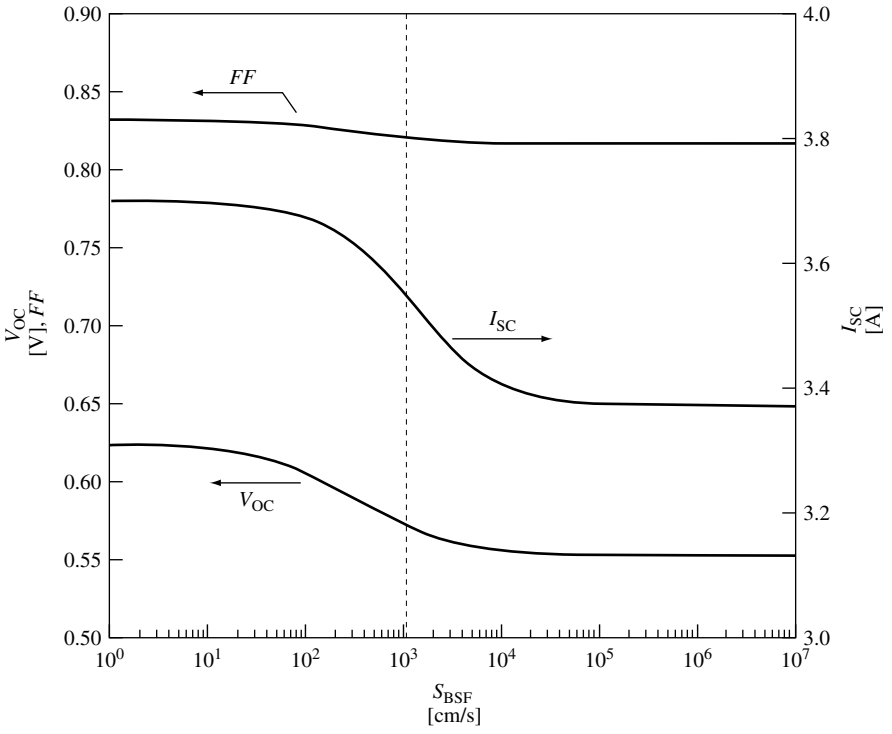

Figure 3.18 Effect of the back-surface field recombination velocity on solar cell performance. All other parameters are from Table 3.2

Table 3.3 Special cases of $S_{F,eff}$

No grid ($s = 0$)	$S_{F,eff} = S_F$
Full grid ($s = 1$)	$S_{F,eff} \rightarrow \infty$
Dark ($\overline{G} = 0$)	$S_{F,eff} = \dfrac{S_F + sD_p/W_N}{1 - s}$
Short circuit (V = 0)	$S_{F,eff} = S_F$
V large ($\approx V_{OC}$)	$S_{F,eff} = \dfrac{S_F + sD_p/W_N}{1 - s}$

3.4.8 An Analogy for Understanding Solar Cell Operation: A Partial Summary

The following analogy illustrates the importance of minimizing all sources of recombination in the solar cell.[4] Imagine a funnel that has a variety of holes of different shapes and sizes in it. It also has a stopcock at the bottom for controlling the flow of liquid

[4] This analogy was developed on the basis of discussions with Professor Richard J. Schwartz of Purdue University, West Lafayette, Indiana.

through the bottom of the funnel. Water, representing the incident sunlight, is poured into the top of the funnel. Water flowing out of the funnel through the stopcock represents the current delivered by the solar cell. Since the funnel is full of holes, some of the water leaks out instead of flowing through the stopcock. This leakage represents the recombination of minority carriers in the solar cell. The different-shaped holes represent different sources of recombination. For instance, square holes might represent recombination in the base region, round holes might be recombination in the space-charge region, triangular holes might be surface recombination at the back contact, and so on. The rate at which water pours in is proportional to the light intensity. At steady state, the water will find a height such that the flow of water in, I_{gen}, is equal to the flow through the stopcock (I) plus the water that leaks through the holes (I_{recomb}). This height represents the solar cell voltage (V).

When the stopcock is fully open, the water flows out through the stopcock at its maximum rate (I_{SC}), although some water will leak out through the holes so that $I_{\text{SC}} < I_{\text{gen}}$. This is analogous to the collection efficiency, η_{C}, of a solar cell – the objective being to minimize the amount of leakage (recombination) so that η_{C} is as close to unity as possible. Smaller holes means less recombination and $I_{\text{SC}} \rightarrow I_{\text{gen}}$.

As the stopcock is slowly closed, the level of liquid in the funnel rises – just as the solar cell voltage increases as the current decreases. When the stopcock is completely closed, the height of the water is representative of the open-circuit voltage (V_{OC}). At open circuit all the minority carriers must recombine just as all the water must leak out of the funnel in this analogy. If the holes are all big, the height of the water will be low. This is equivalent to short minority-carrier lifetimes and large surface recombination velocities that result in a low V_{OC}. By reducing the size of the holes (i.e. increasing the minority-carrier lifetimes and reducing the surface recombination velocities), the height of the water in the funnel (i.e. V_{OC}) is increased. Reducing the size of only the square holes (by increasing the minority-carrier lifetime in the base) will not increase the height of the water as much as might be expected since the round holes (recombination in the depletion region) are still large. All leaks (recombination sources) must be plugged (recombination rates minimized) before the height of the water (V_{OC}) increases substantially.

3.5 ADDITIONAL TOPICS

3.5.1 Efficiency and Band gap

Since only photons with $h\nu > E_{\text{G}}$ can create electron – hole pairs and contribute to the output of the solar cell, it is obvious that the band gap determines how well the solar cell is coupled to the solar spectrum. A simple analysis can be performed to predict the maximum solar cell efficiency. More complete analyses of the theoretical limits of solar cells are given elsewhere [17–19] and are also discussed in Chapter 4 of this handbook. Assuming the maximum energy that can be extracted from an absorbed photon is E_{G}, the maximum efficiency can be expressed as

$$\eta_{\max}(E_{\text{G}}) = \frac{\frac{1}{q}E_{\text{G}}I_{\text{inc}}}{P_{\text{in}}} = \frac{E_{\text{G}}}{(P_{\text{in}}/A)}\int_{\lambda<\lambda_{\text{G}}} f(\lambda)\,\mathrm{d}\lambda. \tag{3.145}$$

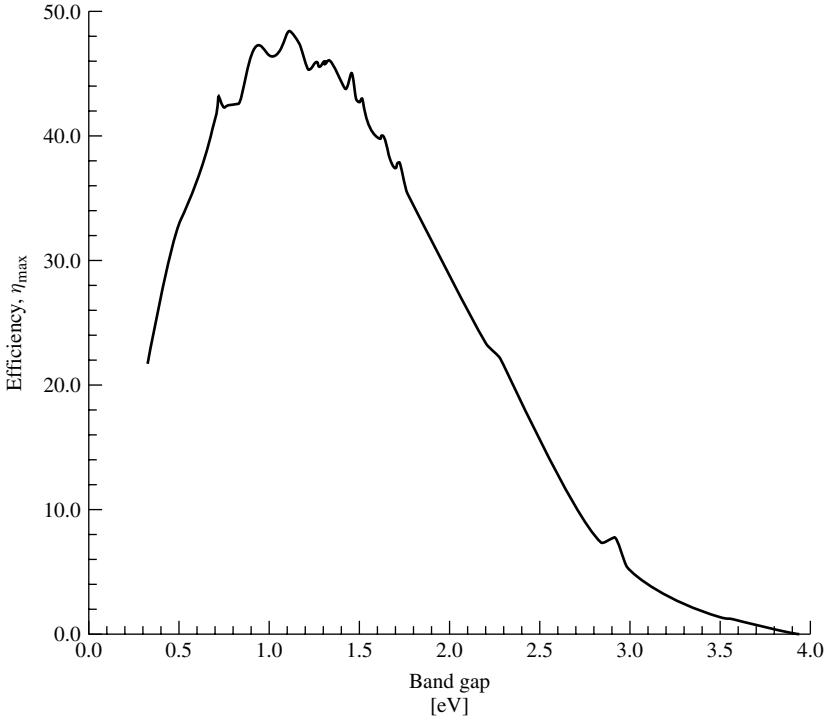

Figure 3.19 Theoretical maximum efficiency as a function of semiconductor band gap for an AM1.5 global spectrum

This is plotted in Figure 3.19 for an AM1.5 global spectrum and shows a maximum efficiency of 48% at about $E_G = 1.1$ eV, close to the band gap of silicon. Of course, this is only a simple estimate and assumes that $V_{OC} = 1/qE_G$ and $FF = 1$, which are obvious exaggerations. Perfect light trapping was also assumed so that $I_{SC} = I_{inc}$, but that is a more realistic prospect. Under nonconcentrated solar illumination, the actual maximum theoretical efficiency for a silicon solar cell is approximately 30%. However, this simple approach does serve to demonstrate the important role the semiconductor band gap plays in determining solar cell performance and shows that band gaps between 1.0 and 1.6 eV have nearly equivalent maximum theoretical efficiencies.

3.5.2 Spectral Response

The spectral response, $SR(\lambda)$, of a solar cell permits an examination of how photons of different wavelengths (energy) contribute to the short-circuit current. Just as the collection efficiency can be measured as either an external or an internal collection efficiency, so can the spectral response. The spectral response is defined as the *short-circuit current*, $I_{SC}(\lambda)$, resulting from a single wavelength of light normalized by the maximum possible current. The external spectral response is defined as

$$SR_{ext} = \frac{I_{SC}(\lambda)}{qAf(\lambda)} \tag{3.146}$$

and the internal spectral response as

$$SR_{\text{int}} = \frac{I_{\text{SC}}(\lambda)}{qA(1-s)(1-r(\lambda))f(\lambda)(e^{-\alpha(\lambda)W_{\text{opt}}}-1)}, \tag{3.147}$$

where W_{opt} is the optical thickness of the solar cell (technically, also a function of wavelength). Experimentally, the external spectral response is measured. The internal spectral response is determined from it along with the knowledge of the grid shadowing, reflectance, and optical thickness. W_{opt} can be greater than the cell thickness if light-trapping methods are used. Such methods include textured surfaces [20] and back-surface reflectors [21] and are discussed in Chapter 8. The short-circuit current can be written in terms of the external spectral response as

$$I_{\text{SC}} = \int_{\lambda} SR_{\text{ext}}(\lambda) f(\lambda)\, d\lambda. \tag{3.148}$$

The internal spectral response gives an indication of which sources of recombination are affecting the cell performance. This is demonstrated in Figure 3.20 where the internal spectral response of the silicon solar cell described by the parameters of Table 3.2 is shown. Also shown is the spectral response when $S_{\text{F,eff}} = 100$ cm/s (a passivated front surface) and the spectral response when $S_{\text{BSF}} = 1 \times 10^7$ cm/s (in effect, no BSF). The short wavelength response improves dramatically when the front surface is passivated

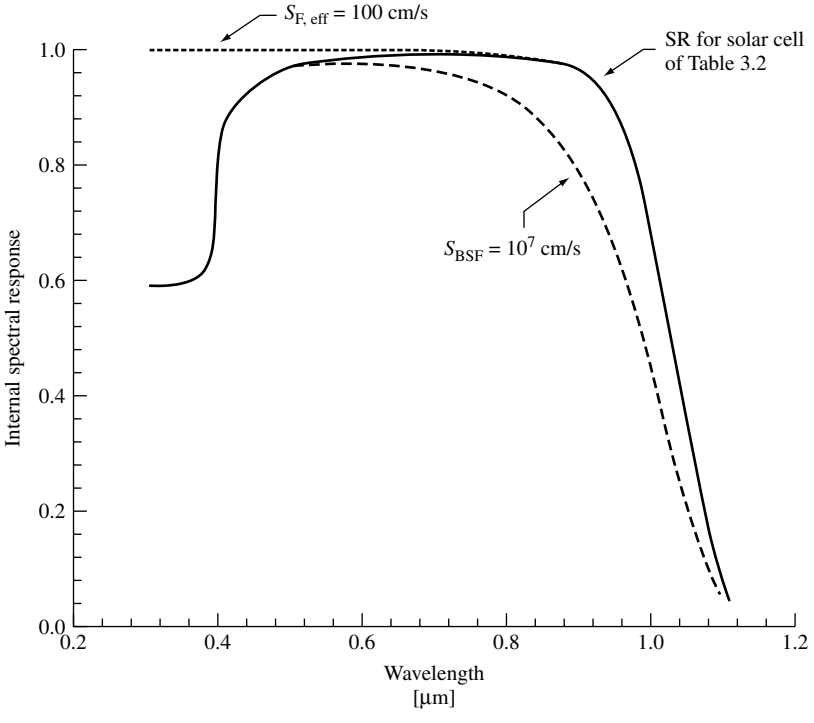

Figure 3.20 Internal spectral response of the silicon solar cell defined in Table 3.2

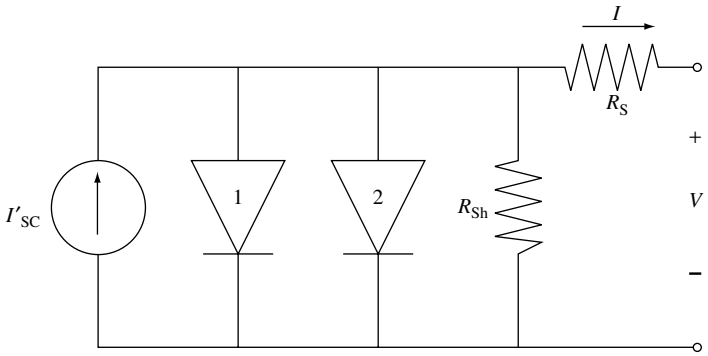

Figure 3.21 Solar cell circuit model including the parasitic series and shunt resistances

since the absorption coefficient is highest for short wavelength (high energy) photons. Conversely, removing the BSF makes it more likely that electrons created deep within the base region of the solar cell (those created by the long wavelength, low-energy photons) will recombine at the back contact and therefore, the long wavelength response is dramatically reduced.

3.5.3 Parasitic Resistance Effects

Equation (3.130) neglects the parasitic series and shunt resistances typically associated with real solar cells. Incorporating these resistances into the circuit model of Figure 3.15, as shown in Figure 3.21, yields

$$I = I'_{SC} - I_{o1}(e^{q(V+IR_S)/kT} - 1) - I_{o2}(e^{q(V+IR_S)/2kT} - 1) - \frac{(V + IR_S)}{R_{Sh}} \tag{3.149}$$

where I'_{SC} is the short-circuit current when there are no parasitic resistances. The effect of these parasitic resistances on the $I-V$ characteristic is shown in Figures 3.22 and 3.23. As can also be seen in equation (3.149), the shunt resistance, R_{Sh}, has no effect on the short-circuit current, but reduces the open-circuit voltage. Conversely, the series resistance, R_S, has no effect on the open-circuit voltage, but reduces the short-circuit current. Sources of series resistance include the metal contacts, particularly the front grid, and the transverse flow of current in the solar cell emitter to the front grid.

It is often more convenient to rewrite equation (3.149) as

$$I = I'_{SC} - I_o(e^{q(V+IR_S)/A_okT} - 1) - \frac{(V + IR_S)}{R_{Sh}} \tag{3.150}$$

where A_o is the diode ideality (quality) factor and typically has a value between 1 and 2, with $A_o \approx 1$ for diode dominated by recombination in the quasi-neutral regions and $A_o \to 2$ when recombination in the depletion region dominates. In solar cells where the

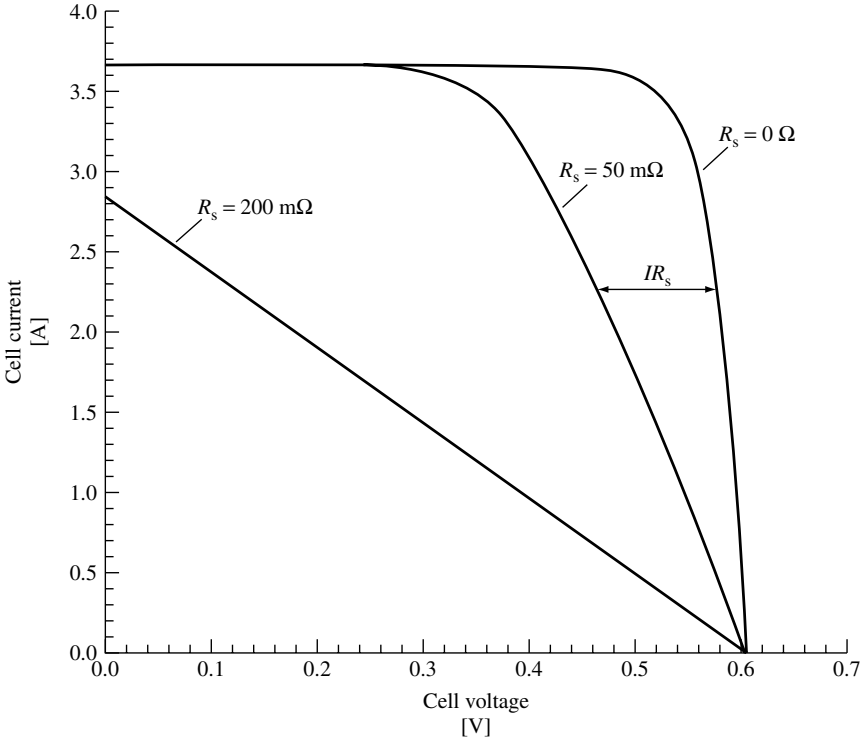

Figure 3.22 Effect of series resistance on the current–voltage characteristic of a solar cell ($R_{\mathrm{Sh}} \to \infty$)

recombination in each region is comparable, A_o is somewhere in-between. At short circuit, equation (3.150) becomes

$$I_{\mathrm{SC}} = I'_{\mathrm{SC}} - I_o(\mathrm{e}^{qI_{\mathrm{SC}}R_{\mathrm{S}}/A_okT} - 1) - I_{\mathrm{SC}}R_{\mathrm{S}}/R_{\mathrm{Sh}} \tag{3.151}$$

and at open circuit, it becomes

$$0 = I'_{\mathrm{SC}} - I_o(\mathrm{e}^{V_{\mathrm{OC}}/A_okT} - 1) - V_{\mathrm{OC}}/R_{\mathrm{Sh}}. \tag{3.152}$$

When $\log(I_{\mathrm{SC}})$ is plotted versus V_{OC} (where I_{SC} and V_{OC} are obtained over a range of illumination intensities), there is typically a regime where neither the series nor shunt resistances are important, as illustrated in Figure 3.24. The slope of this line will yield the diode ideality factor A_o, while the y-intercept will give I_o. In the regime where only series resistance is important, equations (3.151) and (3.152) can be combined to give

$$I_{\mathrm{SC}}R_{\mathrm{S}} = \frac{A_okT}{q} \ln\left[\frac{I_o\mathrm{e}^{qV_{\mathrm{OC}}/A_okT} - I_{\mathrm{SC}}}{I_o}\right] \tag{3.153}$$

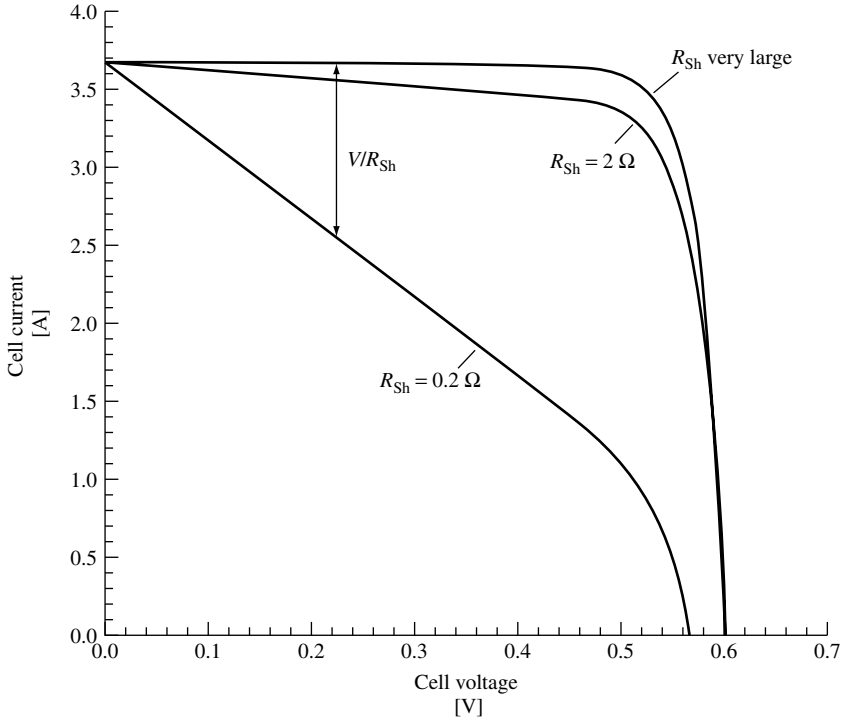

Figure 3.23 Effect of shunt resistance on the current–voltage characteristic of a solar cell ($R_S = 0$)

and a plot of I_{SC} versus $\log[I_o e^{qV_{OC}/A_o kT} - I_{SC}]$ will then permit R_S to be extracted from the slope of this line. Similarly, in the regime where only R_{Sh} is important, equations (3.151) and (3.152) can be combined to give

$$\frac{V_{OC}}{R_{Sh}} = I_{SC} - I_o e^{qV_{OC}/A_o kT} \tag{3.154}$$

and R_{Sh} can be determined from the slope of the line given by plotting V_{OC} versus $[I_{SC} - I_o e^{qV_{OC}/A_o kT}]$. If the series and shunt resistances are such that there is no regime where they can be neglected, the parameters can, with patience, be extracted through the process of trial and error.

3.5.4 Temperature Effects

From equations (3.127) and (3.128), it is apparent that

$$I_{o1,n},\ I_{o1,p} \propto n_i^2 \tag{3.155}$$

and from equation (3.129) that

$$I_{o2} \propto n_i. \tag{3.156}$$

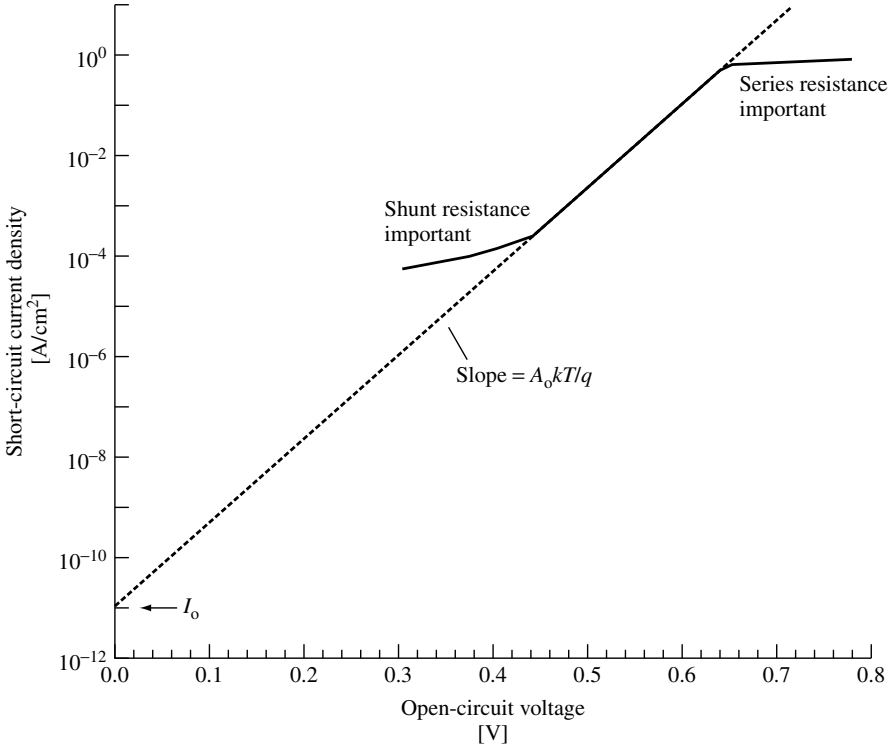

Figure 3.24 Short-circuit current versus open-circuit voltage plot illustrating parameter extraction

An increase in the intrinsic carrier concentration increases the dark saturation (recombination) current and results in a decrease in the open-circuit voltage, as can be seen from equation (3.140). The dark saturation current contains other temperature-dependent terms (D, τ, and S), but the temperature dependence of the intrinsic carrier concentration dominates. The intrinsic carrier concentration is given by equation (3.18), which when combined with equations (3.13) and (3.14) yields

$$n_{\mathrm{i}} = 2(m_n^* m_p^*)^{3/4} \left(\frac{2\pi kT}{h^2}\right)^{3/2} \mathrm{e}^{-E_{\mathrm{G}}/2kT}. \tag{3.157}$$

The effective masses are generally taken to be weak functions of temperature. The band gap decreases with temperature and its temperature dependence is well modeled by

$$E_{\mathrm{G}}(T) = E_{\mathrm{G}}(0) - \frac{aT^2}{T+\beta}. \tag{3.158}$$

where α and β are constants specific to each semiconductor. It is clear that as the temperature increases, n_{i} increases, and thus recombination increases, and cell performance is impaired. Band gap narrowing, referred to earlier, is a reduction in band gap due to high doping and also serves to increase n_{i} and impair solar cell performance.

The open-circuit current expression, equation (3.140), can be rearranged and the temperature dependence explicitly included to give

$$I_{SC} \approx I_{o1} e^{qV_{OC}/kT} \approx BT^{\zeta} e^{-E_G(0)/kT} e^{qV_{OC}/kT} \tag{3.159}$$

where B is a temperature-independent constant and $T^{\zeta} e^{-E_G(0)/kT}$ accounts for the temperature dependence of the saturation current. The short-circuit current is relatively unaffected by temperature under typical operating conditions, so by differentiating with respect to T, the temperature dependence of the open-circuit voltage can be expressed as [15]

$$\frac{dV_{OC}}{dT} = -\frac{\frac{1}{q}E_G(0) - V_{OC} + \zeta\frac{kT}{q}}{T} \tag{3.160}$$

which for silicon at 300 K corresponds to about -2.3 mV/°C. Equation (3.159) can be rearranged as follows:

$$V_{OC}(T) = \frac{1}{q}E_G(0) - \frac{kT}{q}\ln\left(\frac{BT^{\zeta}}{I_{SC}}\right). \tag{3.161}$$

V_{OC} varies roughly linearly and inversely with temperature and an extrapolation of V_{OC} to $T = 0$ is approximately the band gap since $\lim_{T\to 0}[T \ln T] = 0$.

3.5.5 Concentrator Solar Cells

Operating solar cells under concentrated illumination offers two main advantages. The first is that since fewer solar cells are required to collect the sunlight falling on a given area, their cost of manufacture can be higher than that for cells designed for nonconcentrated illumination, and they are therefore presumably of higher quality (efficiency). The second is that operation under concentrated illumination offers an advantage in the solar cell efficiency. If sunlight is concentrated by a factor of X (X sun illumination), the short circuit at that concentration is

$$I_{SC}^{Xsuns} = XI_{SC}^{1sun}. \tag{3.162}$$

This is assuming that the semiconductor parameters are unaffected by the illumination level and that the cell temperature is the same at both levels of illumination – not necessarily valid assumptions especially at very large X, that is, X > 100. However, these assumptions will allow the demonstration of the potential efficiency of concentrator solar cells. Substituting equation (3.162) into equation (3.135) gives

$$\eta = \frac{FF^{Xsuns}V_{OC}^{Xsuns}I_{SC}^{Xsuns}}{P_{in}^{Xsuns}} = \frac{FF^{Xsuns}V_{OC}^{Xsuns}XI_{SC}^{1sun}}{XP_{in}^{1sun}} = \frac{FF^{Xsuns}V_{OC}^{Xsuns}I_{SC}^{1sun}}{P_{in}^{1sun}} \tag{3.163}$$

From equation (3.131),

$$V_{OC}^{Xsuns} = V_{OC}^{1sun} + \frac{kT}{q}\ln X. \tag{3.164}$$

The FF is a function of V_{OC} (equation 3.134), so

$$\eta^{\text{Xsuns}} = \eta^{\text{1sun}} \left(\frac{FF^{\text{Xsuns}}}{FF^{\text{1sun}}} \right) \left(1 + \frac{\dfrac{kT}{q} \ln \text{X}}{V_{\text{OC}}^{\text{1sun}}} \right). \tag{3.165}$$

Both factors multiplying the 1 sun efficiency increase as the illumination concentration increases. Therefore, the efficiency of concentrator cells increases as the illumination concentration increases, as shown in Figure 3.25.

Of course, there are many obstacles to achieving this. Concentrator cells must be cooled, since an increase in operating temperature reduces V_{OC}, and hence the cell efficiency. The FF^{Xsuns} eventually decreases with increasing X and current due to the parasitic series resistance. Concentrator solar cells are discussed in more detail in Chapter 11.

3.5.6 High-level Injection

In high-level injection, the excess carrier concentrations greatly exceed the doping in the base region, so $\Delta p \approx \Delta n \approx n \approx p$ if the carriers are moving generally in the same direction. This occurs with back-contact solar cells, such as the silicon point-contact solar

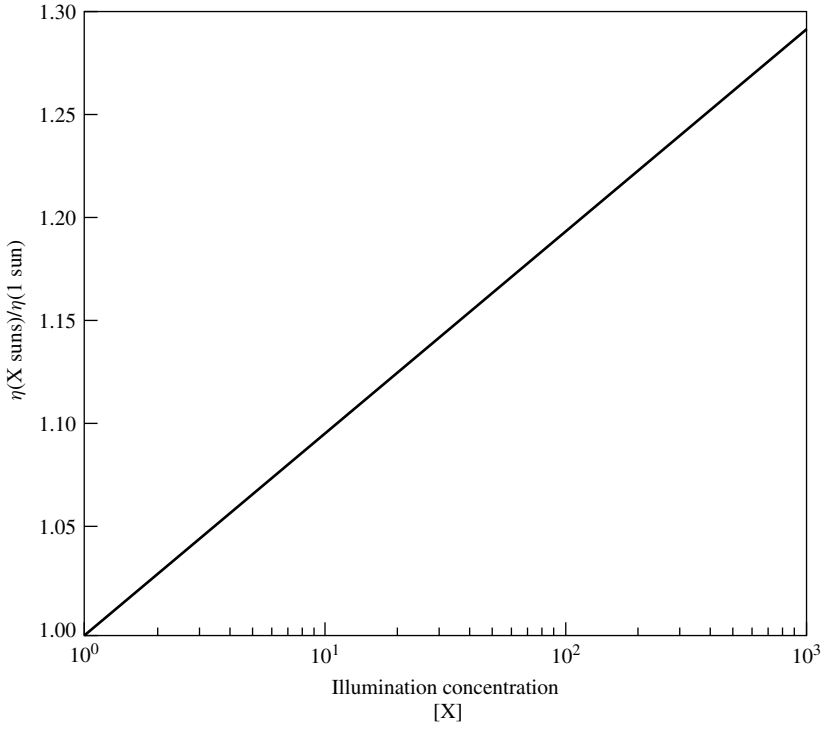

Figure 3.25 Relative efficiency as a function of illumination concentration

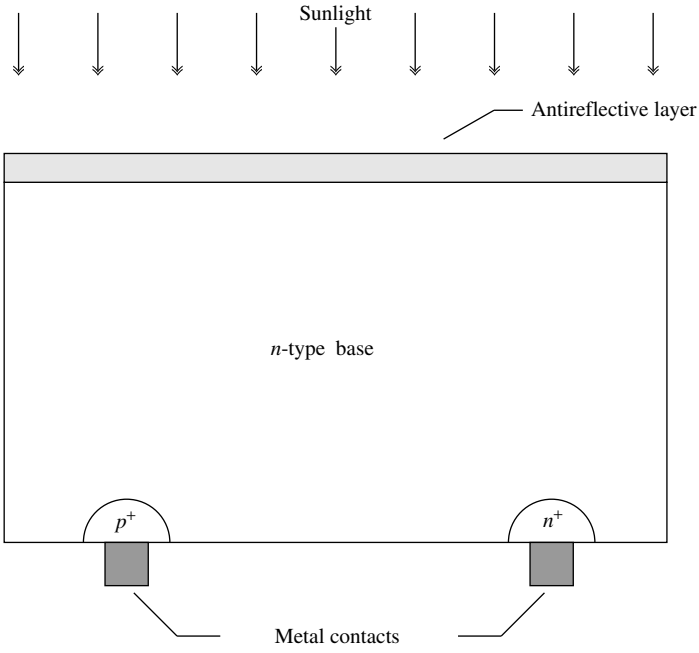

Figure 3.26 Schematic of a back-contact solar cell

cell [22], as illustrated in Figure 3.26. Since both electrical contacts are on the back, there is no grid shadowing. These cells are typically used in concentrator application and high-level injection conditions pervade. Assuming high-level injection, a simple analysis is possible.

Returning to equations (3.76) and (3.77), it can be seen that in high-level injection, the electric field can be eliminated (it is not necessarily zero), resulting in the ambipolar diffusion equation

$$D_{\mathrm{a}}\frac{\mathrm{d}^2 p}{\mathrm{d}x^2} - \frac{p}{\tau_n + \tau_p} = -G(x), \tag{3.166}$$

where the ambipolar diffusion coefficient is given by

$$D_{\mathrm{a}} = \frac{2D_n D_p}{D_n + D_p}. \tag{3.167}$$

The ambipolar diffusion coefficient is always less than the larger diffusion coefficient and greater than the smaller one.

In silicon, where $D_n/D_p \approx 3$ over a wide range of doping, the ambipolar diffusion coefficient is $D_{\mathrm{a}} \approx 3/2D_p \approx 1/2D_n$ and, if we also assume $\tau_p \approx \tau_n$, the ambipolar diffusion length is

$$L_{\mathrm{a}} \approx \sqrt{3}L_p \approx L_n. \tag{3.168}$$

Thus, the increased high-injection lifetime (see equation 3.40) offsets the reduced ambipolar diffusion coefficient.

It is crucial that the front surface of a back-contacted cell be well passivated, so we will assume that $S_F = 0$. We will further assume that optical generation is uniform throughout the base region. At open circuit, with these assumptions, $d^2p/dx^2 = 0$ and therefore

$$V_{OC} = \frac{2kT}{q} \ln\left[\frac{G(\tau_n + \tau_p)}{n_i}\right]. \tag{3.169}$$

The short-circuit current (with $p \simeq 0$ at the back of the cell) is

$$I_{SC} = qAL_aG \sinh(W_B/L_a) \tag{3.170}$$

which, when $L_a \gg W_B$, becomes

$$I_{SC} = qAW_BG. \tag{3.171}$$

3.5.7 *p-i-n* Solar Cells

The *p-i-n* solar cell takes advantage of the fact that in many semiconductor materials, especially direct band gap semiconductors (i.e. large absorption coefficient), most of the electron–hole pairs are created very near the surface. If an intrinsic (undoped) layer is placed between the (very thin) *n* and *p* regions, the depletion region thickness is the most significant fraction of the total solar cell thickness, as illustrated in Figure 3.27. Carrier collection is now aided by the electric field in the depletion region, which helps offset the low lifetimes in some materials, such as amorphous silicon (see Chapter 12). The $I-V$ characteristic of a *p-i-n* solar cell can be described with minor modifications to the previously derived expressions. The most significant modification is to equation (3.129) where the depletion width is now written as

$$W_D = \chi_N + W_I + \chi_P \tag{3.172}$$

where W_I is the thickness of the intrinsic layer. Since χ_N and χ_P are very thin, short-base approximations are in order for equations (3.127) and (3.128). Also, there is no BSF ($S_{BSF} \to \infty$).

3.5.8 Detailed Numerical Modeling

While analytic solutions such as those discussed thus far in this chapter provide an intuitive understanding of solar cell performance and are therefore very important, they are limited in their accuracy due to the many simplifying assumptions that must be made in order to obtain them. It is rather straightforward to solve the semiconductor equations numerically without the need to make so many simplifications. Several computer codes have been written that solve the semiconductor equations for the explicit purpose of modeling solar cells – PC-1D [23], AMPS [24], ADEPT [25], and its predecessors [16, 26, 27], for example. The basic design of these computer programs is very similar. The semiconductor

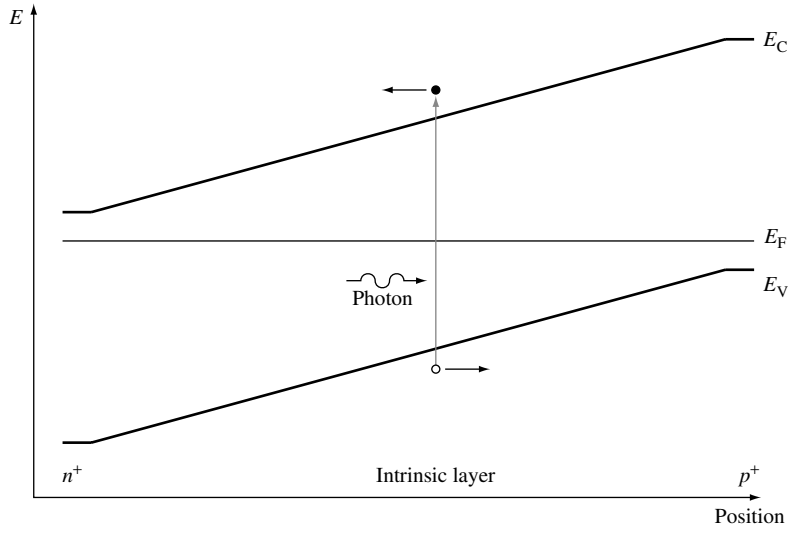

Figure 3.27 Band diagram of a *p-i-n* solar cell illustrating field-enhanced collection

equations (three coupled nonlinear partial differential equations) are cast in a normalized form [28] to simplify the calculations. Finite difference or finite element methods are then used to discretize the equations on a mesh (grid), resulting in a set of three coupled nonlinear difference equations. Using appropriately discretized boundary conditions, these equations are solved iteratively using a generalized Newton method to obtain the carrier concentrations and electric potential at each mesh point. Each Newton iteration involves the solution of a very large matrix equation or order $3N$, where N is the number of mesh points. One-dimensional simulations typically utilize on the order of 1000 mesh points, so the matrix is 3000×3000. In 2D, the minimum mesh is typically at least 100×100, so $N = 10^4$ and the matrix is of order 3×10^4 and contains 9×10^8 elements. Fortunately, the matrices are sparse and can be solved using considerably less computer memory than one would expect at first glance.

Numerical simulation allows analysis of solar cell designs and operating conditions for which simple analytic expressions are inadequate. The necessity of ignoring the spatial variation of parameters is eliminated and more accurate representations of the solar cell are possible. In particular, nonuniform doping, heterojunction solar cells (band gap varies spatially), amorphous silicon solar cells (complex trapping/recombination mechanisms, field-assisted collection), and concentrator solar cells (high-level injection, 2D/3D effects) can all be modeled with more precision.

3.6 SUMMARY

It has been the objective of this chapter to give the reader a basic understanding of the physical principles that underlie the operation of solar cells. Toward that end, the fundamental physical characteristics of solar cell materials that permit the conversion of light into electricity have been reviewed. These characteristics include the ability of

semiconductors to absorb photons by conferring that energy to carriers of electrical current and the ability of semiconductor materials to conduct electricity.

The basic operating principles of the solar cell (a carefully designed *pn*-junction diode) were derived from the (simplified) equations describing the dynamics of holes and electrons in semiconductors. This led to the definition of the solar cell figures of merit – the open-circuit voltage (V_{OC}), the short-circuit current (I_{SC}), the fill factor (FF), and the cell efficiency (η). The two key factors determining solar cell efficiency – electron–hole pair generation and recombination – were identified and discussed. In particular, the need to minimize all sources of recombination in the solar cells was demonstrated through examples and by way of a simple analogy.

The importance of matching the band gap of the solar cell material to the solar spectrum was also discussed and it was shown that silicon, with a band gap of 1.12 eV, is an excellent match to the solar spectrum. The effects of parasitic resistances and temperature on solar cell performance were examined and, finally, some advanced cell concepts were briefly introduced. Many of these topics will be expanded upon in the following chapters of this handbook.

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6

Bulk Crystal Growth and Wafering for PV

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6.1 INTRODUCTION

The workhorse of the photovoltaics industry is silicon. More than four out of five amperes of solar-module produced current come from crystalline silicon modules. Of this amount, over 50% is produced by a steadily increasing share from multicrystalline silicon material.

Silicon solar cells first were made about 50 years ago from Czochralski (Cz)-pulled monocrystals with technology adapted from the microelectronics industry. Subsequently, world-record cell efficiencies have been achieved at a very high cost on a laboratory scale with Float Zone (FZ) monocrystals.

Cost pressures have forced the development of multicrystalline material solidification processes for production of very large silicon ingots (blocks), which have reached typical sizes of 250 kg in 2000. A good theoretical understanding of growth processes, together with numerical simulations of the entire process down to a microstructural defect level in the crystal today has resulted in the economical production of high-quality material. Sawing of silicon crystal into the thin wafers required for the best performance in solar cells wastes about 50% of expensive, pure silicon feedstock and is very costly. This has led to the development of several crystalline silicon foil, that is, ribbon production processes, and these are now in various stages of R&D and commercialization.

Handbook of Photovoltaic Science and Engineering. Edited by A. Luque and S. Hegedus
 ISBN: 0-471-49196-9

6.2 BULK MONOCRYSTALLINE MATERIAL

The dominant issue of the photovoltaic industry is to fabricate solar cells in large volumes that are both highly efficient and cost-effective. An overall industrial goal is to significantly lower the costs per watt. The dominant absorber material used today for the majority of the commercially produced solar cells is the Czochralski-grown crystalline silicon (c-Si) in monocrystalline and block-cast material in multicrystalline form (mc-Si). Up to now, a lot of effort has been undertaken to increase the electrical efficiency of solar cells reproducibly towards and even above 20% [1], whereas much higher efficiencies were indeed claimed [2] but were most probably never reached [3]. Unfortunately, efficiency improvements are often reached only with the help of cost-intensive process steps so that most steps cannot be directly implemented into industrial products but have to be reengineered for low-enough cost. Hence, there still remains a significant efficiency gap between monocrystalline laboratory cells with efficiencies up to 24% and cost-effective, commercial Cz solar cells that are presently produced and sold in high volume at approximately 14 to 17% efficiency.

While some years ago the cost of a module was driven almost equally by the cost of the wafer (33%), the cell process (33%) and the module making (33%), this well-known ratio has changed significantly – both for C-Si and mc-Si. Today, in most products the wafer attributes to sometimes more than 50% (!) of the module cost, whereas the cell process and the module process attribute to the rest with similar portions of ∼25%. The main reason for this is on one hand a steady cost reduction in the cell and module processes and on the other hand a significant increase in feedstock price together with an almost unchanged wafer thickness of 250 to 350 μm in production.

One way to meet today's demand of lower wafer cost is to (1) reduce the cost of crystal growth by improvement of productivity and material consumption at constant wafer quality, (2) reduce the cost of the wire-sawing process and (3) cut thinner wafers. While commercial Si solar cells still have a present wafer thickness of 250 to 350 μm for reasons of mechanical stability, a thickness of only 60 to 100 μm has been calculated to be the physical optimum thickness for silicon solar cells [4]. In this thickness regime the maximum theoretical efficiency for c-Si solar cells can be reached. In this optimum thickness regime, however, monocrystalline silicon becomes very fragile so that not only the electronic but also the mechanical properties of the wafer as well as the handling and processing techniques become of utmost importance for a good overall fabrication yield. Besides the mere mechanical wafer stability, manufacturing processes have to be adapted, redesigned or newly developed to avoid bending and breaking of ultra-thin wafers. With reduced wafer thickness, the necessity for surface passivation has to be taken into account. Since this cannot be done without adding to the cost, any added process step has to add adequate efficiency to remain cost-effective. Other important issues to get as much efficiency as possible out of the "valuable" wafer are improvements in anti-reflection (AR) coating, grid shadowing, "blue" response of the emitter and both surface and volume passivation.

The demand for high-quality polysilicon feedstock in the world market grew quickly not only in the microelectronic but also in the photovoltaic industry. In 1980 the worldwide production of single-crystal silicon amounted to approximately 2000 metric tons per year. This number was equivalent to ∼100 000 silicon crystals every year

by either the Czochralski technique (80%) or the floating-zone technique (20%). The PV industry used both the high-quality tops and tails of the microelectronic crystals for less than 5$/kg to fit the feedstock demand and the depreciated Cz pullers of the "big brother" microelectronic industry. Since the microelectronic industry was and is still driven by continuously increasing ingot diameters, the "small" Cz machines became available for the PV-industry at interesting prices. During the last expansion phase of the microelectronic industry (1993–99), the PV industry had to struggle with a severe shortage of affordable feedstock. To reach the production volume, even pot scrap Si material had to be used. New and demanding techniques were developed in a hurry to separate the Si from the quartz crucible parts and to pre-select and pre-clean this material. Also, fine grain material had to be made usable. However, the annual world requirement for solar quality silicon in 2010 is estimated at 8000 to 10 000 metric tons for PV use, that is, the silicon demand will be roughly as high in volume as today's world production for microelectronics. A dedicated Si feedstock supply only for PV is therefore a necessity.

It can no longer be denied that the growing of silicon crystals has matured from an art into a scientific business. In today's PV-business, some of the bigger companies convert more than ~1 to 2 tons of silicon per day into solar grade Cz crystals and solar cells. Since PV has different main requirements for crystal growing from the microelectronic industry, the focus of machine and process development differ.

6.2.1 Cz Growth of Single-crystal Silicon

Solar cells made out of Czochralski (Cz)-grown crystals and wafers play – together with multicrystalline cells – a dominant part in today's PV industry. This is due to the following advantages.

Cz crystals can be grown from a wide variety of differently shaped and doped feedstock material. This enables the PV industry to buy cost-effective feedstock Si with sufficient quality even on spot markets. Since the feedstock is molten in a crucible, the shape, the grain size and the resistivity of the different feedstock materials can be mixed for the required specifications, although a given feedstock alone would fail. However, special care must be taken to avoid any macroscopic particles (SiO_2, SiC) that would not be dissolved in the melt especially when pot scrap material is used.

The Cz process acts as a purification step with respect to lifetime-limiting elements. The effective distribution coefficients of the most dominant lifetime-limiting metals (Fe, Ni, Au, Ti, Pt, Cr) are in the range of 10^{-5} or below. Together with appropriate gettering steps during cell processing, highly efficient commercial solar cells can even be made out of ingots grown from low-grade pot scrap material. The targeted iron equivalent concentration in the finished cell must be $<10^{12}$ atoms/cm^3 to achieve a minority carrier diffusion length well above ~150 μm.

The Cz process itself acts as a quality control step since proper crystallisation, that is, dislocation-free growth of an ingot, can only take place in a well-defined process window. The homogeneity of a well-grown solar grade Cz ingot for PV application is excellent with respect to the bandwidth of electronic and structural properties, whereas mc-Si block casting produces specifications with higher variances in most parameters. Cell

processes with Cz-Si can therefore use high-efficiency processes with smaller process windows that require well-defined starting material.

Cz technology is mature and cost-effective. Equipment and processes for semi-automated growing of crystals are commercially available so that several Cz pullers can be run by a single operator. Owing to the robust making of the machines, many Cz growers more than 20 years age are still in production.

The ingot can be pulled in a defined <100> orientation. This is a big economic advantage since the solar cell process can use this crystallographic property to homogeneously texture solar cells with a very cost-effective wet chemical etching step. By anisotropic etching, a surface structure with random pyramids is built that couples the incoming light very effectively into the solar cell. This effect together with the usually higher diffusion length of Cz crystals gives rise to the increased efficiency of Cz-Si solar cells compared to similarly processed mc-Si cells.

There exists a high potential for increasing the net pulling speed, that is, the productivity of a puller by a clever design of the hot zone, by sophisticated recharging concepts of Si in the hot crucible and by tuning the growth recipe to the optimum pull speed. Here the PV industry is in the novel position that it can neglect most specifications that are required in the microelectronic industry.

This is possible since the PV specifications are strongly reduced in the number of required parameters in contrast to microelectronic material. A PV specification "simply" focuses on the maximum productivity, a minority-carrier diffusion length of the material that should be exceeding the cell thickness and a shallow p-type doping that leads to a specific resistivity between 0.3 and 10 Ωcm, depending on the fabricated solar cell type.

One of the main disadvantages of Cz crystallisation of silicon is the fact that square cells are best suited to built a highly efficient solar module, whereas Cz ingots have a round cross section. In order to use both the crystal and the module area in the best manner, the ingots are usually cut into a pseudosquare cross section before they are cut into wafers. Additionally, the tops and tails of the ingots cannot be used for wafer production. The cropped and slapped materials, that is, tops and tails and so on, are then fed back into the growth process again.

The equipment and the basic principle for Cz pulling is shown in Figure 6.1. The Cz equipment consists of a vacuum chamber in which feedstock material, that is, polycrystalline silicon pieces or residues from single crystals, is melted in a crucible and a seed crystal is first dipped into the melt. Then the seed is slowly withdrawn vertically to the melt surface whereby the liquid crystallises at the seed. High vacuum conditions can be used as long as the melt weight is small (<1–2 kg), but with larger melts (often more than 30 kg) only pulling under argon inert gas stream is practicable. Owing to the reduced argon consumption, the argon pressure is set in the 5 to 50 mbar regime in the PV industry, whereas in the microelectronic industry, atmospheric pressure is also used.

After the silicon is completely molten, the temperature of the melt is stabilised to achieve the required temperature to lower the seed into the melt. The temperature must be chosen so that the seed is not growing in diameter (melt too cold) or decreasing in diameter (melt too hot). In PV the seed is usually <100>-oriented, is monocrystalline and

(a) (b)

Figure 6.1 Cz pullers in a PV-production environment (a) and growing Cz crystal (b) in a quartz crucible

is pulled upwards to grow a "crystal neck". Since dislocations propagate on (111) planes that are oblique in an <100>-oriented crystal, the dislocations grow out of the crystal neck after a couple of centimetres so that the rest of the crystal grows dislocation-free even if the growth was started from a dislocated seed. The dislocation-free state of the grown crystal manifests itself in the development of "ridges" on the crystal surface. If this state is achieved, the diameter of the crystal can be enlarged by slower pulling until it reaches the desired value. The transition region from the seed node to the cylindrical part of the crystal has more or less the shape of a cone and is therefore called the "seed cone". This cone can be pulled differently, either flat or steep.

Shortly before the desired diameter is reached, the pulling velocity is raised to the specific value at which the crystal grows with the required diameter. Owing to the seed rotation, the crystal cross section is mostly circular. In general, the pulling velocity during the growth of the cylindrical part is not kept constant, but is reduced towards the bottom end of the crystal. This is mainly caused by the increasing heat radiation from the crucible wall as the melt level sinks. The heat removal of the crystallisation thus becomes more difficult and more time is needed to grow a certain length of the crystal. Standard pull speeds in the body range from 0.5 to 1.2 mm/min. The diameter of the crystal in PV is often chosen between 100 and 150 mm. This is due to the short-circuit current of big solar cells where values of 6 A per cell are exceeded. It is difficult to provide a proper contacting scheme in screen print technology that can handle such high currents in the front contacts without high series-resistance losses. With even larger cell sizes, this effect becomes more problematic.

To complete the crystal growth free of dislocations, the crystal diameter has to be reduced gradually to a small size, whereby an end cone develops. For this purpose, the pulling speed is raised and the crystal diameter is decreased. If the diameter is small enough, the crystal can be separated from the melt without a dislocation forming in the cylindrical part of the crystal. The withdrawal of the crystal from the residual melt can be done with a rather high velocity, but not too fast, because thermal shock would cause plastic deformation called "slip" in the lower part of the crystal. The final crystal length is dependent on the crucible charge and varies between 40 and 150 cm.

Nowadays, the seed crystals used for Cz crystal growth are usually dislocation-free. However, each time the seed crystal is dipped into the melt, dislocations are generated by the temperature shock and by surface tension effects between the melt and the crystal. Normally these dislocations are propagated, or move into the growing crystal, particularly if the crystals have large diameters. The movement of dislocations is affected by cooling strain and faulty crystal growth.

The strain that occurs as a result of different cooling rates between the inner and the outer parts of the crystal is probably the main reason for the dislocation movement in the case of large crystals. At the usual <100>-crystal orientation, no (111) lattice plane, that is, no main glide plane, extends parallel to the crystal axis. All (111) glide planes are oblique to the crystal axis and as a result all dislocations that move only on one glide plane are conducted out of the crystal at some time. For movement in the pulling direction, the dislocations have to move downwards in a zigzag motion using at least two of the four different (111) glide planes. Dislocation-free crystal growth is relatively stable even for large crystal diameters, in spite of the higher cooling strain. This is so because it is difficult for a perfect crystal to generate a first dislocation. However, if a first dislocation has been formed, it can multiply and move into the crystal. In this way, numerous dislocations are generated and spread out into the crystal until the strain becomes too low for further movement of dislocations. Therefore, if a dislocation-free growing crystal is disturbed at one point, the whole cross section and a considerable part of the already-grown good crystal are inundated with backward-moving slip dislocations. The length of the slip-dislocated area is approximately equal to the diameter. Wafers and cells that show these types of dislocations can easily be hydrogen-passivated.

After losing the dislocation-free state, the crystal continues to grow with a high density of dislocations that usually are irregularly arranged. They are partly grown-in into the crystal and partly generated later by strain-induced processes. At high temperatures, climb processes take place that distort the dislocation array even more. This further increases the irregular shape and the distribution of the dislocations. In contrast to simple "slip" dislocations, these "grown-in" dislocations cannot be passivated well by a hydrogen-passivation step later in the solar cell processing. With crystal diameters above 30 mm, the monocrystalline but dislocated growth is not stable and in most cases changes to polycrystalline growth because of the tendency of a Si crystal to form twins in the presence of strain and dislocations. These twins also multiply and form higher-order twins and thus rapidly form a polycrystal. This fine-grained poly-Si material is not usable for solar cell production. Known causes for the generation of the critical first dislocation are either solid particles in the melt that move to the solidification front, gas bubbles that are trapped at the solidification front, impurities that exceed the solubility limit in the melt, vibrations of crystals and melt, thermal shocks or a too high cooling strain.

The growth of the seed cone is the most critical stage in the pulling of the Cz crystal. For productivity reasons very flat seed cones are preferable since the time for the making of the cone is not productive. However, the probability of introducing dislocations in the seed cone is lowest for tapered cones, although this means an increase in the pulling time by 15 to 25% for the same body length and additional loss in usable material. The loss of time and material gets worse for larger ingot diameters.

Owing to the reaction between the liquid Si and the quartz crucible, the crucible is of considerable importance to the growth. The silica of the crucible supplies considerable amounts of oxygen to the melt and, owing to the high purity of the silica, only small amounts of other impurities. However, the crucible tends to dissolve after a long-standing time so that the risk for particles in the melt from the crucible is increased with increased pulling time. The oxygen of the melt adds up to 10^{18} oxygen atoms/cm^3 to the growing crystal, whereas carbon is usually $<10^{17}$/cm^3 and has only little impact on the solar cell performance. Oxygen effects like thermal donors and precipitates can be well controlled in Cz cell processing.

6.2.2 Tri-crystalline Silicon

The mechanical properties of tri-crystalline silicon (tri-Si) allow slicing of ultra-thin wafers with higher mechanical yield than monocrystalline silicon (see [5, 6]). Tri-Si is a crystal compound consisting of three mutually tilted monocrystalline silicon grains [5, 6]. The crystal compound has a (110) surface orientation in all grains in contrast to the standard (100) orientation of wafers for today's solar cell production. While two of the grain boundaries in a tri-crystal are $\sum 3$ classified, that is, first-order twins, the third grain boundary is a $\sum 9$ structure, that is, a second-order twin. All boundaries are perpendicular to the (110) wafer plane and meet at the ingot centre forming a characteristic tri-star. Tri-Si growth is fully compatible with standard Cz monocrystalline growth, but it is faster. Using a tri-crystal seed that contains the complete generic information, tri-Si ingots of 100 to 150 mm diameter and up to 700 mm length are grown in standard commercial crystal pullers using optimised growth parameters for neck, crown and body (see Figure 6.2).

As the pulling axis is parallel to the common <110> orientation of all three grains, the dislocations often cannot be completely eliminated during necking, resulting in ingots that are not dislocation-free. The maximum local dislocation densities are about 105/cm^2 in the ingot top and about 107/cm^2 in the ingot bottom. The dislocations are often arranged

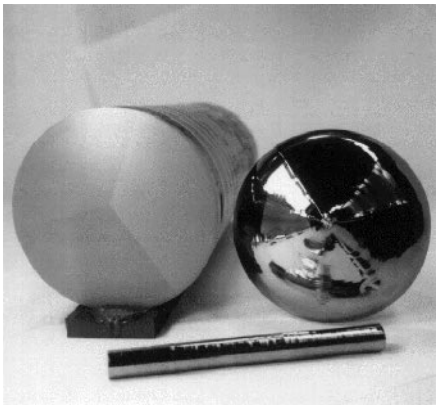


Figure 6.2 Tri-crystal seed (front), tri-crystal with cropped crown (left) and tri-crystal crown (right) with typical facets

in a streetlike geometry, while the dislocation density is significantly reduced in between the streets. However, despite the presence of dislocation from the very beginning (!), ingots of up to 700-mm length can be Cz-grown with multiple recharges at increased pull speed (see Figure 6.3). This is in fundamental contrast to the traditional c-Si growth with (100) orientation where dislocations must be completely avoided because otherwise the crystalline structure is totally lost after only a few centimetres of dislocated growth due to rapid dislocation multiplication. This peculiar structural stability of tri-Si, studied in detail through a geometrical stress model, is attributed to a reduction of cross slip in the tri-Si structure [7, 8].

Regarding electrical properties, ELYMAT mappings [9] show that there is a good spatial correlation between dislocation density and minority-carrier diffusion length: areas of high dislocation density show low diffusion length values. For dislocation lean ingots with 4- to 10-Ωcm resistivity, diffusion length values of more than 1000 μm (see Figure 6.4) can be obtained before light-induced degradation (LID).

The LID of the diffusion length of Cz-Si has recently been investigated extensively by several groups [1, 10, 11]. Although the identification of the defect structure is yet

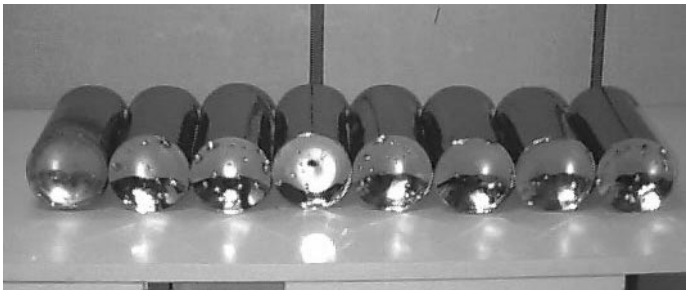


Figure 6.3 Tri-Si ingots (Ø140 mm) from quasi-continuous pulling

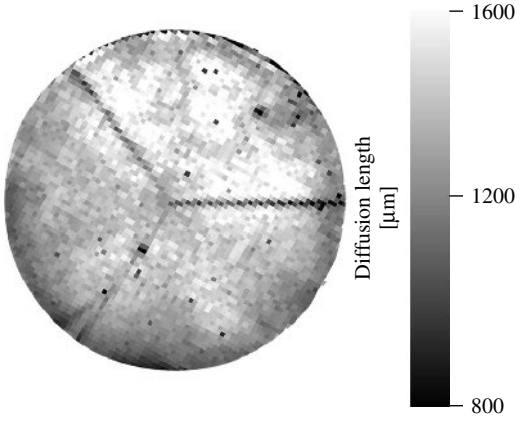


Figure 6.4 Diffusion length map of a 10-Ωcm as-grown wafer cut from the top of a dislocation lean tri-Si ingot. Lateral average diffusion length is 1300 μm

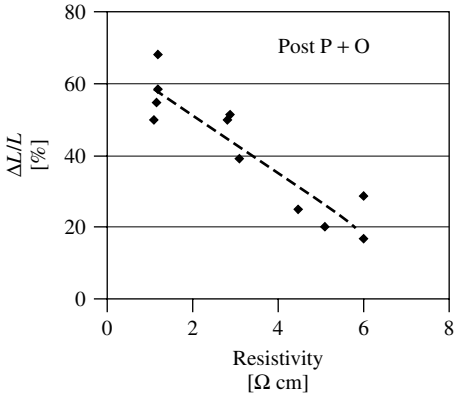


Figure 6.5 Relative degradation of diffusion length versus base resistivity for tri-crystalline silicon, measured after a standard P-diffusion and oxidation process

to be accomplished, a strong correlation of the effect with boron and oxygen is well established. Because tri-Si is grown with boron doping using standard Cz technology, an impact of LID on electrical quality is also present. Figure 6.5 shows a plot of the relative degradation as a function of base resistivity after a standard P-diffusion and oxidation process. Relative degradation values of less than 30% can be reached with 4- to 6-Ωcm material.

Tests on Si crystals fabricated from virgin poly-feedstock material with gallium, indium or aluminium as doping material have been performed to study LID. Best results have been obtained for Indium-doped material, for which the LID effect is reduced to almost below 3% of the diffusion length, which is within the accuracy limit of the ELYMAT measurements. With this material, light stable diffusion length values above 1 mm (!) can be achieved. This material is therefore best suited for high-efficiency cell processes.

In order to test the tri-Si material with standard solar cell processes, test cells are manufactured with a modified "Siemens Solar Boron Back Surface Field" (BSF) process with screen-printed contacts, as described in [12]. The final cell thickness was between 120 and 250 μm. A boron-BSF process was chosen since the BSF is crucial for high efficiency at reduced wafer thickness and beneficial for material with high diffusion length. SiN deposited with a commercial low pressure chemical vapour deposition (LP-CVD) method was applied as an AR coating, that is, no volume passivation can be expected since no molecular hydrogen was present during SiN deposition. In this case no complicated passivation or activation effects of hydrogen in Si must be taken into account [13–16]. In order to eliminate the effect of the different surface orientations and in order to focus on the pure material response, the wafers were *not* textured.

Table 6.1 shows that the efficiencies reach 15.5% in a lab-scale average. This efficiency compares well and slightly exceeds the results of corresponding solar cells from *solar-grade* <100> mono-material that was grown in standard production. The champion tri-Si cell efficiency without surface texturing was 15.9% using this cost-effective process.

Table 6.1 AM1.5 cell efficiencies for non-textured BSF cells on tri-Si and mono-Si substrates. Cell area is 103×103 mm^2 pseudo square

Material (non-textured)	Thickness average [μm]	Average efficiency [%]	V_{OC} [mV]	I_{SC} [mA/cm^2]	FF [%]	Rho [ohm cm]
Tri-Si	140	15.5	615	33.4	75.5	4
Mono-Si	200	15.2	612	32.7	76	1

6.3 BULK MULTICRYSTALLINE SILICON

Multicrystalline silicon besides monocrystalline silicon represents the basis of today's photovoltaic technology. Multicrystalline silicon offers advantages over monocrystalline silicon with respect to manufacturing costs and feedstock tolerance at, however, slightly reduced efficiencies. Another inherent advantage of multicrystalline silicon is the rectangular or square wafer shape yielding a better utilisation of the module area in comparison to the mostly round or pseudosquare monocrystalline wafers. The efficiencies of multicrystalline silicon solar cells are affected by recombination-active impurity atoms and extended defects such as grain boundaries and dislocations. A key issue in achieving high solar cell efficiencies is a perfect temperature profile of both ingot fabrication and solar cell processing in order to control the number and the electrical activity of extended defects. Moreover, the implementation of hydrogen-passivation steps in solar cell processing turned out to be of particular importance for multicrystalline silicon. With the introduction of modern hydrogen-passivation steps by Si_3N_4 layer deposition, the efficiencies of industrial multicrystalline silicon solar cells were boosted to the 14 to 15% efficiency range and consequently market shares were continuously shifted towards multicrystalline silicon as the standard material of photovoltaics.

6.3.1 Ingot Fabrication

Two different fabrication technologies for multicrystalline silicon, the Bridgman and the block-casting process (see illustrations in Figures 6.6 and 6.7) are employed. In both processes the solidification of high-quality multicrystalline silicon ingots with weights of 250 to 300 kg, dimensions of up to 70×70 cm^2 and heights of more than 30 cm have been successfully realised. While the Bridgman technology is a quite commonly used technique, the only two companies mainly employing the casting technology are Kyocera (Japan) and Deutsche Solar GmbH (Germany) [17, 18].

The main difference between both the techniques is that for the melting and crystallisation process only one crucible (Bridgman) is used, whereas for the crystallisation process a second crucible (block casting) is used.

In the case of the Bridgman process, a silicon nitride (Si_3N_4)-coated quartz crucible is usually employed for melting of the silicon raw material and subsequent solidification of the multicrystalline ingot. The Si_3N_4 coating thereby serves as an anti-sticking layer preventing the adhesion of the silicon ingot to the quartz crucible walls that owing to the volume expansion during crystallisation of the silicon material would inevitably lead to a destruction of both the silicon ingot and the crucible. Concerning the block-casting

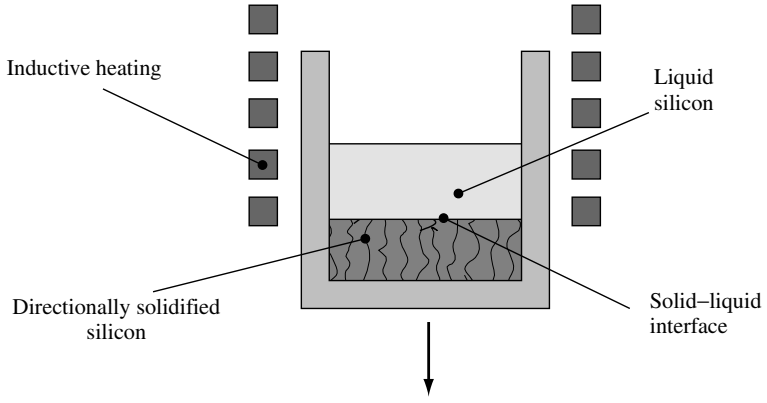


Figure 6.6 Conventional Bridgman technique that still is mainly used for the fabrication of multicrystalline ingots. Both melting and crystallisation of the silicon is performed in a Si_3N_4-coated quartz crucible. Crystallisation is realised by slowly moving downward the liquid silicon-containing crucible out of the inductively heated hot zone of the process chamber

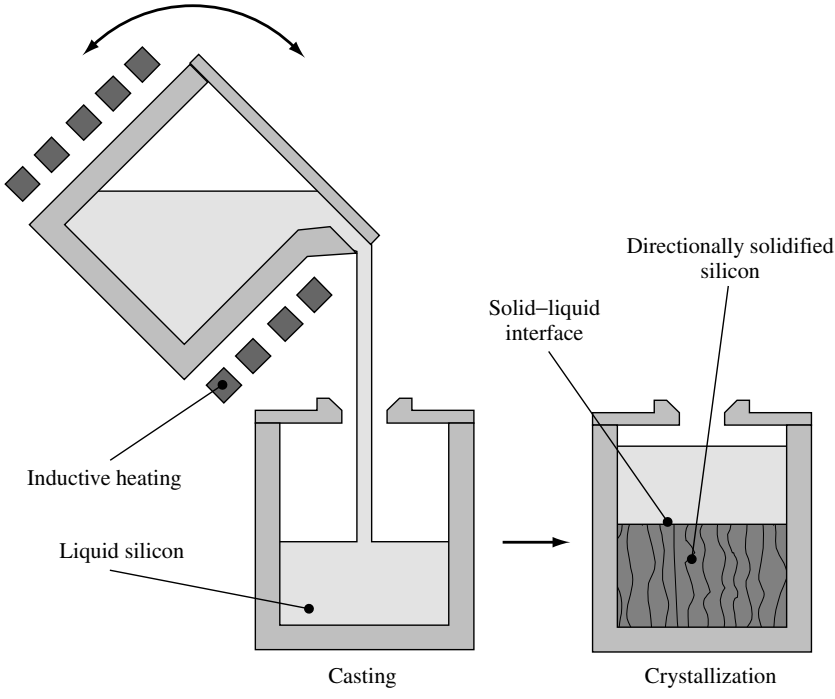


Figure 6.7 Block-casting process for the fabrication of multicrystalline silicon. After melting the silicon in a quartz pot, the silicon is poured into a second quartz crucible with a Si_3N_4 coating. The heating elements of the crystallisation crucible are not shown in the figure. In comparison with the Bridgman technique (see Figure 6.6), shorter crystallisation and cooling times can be realised by employing a more variable heater system

process, the melting is performed in a quartz crucible without a coating, whereas – after pouring the molten silicon into a second crucible – for the crystallisation also a Si_3N_4-coated one is used.

Usually, in both production technologies, crystallisation starts at the bottom of the crucible by lowering the temperature below the melting temperature (1410°C) of silicon. Within the Bridgman process the temperature reduction is achieved by simply descending the liquid silicon-containing crucible out of the hot area of the crystallisation furnace. Contrarily, the temperature control during the block-casting process is achieved by a corresponding adjustment of the heaters, whereas the crucible itself is not moved during solidification.

After solidification starts in the bottom region, the crystallisation front, that is, the liquid–solid interphase, moves in a vertical direction upwards through the crystallisation crucible. This so-called directional solidification results in a columnar crystal growth and consequently adjacent wafers fabricated out of the ingots show nearly identical defect structures (grain boundaries and dislocations).

Common crystallisation speeds used for the Bridgman technology are in a range of about 1 cm/h (corresponding to a weight of approximately 10 kg/h for large ingots). With regard to the increase in crystallisation speed, that is, productivity, mainly cooling of the already crystallised fraction of the ingot has to be taken into account. Too high process speeds cause large thermal gradients within the solidified silicon that may result in cracks or even destruction of the ingot. For the block-casting technology, however, owing to the more versatile and sophisticated heater system, considerably higher crystallisation speeds can be achieved [18].

6.3.2 Doping

Standard multicrystalline silicon is a boron-doped p-type material with a specific electrical resistivity of about 1 Ωcm, which corresponds to a boron concentration of about $2 \times 10^{16}/cm^3$. The specific resistivity is adjusted in a way such that optimal solar cell performance is guaranteed. Naturally, the boron concentration can be varied according to the requirements of specific solar cell processes. Specific resistivities in a range of 0.1 to 5 Ωcm have been used for solar cell fabrication so far. The boron concentration is normally adjusted by adding the equivalent amount of B_2O_3 to the silicon raw material prior to melting of the silicon. Considering alternative doping elements like gallium (p-type) or phosphorous (n-type) first, the segregation coefficient governing the resistivity decrease with increasing block height has to be considered. With a segregation coefficient of 0.8, boron nearly always is the optimal doping element giving only a small resistivity change over the silicon ingot (see Figure 6.8), whereas gallium and phosphorous with segregation coefficients of 0.008 and 0.35, respectively, are less favourable.

For phosphorous as an n-type dopant, additionally the disadvantage of a lower minority charge carrier (i.e. holes) mobility and a more complicated solar cell process using, for example, higher process temperatures for boron instead of phosphorous diffusion is encountered. However, recent results indicate that the activity of extended defects in n-type multicrystalline silicon is unexpectedly low, which could render n-type material nevertheless an attractive new feedstock source for photovoltaics.

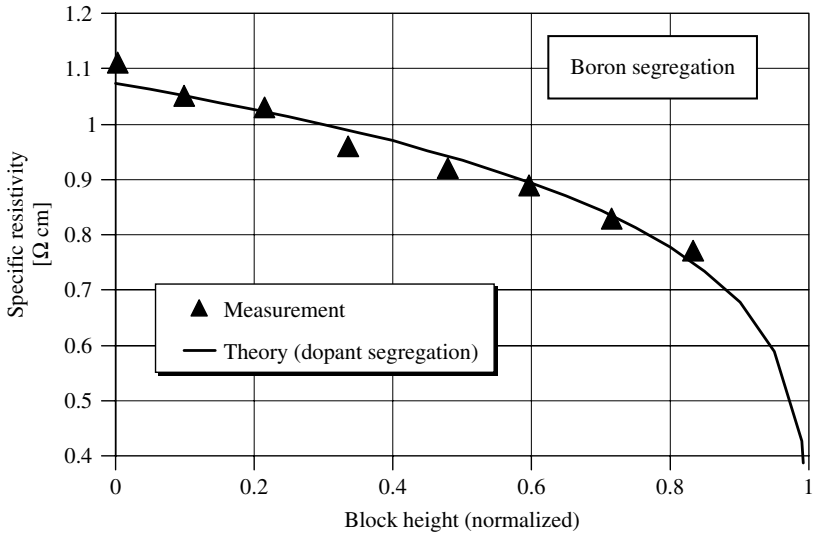


Figure 6.8 Decrease in the specific resistivity of *p*-type multicrystalline silicon due to segregation of the doping element boron

6.3.3 Crystal Defects

The main crystal defects in multicrystalline silicon are grain boundaries and dislocations. Concerning the attainable efficiencies of solar cells, not only the concentration of these defects but also their electrical activity is considered as crucial.

With respect to the grain boundaries and the grain size, basically smaller grains are observed at the beginning of the crystallisation process in the ingot bottom part. With increasing block height, individual grains prevail at the expense of surrounding grains and thus give rise to an increase in the mean grain size. This increase of grain size, however, depends on the crystallisation speed (see Figure 6.9). A higher crystallisation speed also means higher temperature gradients and thus an increased probability for the formation of crystal seeds in the melt that in turn lead to a limitation of the grain size. This is also the reason for faster crystallised block-cast material usually exhibiting smaller grains than conventional Bridgman-type multicrystalline silicon.

On the other hand, the grain sizes achieved with modern block-cast material are still large enough to not degrade solar cell efficiencies provided that the electrical activity of the grain boundaries is low enough. Grain boundaries and dislocations, if electrically charged, effectively attract minority charge carriers and consequently represent highly active recombination centres for photo-generated charge carriers. The electrical activity of grain boundaries and dislocations is determined by their impurity decoration (specifically by transition metals) and strongly increases with higher impurity concentrations.

Moreover, it was discovered that the shape of the crystallisation front during solidification also has considerable influence on the grain boundary activity [19]. Preserving a strictly planar solidification front clearly leads to a reduced grain boundary activity.

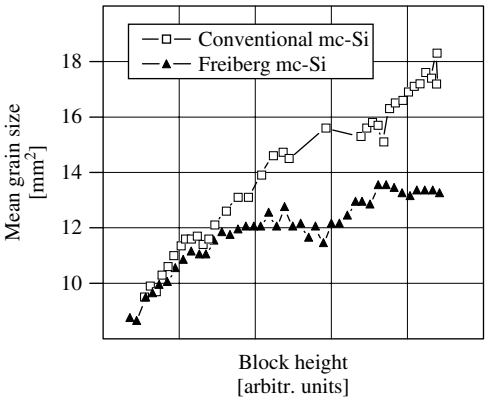


Figure 6.9 Mean grain size as a function of the block height for conventional Bridgman-type multicrystalline silicon (mc-Si) and the faster crystallised block-cast material from the Freiberg production facility of Deutsche Solar GmbH. Reduced crystallisation times lead to slightly lower grain sizes of the Freiberg mc-Si

Because also in modern high-throughput production processes a nearly perfectly planar solidification front is kept throughout the crystallisation process, grain boundaries show only weak electrical activities and therefore are generally considered as less important for solar cell efficiencies.

Crystal dislocations, however, turned out to be the most efficiency-relevant defects in multicrystalline silicon for solar cells. The dislocation density that is experimentally accessible by counting micrometer-small etch pits after appropriate chemical etching steps nearly shows a perfect correlation to the wafer lifetime and diffusion length (Figure 6.10) that are closely linked to solar cell performance. Dislocations are induced and multiplied

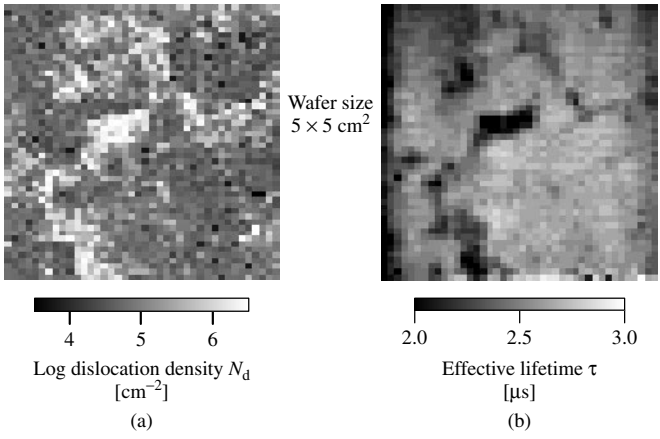


Figure 6.10 Topographies of the dislocation density N_d (a) and the effective lifetime τ_{eff} (b) of a typical multicrystalline silicon wafer showing the excellent correlation of both parameters. The effective lifetime measurements were conducted out without any surface passivation and thus are limited to less than approximately 3 μs by surface recombination processes

by thermal stress that is originated from temperature non-homogeneities during crystallisation and cooling of the ingot. The reduction of these temperature variations while keeping high process speed is therefore considered one of the most important issues for the further improvement of multicrystalline silicon.

An optimal process scenario for the production of multicrystalline silicon from both the crystal defect and the productivity point of view starts with a small crystallisation speed and minimal temperature gradients in order to secure a low-defect density bottom region of the ingot. After that, crystallisation speed should be largely increased for productivity reasons while keeping the solidification front planar and thermal gradients within the solidified silicon low.

6.3.4 Impurities

Despite boron being the standard dopant and thus an intentionally introduced impurity, even higher impurity concentrations in multicrystalline silicon are observed for both oxygen and carbon.

The interstitial oxygen concentration in multicrystalline silicon is affected by two processes, which are oxygen incorporation via the quartz crucible during melting and oxygen loss through evaporation of SiO, that is, the evaporating gaseous silicon monoxide that is stable at high temperatures only.

Because the segregation coefficient >1, the oxygen content decreases with increasing block height. Typical concentrations of the interstitial oxygen content of Bridgman and block-cast material are given in Table 6.2. Obviously, although the silicon melt never stays in direct contact with the quartz crucible, lower oxygen concentrations with Bridgman-type material compared to silicon from the block-casting process are not feasible. We therefore conclude that there also has to exist an oxygen release from the Si_3N_4 coating (containing some percentage of oxygen) into the silicon melt during the Bridgman process. In addition, we observe a much more rapid decrease of the oxygen concentration with increasing block height for block-cast material, which is attributed to the normally employed lower ambient pressure and enhanced gas exchange during this process.

Table 6.2 Typical concentrations of interstitial oxygen $[O_i]$ for block-cast material from the Freiberg production plant of Deutsche Solar GmbH and for typical material coming from a Bridgman process. For the determination of the oxygen concentration by Fourier Transform Infrared Spectroscopy (FTIR), a conversion factor of $2.45 \times 10^{17}/cm^2$ was used

Ingot position	Interstitial oxygen concentration $[O_i]$ $[10^{17}/cm^3]$	
	Block-casting process	Bridgman process
Bottom	6.5	6
Middle	0.9	3.5
Top	0.5	2

Although oxygen residing on interstitial lattice sites is not electrically active, recombination-active oxygen complexes such as thermal donors [20–22], new donors [23, 24] and oxygen precipitates may be formed after annealing steps, specifically in the high oxygen concentration bottom part of the ingot (see an example of the donor activity in Figure 6.11).

Specifically, thermal donors turned out to be mainly responsible for a broad low-lifetime region with a width of 4 to 5 cm in the bottom part of Bridgman-type ingots [25]. Owing to the instability of the thermal donors in high-temperature steps during solar cell processing, these low lifetimes, however, does not lead to low efficiencies. It is worth noting that the width of this low-lifetime region in the bottom part of the ingots is largely reduced for material from the block-casting process. The most likely explanation for this is the shorter process times that consequently give less time for the formation of oxygen complexes out of interstitial oxygen atoms.

Similar to metals, oxygen segregation at grain boundaries and dislocations enhances the recombination strength of these extended defects. Oxygen precipitates may also getter metal impurities during crystallisation, which are released afterwards during solar cell processing as highly recombination-active point defects.

Generally, the manifold involvement of oxygen in efficiency-relevant microscopic processes makes the reduction of the oxygen incorporation into multicrystalline silicon one of the most important targets of material improvement efforts.

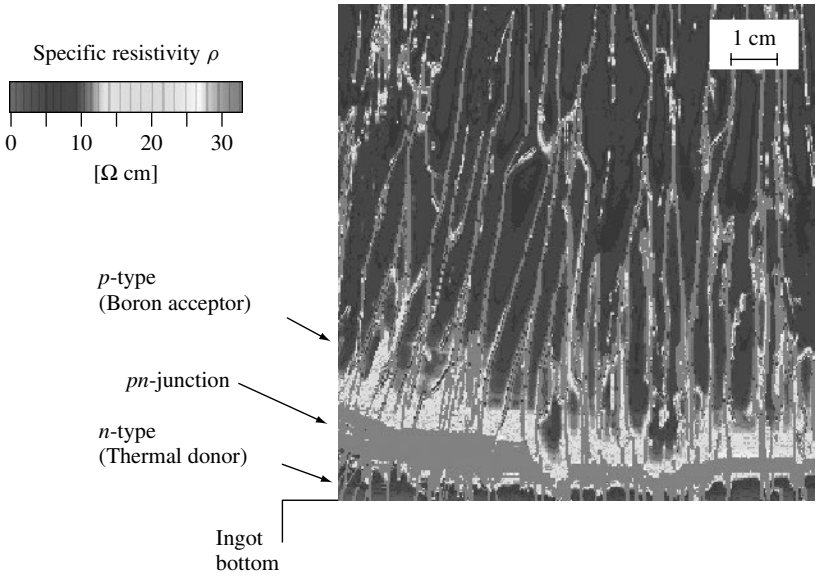


Figure 6.11 High resolution map of the specific resistivity (van-der-Pouw measurement technique) of a vertically cut wafer from a special high resistivity *p*-type multicrystalline silicon test ingot. Owing to the increased oxygen content, the formation of thermal oxygen donors changes the conductivity to *n*-type in the bottom part. The *pn*-junction can be identified by a remarkable increase in the specific resistivity

Like oxygen, carbon in multicrystalline silicon appears in concentrations considerably higher than those of the boron dopant concentrations. Typical concentrations of substitutional carbon are in the range of $2-6 \times 10^{17}/cm^3$ generally increasing with increasing block height. The incorporation of carbon into the silicon melt takes place via gaseous CO formation inside the crystallisation chamber by SiO chemically reacting with the graphite heaters. The main problem that is caused by an increased carbon concentration is the formation of needle-shaped SiC crystals (often associated with oxygen and nitrogen, see Figure 6.12) within the silicon material. SiC representing an electrically conductive semiconductor material effectively shorts the solar cell *pn*-junction, thereby leading to drastically reduced efficiencies. The problem of SiC formation, however, usually occurs only in the uppermost region of the ingot that is anyway rejected because of segregation of metallic impurities.

Despite oxygen and carbon being present in much higher concentrations, transition metals like iron or titanium are considered as much more important with regard to solar cell efficiencies with the exception of the outer edges (width 5–10 mm) of an ingot where in-diffusion from the Si_3N_4 coating may occur and the top segregation region metal point defects in high-quality multicrystalline silicon are present in concentration levels below the detection limit of Deep Level Transient Spectroscopy (DLTS) measurements,

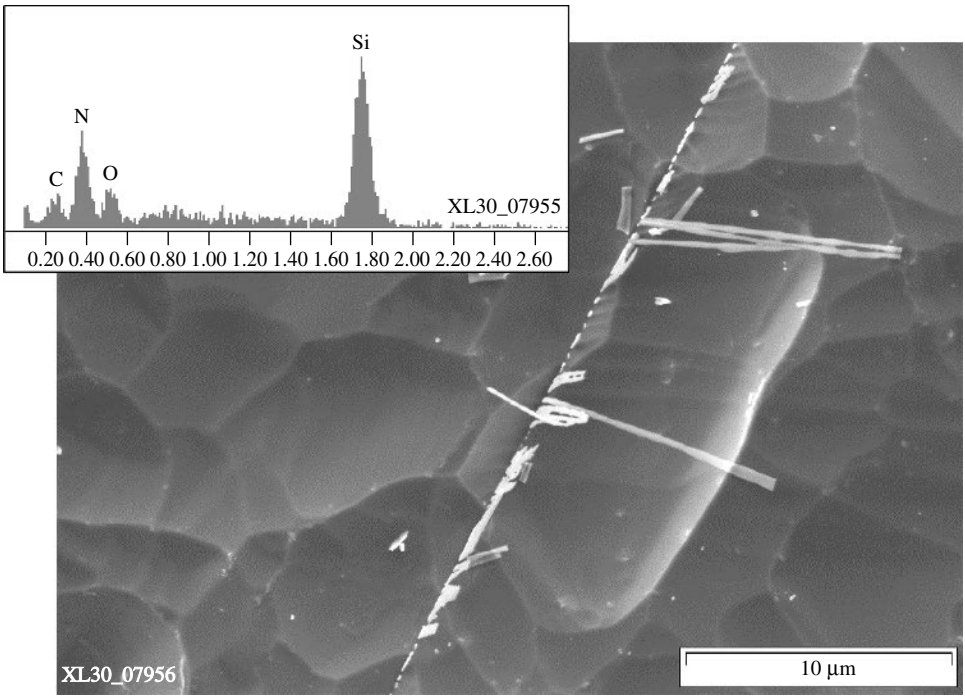


Figure 6.12 SEM (Scanning Electron Microscope) image of a heavily shunted solar cell region. The microscopic investigations reveal needle-shaped structures containing silicon, nitrogen, oxygen and carbon. The shunting mechanism is assumed to be due to electrically conductive SiC that short-circuits the solar cell *pn*-junction

that is, below approximately $10^{12}/cm^3$. The importance of metal impurities for multicrystalline silicon solar cells is, however, based on metal impurities controlling the activity of extended defects, specifically that of crystal dislocations.

We anticipate that metallic impurities are, for example, responsible for the observed systematic changes of the lifetime of multicrystalline silicon wafers after high-temperature steps in the range of 800 to 1000°C (e.g. the phosphorous diffusion step for fabrication of the solar cell *pn*-junction). The wafer lifetime quite commonly decreases in annealing steps above 900°C, where this decrease is even more significant at enhanced cooling speeds after the anneal. The proposed mechanism behind this lifetime degradation is a release of metal atoms from extended defects like dislocations into the wafer bulk material and a subsequent quenching of the metal atoms as highly recombinative point defects.

Another hint of an extensive interaction between extended defects and metal impurities is given in Figure 6.13 that depicts the theoretical segregation profile of iron in an intentionally contaminated multicrystalline ingot (mean iron concentration: $7.9 \times 10^{17}/cm^3$) as compared to the experimental one. We clearly can state a reduced experimentally determined segregation effectiveness most probably caused by iron segregation into extended defects competing with the segregation process in the liquid silicon phase during crystallisation.

In order to prevent such defect–metal interaction processes leading to enhanced recombination activity, a very effective segregation of metallic impurities into the ingot top region has to be assured. This segregation effectiveness, however, decreases with both increasing crystallisation speed and increasing concentration of extended defects.

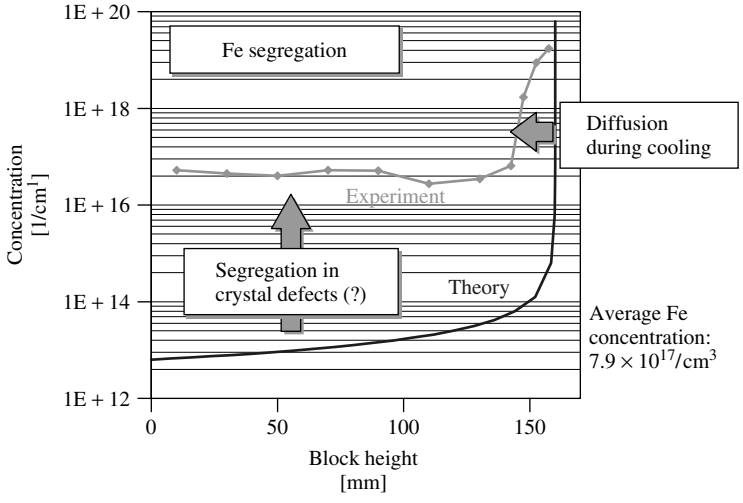


Figure 6.13 Experimentally determined iron concentration of an intentionally contaminated multicrystalline silicon test ingot (mean Fe concentration: $7.9 \times 10^{17}/cm^3$). The experimental data is given as a function of the block height and in comparison to the theoretically expected profile. The much higher than theoretically predicted concentration in the bottom and middle part of the ingot is attributed to a segregation not only into the silicon melt but also into extended crystal defects during solidification

This in turn verifies the importance of a properly adjusted and controlled crystallisation speed. In order to assure an effective impurity segregation for high-quality multicrystalline silicon, specifically in regions with increased defect densities (e.g. ingot bottom part), solidification at a low crystallisation speed is essential.

6.4 WAFERING

More than 80% of the current solar cell production requires the cutting of large silicon crystals. Multicrystalline ingots grown by the Bridgman or gradient freeze technique now reach cross sections of more than 50×50 cm^2 and weigh over 250 kg; monocrystalline Cz crystals have diameters of up to 20 cm today. While in the last few years the cost of solar cell processing and module fabrication could be reduced considerably, the sawing costs remain high.

Figure 6.14 shows that the sawing costs are a substantial part (29%) of the wafer production cost and thus contribute considerably to the total module cost. Since the sawing of the crystals is connected with high material losses (about 50%), ribbon growth techniques or the thin film technology, which avoid the sawing step, have a high potential for developing cheaper solar cells. However, both technologies still have to overcome serious difficulties and their development will probably take another 5 to 10 years. The present task is therefore to optimise the sawing technique for further cost reduction in mass production.

At the beginning of the PV industry, the available sawing technology of the microelectronic industry was used. The ingots were mainly cut by inner diameter (ID) saws. This technology is, however, relatively slow and not economical for mass production [26]. It was therefore gradually replaced by the multi-wire slicing technology [27]. The advantages are the higher throughput of about 500 to 700 wafers per day and per machine, a smaller kerf loss of about 180 μm and almost no restrictions on the size of the ingots. Currently, wafers between 250 and 350 μm are usually cut, but a wafer thickness down to about 100 μm can be achieved by the technique. Since the technology is relatively new and still under development, most wafer manufacturers have to optimise the sawing process by their own experience. The sawing process depends on several variable parameters as will be described next, which makes it difficult to optimise the process in view of throughput, material losses, reduction of supply materials and wafer quality.

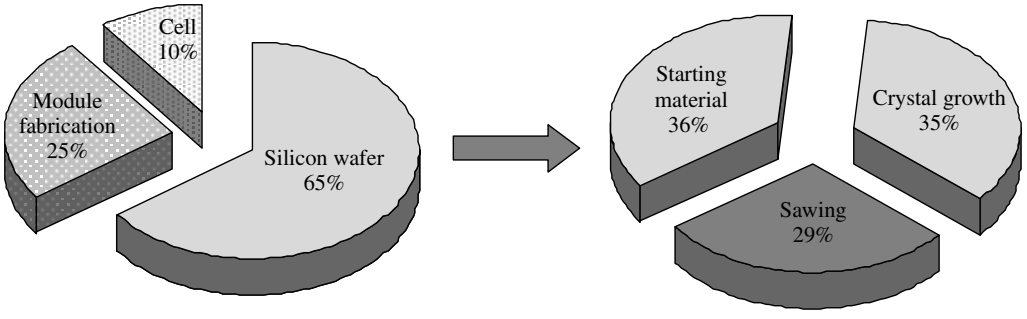


Figure 6.14 Cost distribution for modules and silicon wafers

Basic knowledge about the microscopic details of the sawing process is required in order to slice crystals in a controlled way. In the following section, the principles of the sawing process will be described as far as they are understood today.

6.4.1 Multi-wire Wafering Technique

After crystal growth the silicon ingots are cut in a first step by band saws into columns with a cross section that is determined by the final wafer size. Standard sizes are about 10×10 cm^2, but larger wafers sizes up to 15×15 cm^2 are increasingly used in the solar cell technology. The columns are glued to a substrate holder and placed in a multi-wire saw that slices them into the final wafers. The principle of the multi-wire technology is depicted in Figure 6.15. A single wire is fed from a supply spool through a pulley and tension control unit to the four wire guides that are grooved with a constant pitch. Multiple strands of a wire net (known as a web) are formed by winding the wire on the wire guides through the 500 to 700 parallel grooves. A take-up spool collects the used wire. The wire is pulled by the torque exerted by the main drive and slave as shown in the figure. The tension on the wire is maintained by the feedback control unit at a prescribed value. The silicon column on the holder is pushed against the moving wire web and sliced into hundreds of wafers at the same time. The wire either moves in one direction or oscillates back and forth. Solar cell wafers are mainly cut by a wire that is moving in one direction, whereas wafers for the microelectronic industry are cut by oscillating wires. Cutting in one direction allows higher wire speeds between 5 and 20 m/s, but yields less planar surfaces. Smoother and more even surfaces are obtained by oscillating sawing. Depending on the pulling speed, the wires have a length between 150 and 500 km in order to cut a single column in one run. The wire material is usually stainless steel.

Cutting is achieved by an abrasive slurry, which is supplied through nozzles over the wire web and carried by the wire into the sawing channel. The slurry consists of a

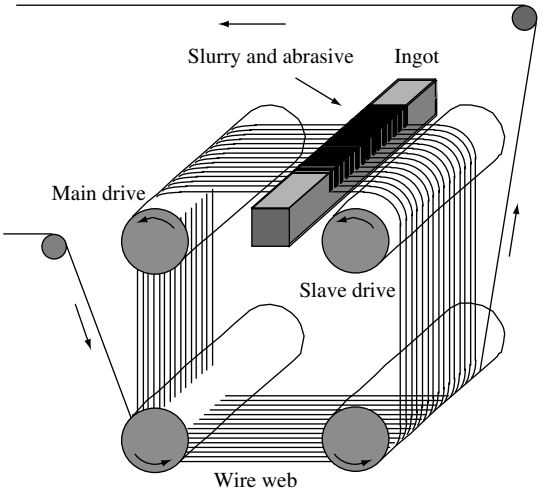


Figure 6.15 Schematic diagram depicting the principle of the multi-wire sawing technique

suspension of hard grinding particles. Today, SiC and diamond are the most commonly used abrasives. Both materials are very expensive and account for 25 to 35% of the total slicing cost. The volume fraction of solid SiC particles can vary between 20 and 60% and the mean grain size between 5 and 30 μm. For polishing smaller grain sizes below 1 μm are used. The main purpose of the slurry is to transport the abrasive particles to the sawing channels and to the crystal surface. It also has to keep the particles apart and must prevent their agglomeration. The entry of the slurry is a result of the interaction between the wire and the highly viscous slurry. Normally, only a small amount of slurry enters the cutting zone. The factors that are important here are the viscosity and the wire speed, but to understand the fluid mechanical problems that are involved a complex physical modelling is required. First attempts of a description have been reported recently [28–31].

Most of the commercial slurries are based on oil, but water-based or water-washable slurries based on ethylene glycol have been tested as well. Oil slurries have several drawbacks. The wafers can stick together and are difficult to separate after sawing. This problem will become even more severe when the wafer thickness will be reduced in the future. The removal of oil from the wafer surfaces requires comprehensive cleaning procedures. Since large quantities of slurry and SiC are used during sawing and recycling is not possible at present, the disposal of these materials has to be considered as well. The disposal causes, however, environmental hazards and is therefore complicated and expensive. On the contrary, water-based slurries or slurries that are very hygroscopic have the problem that hydrogen gas is generated from the interaction of water and silicon, which can cause the hazard of explosion. From the environmental point of view, water-washable slurries may be the choice of the future.

Material is continuously removed through the interaction of the SiC particles below the moving wire and the silicon surface. The abrasive action of the SiC depends on many factors such as wire speed, force between wire and crystal, the solid fraction of SiC in the suspension, the viscosity of the suspension, the size distribution and the shape of the SiC particles. The viscosity of the slurry depends on the temperature and the solid fraction of particles. Since the temperature rises as a result of the cutting process, the suspension has to be cooled and the temperature controlled during sawing. The viscosity of the slurry also changes because of the continuous abrasion of silicon and iron from the wire. This gradually deteriorates the abrasive action and the slurry has to be replaced or mixed with new slurry after some time.

The kerf loss and surface quality are determined by the diameter of the wire, the size distribution of the SiC particles and the transverse vibrations of the wire. The amplitude of vibration is mainly sensitive to the tension of the wire, but it also depends on the damping effect of the slurry. Increasing the tension will reduce the amplitude of vibration, hence the kerf loss [32]. Typical wire diameters are around 180 μm and the mean size of active particles can vary between 5 and 30 μm. This yields kerf losses around 200 to 250 μm per wafer.

The objective of efficient sawing is to slice with a high throughput, with a minimum loss of slurry and silicon and with a high quality of the resulting wafers. Since many parameters can be changed, the optimisation of sawing becomes a difficult task and today it is mainly done by the wafer manufacturers. They are mostly guided by experience. In

the following section, the main results of investigations are summarised, which describe the current understanding of the microscopic details of the wire sawing and yield some guidelines to optimise the process.

6.4.2 Microscopic Process of Wafering

Figure 6.16 shows schematically a cross section of the wire in the cutting zone. The space between the wire and the crystal surface is filled with slurry and SiC particles. The pressure of the wire on the particles varies along the contact area. The forces are maximal directly below the wire and decrease towards the side faces. Because of the transverse vibrations, the wire also exerts forces sideward, which determines the surface quality of the sliced wafers. The interaction between the abrasive SiC particles and the silicon crystal yields a distinct damage pattern on the surface that can be analysed by microscopic techniques. A typical surface structure as seen under an optical microscope is shown in Figure 6.17. Similar structures are obtained along the entire contact zone, which shows that the abrasive process is the same in all directions.

The surface structure consists of local indentations with a mean diameter of a few micrometers. Such a uniform structure can be explained by the interaction of loose, rolling particles that are randomly indented into the crystal surface until small silicon pieces are chipped away. Since SiC particles are facetted and contain sharp edges and

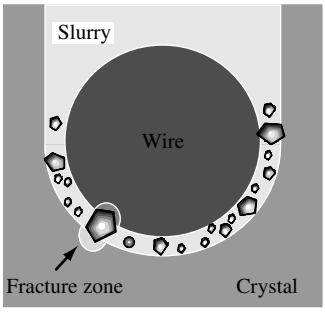
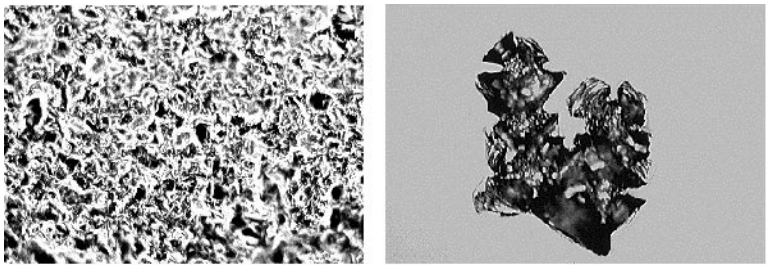


Figure 6.16 Cross section of wire, slurry with abrasive and crystal in the cutting zone



(a) (b)

Figure 6.17 Optical micrograph of the surface of an as-cut silicon wafer (a) and several micro-indentations on a polished silicon surface (b)

tips, they can exert very high local pressures on the surface. This "rolling grain" model forms the physical basis of the wire sawing process. Similar surface structures also form after lapping semiconductor surfaces with loose abrasive particles.

The individual process of the interaction of a single particle with sharp edges and the surface of a brittle material can be studied by micro-indentation experiments. This is shown in Figure 6.17(b) for a silicon surface. The damage structure of several overlapping micro-indentations with a Vickers diamond indenter resembles the structure of an as-cut wafer. Numerous micro-indentation experiments on monocrystalline silicon have been carried out in the past to investigate the damage structure quantitatively (e.g. [33–37]). The main results are summarised schematically in Figure 6.18 for a "sharp" Vickers indenter with pyramid geometry. Loading by sharp indenters first leads to the generation of a remnant plastic impression in the surface known as the elastic–plastic zone. Recent Raman investigations of this region have shown that under high pressures the silicon lattice transforms into other crystal structures. Several phase changes have been observed directly under the indenter, in particular a metallic high-pressure phase [38, 39]. Under loading at 11.8 GPa an endothermic transformation to metallic silicon (Si II) occurs ($\Delta G = 38$ kJ/mol), which partly transforms back to another high-pressure phase (Si III at 9 GPa, $\Delta G = -8.3$ kJ/mol). In the metallic state the silicon can plastically deform and

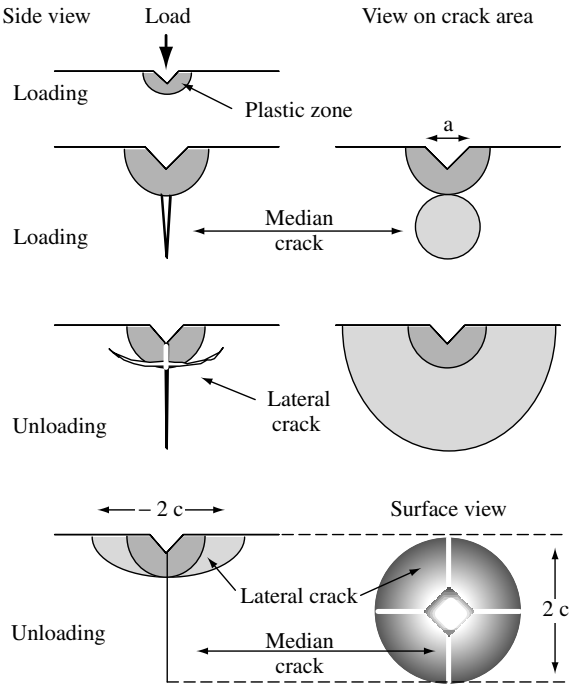


Figure 6.18 Schematic diagram of the development of the crack system below a sharp indenter upon loading and unloading. Dark gray areas indicate the plastic zone below the indenter. The dotted areas are the crack planes of the halfpenny-shaped median crack system. They are viewed from end-on (left side) or perpendicular to the plane (right side). In case radial cracks also occur, they may coalesce with the median crack and form a similar crack pattern

the material can be removed by processes known for ductile metals. This is, however, a slow but moderate process.

With increasing pressure the material begins to break and cracks are generated parallel to the load axis emanating from the plastic zone. Median cracks are generated beneath the plastic zone, where the tensile stresses are maximal, in the form of full or truncated circles. At a critical size they become unstable and extend towards the surface. In addition, shallow radial cracks may be generated at the edges of the plastic zone. Both radial and median cracks may coalesce to form halfpenny-shaped cracks that are visible at the surface (as shown in Figure 6.19). Upon unloading, residual stresses from the elastic–plastic zone can lead to lateral cracks parallel to the surface. When these lateral cracks reach the surface, material is chipped away. This is the main process for material removal during sawing. Chipping requires a certain minimum load to occur (chipping threshold). Above the limit when material is removed only the median and radial cracks remain. They are finally part of the saw damage.

A quantitative model based on the rolling grain interaction described above has been developed. Results have been compared with experimental investigations of the sawing process on commercial multi-wire saws, allowing for the extraction of useful conclusions. Details can be found in Reference [40].

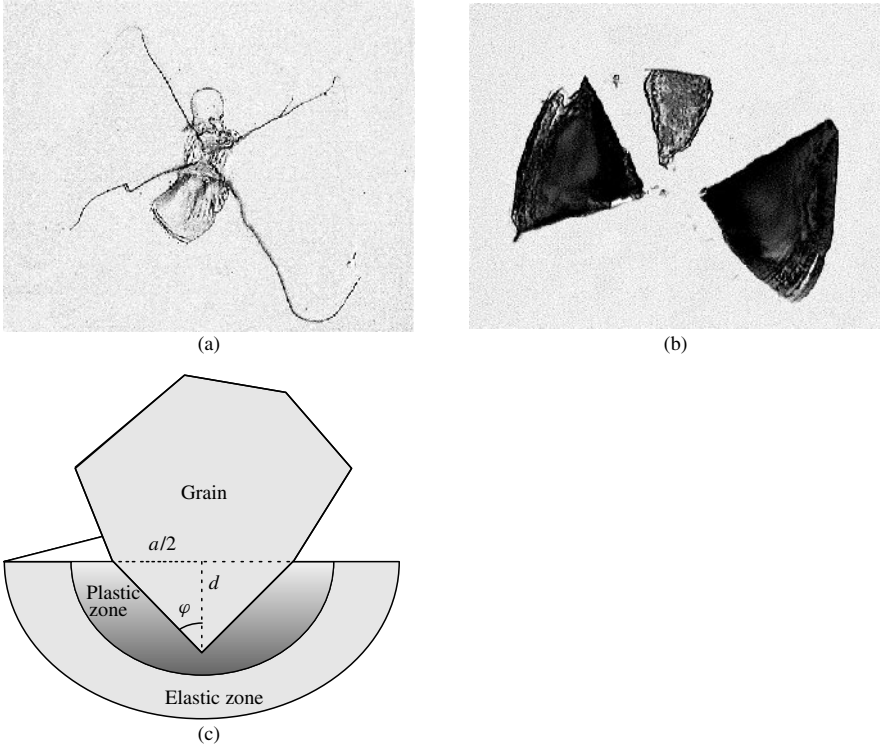


Figure 6.19 (a) Optical micrograph of median and (b) lateral cracks (below the surface) at a Vickers indentation. (c) Schematic representation of the impression of a sharp grain into a surface

6.4.3 Wafer Quality and Saw Damage

Several factors are currently considered to determine the quality of the wafers: fracture behaviour, crack density, thickness variations, surface roughness and cleanness. After sawing the surface of the wafer is damaged from the fracture processes and contaminated with organic and inorganic remnants from the slurry. Therefore, the wafers have to be cleaned and the saw damage removed by etching before a solar cell can be fabricated. In addition, the thickness and surface roughness of the wafer may vary, which may be detrimental for some of the further processing steps. All factors are related to the sawing process. Figure 6.20 shows an example of the topology of an as-cut surface. It consists of thickness variations on different length scales. On the scale of millimetres, one can observe grooves parallel to the direction of the wire. They occur particularly under higher loads and can be caused by a deficit of slurry, mechanical vibrations or inhomogeneities of the material. Mostly a large number of parallel wafers are then affected. Grooves on wafers cannot be removed by etching and thus reduce the quality of a wafer.

On a length scale of about 100 μm, the surface may have a wavy topology that is not detrimental unless sharp steps occur. On the micrometer-length scale the surface shows a certain roughness, which is directly related to the microscopic sawing process as described before. The extent of saw damage, which has to be etched away before solar cell processing, lies typically in the range of 5 to 10 μm.

Saw damage also occurs in the abrasive grains and the wire itself. Although the fracture strength of the SiC particles is higher than that of silicon, the grains eventually lose their sharpness owing to breakage that reduces their sawing performance. To reduce the abrasion of the grains, sawing should be done in a stress range where the load on the individual grains lies above the fracture strength of silicon but below that of SiC.

Typically, the wires have diameters between 150 and 180 μm and a length of about 150 to 500 km. They are made of stainless steel and coated with a brass layer.

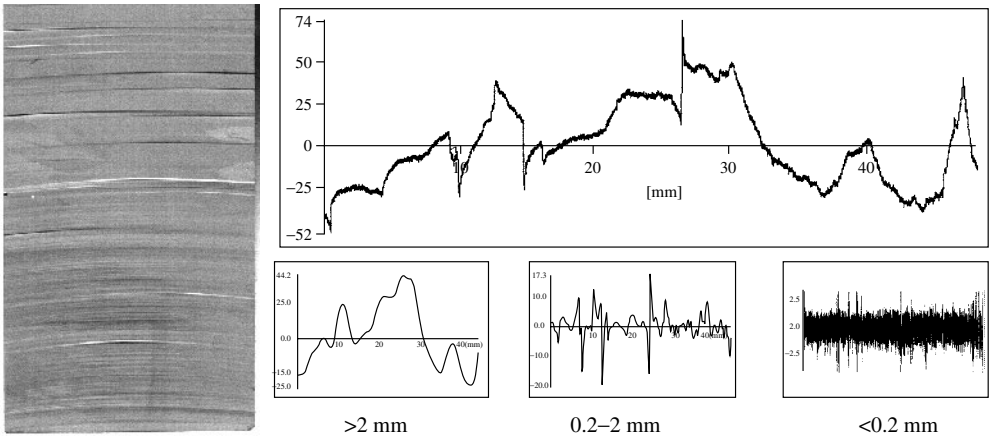


Figure 6.20 Surface structure of a wafer with grooves resulting from uneven cutting. It also shows the bowing of the wire under load during sawing. The surface profile measured by a laser scanner profiler is depicted on the right. Different wavelengths filtered from the profile are shown below

It is important that the thickness is very uniform over the entire length, because sudden changes in the diameter can lead to fracture of the wire or damage to the wafer surface. The abrasion of the steel wires is also due to the interactions with the grains. Excessive wear can lead to breakage, which is undesirable during sawing because it is very time consuming to build up the wire web inside the machine. Some manufacturers are beginning to develop *in situ* detection systems to control the sawing process and thus prevent the wire breakage.

6.4.4 Cost and Size Considerations

The investigations of the microscopic processes of wire sawing have laid the basis for the selection of the best range of parameters and for further modifications. It allows one to increase the sawing performance, to reduce the consumption of slurry, SiC powder, wire material and etchant, and hence directly the costs of slicing. Furthermore, the quality of the wafers such as roughness, flatness and saw damage of the surfaces can be improved. This is important in view of the development of thinner wafers for solar cells, which will reduce the consumption of expensive silicon. The current sawing technique in production allows the sawing of wafers with thickness down to about 200 μm. The goal is to further reduce the thickness to about 100 to 150 μm in production. Sawing of thinner wafers is possible but at present still at the expense of more breakage. The problem becomes even more severe when the wafer size increases at the same time to 15×15 cm^2 or more. In mass production such a development will only become possible by a careful selection of the parameter range and an *in situ* control of all the factors that determine the slicing process.

6.5 SILICON RIBBON AND FOIL PRODUCTION

Research and development on crystal growth technologies for production of crystalline silicon ribbon have been under way for three decades. Interest in methods of crystalline silicon wafer production was initiated during the oil crises of the mid-1970s. Out of this period arose the first large-scale efforts in R&D to develop low-cost methods of producing substrates for solar cell manufacture. A seminal program was conducted in the US, which was led between 1975 and 1985 by the Jet Propulsion Laboratory (JPL) Flat Plate Array Project [41]. It was the activity in this project in this time period, combined with larger investments from the private sector both in the US and internationally, that developed the seeds of the technology of crystalline silicon ribbon and foil production methods being commercialised today.

The past decade of R&D on crystalline silicon materials has culminated in the expansion of wafer manufacturing at an unprecedented pace. While established methods of production based on Cz growth, directional solidification and ingot casting have flourished, a new generation of ribbon technologies has moved past the R&D stage into large-scale manufacturing and is in competition with these conventional approaches. Ribbon technologies, some of which had entered R&D already in the early 1970s, and have now reached maturity with the start up of manufacturing on a megawatt (MW) scale, include Edge-defined Film-fed Growth (EFG), String Ribbon (STR) and Silicon Film™ (SF).

Dendritic Web (WEB) production and the Ribbon Growth on Substrate (RGS) technique are moving to pilot demonstration phases. A summary of the changes in the status of leading ribbon/foil technologies over the past decade and projections for manufacturing capacities are given in Table 6.3. It is anticipated that the ribbon production will contribute in excess of 30 MW of wafers to world solar energy markets by the end of 2001.

Development has not been continuous for most of the methods listed above. The R&D has been interrupted and then restarted in several cases when the technological status changed to generate new opportunities for cost-effective production. EFG development has the longest continuous history. After initial technology development on EFG started at Tyco Laboratories in 1971, it was subsequently augmented with funding from Mobil Oil, starting in 1974. In the time span from 1971 to the present, pilot lines using five different variations of the EFG process have been evaluated, starting with single ribbons in 1971 to the octagonal crystal tube now being commercialised. Ownership transferred to ASE Americas in 1994, at which time the transition to manufacturing was initiated. After periods of decreased activity, WEB, STR and RGS have all been strengthened with R&D in the past several years subsequent to being revitalised by new owners. WEB development was initiated with funding from Westinghouse in the 1970s, but now is being carried out by EBARA Solar. STR technology underwent an R&D phase in the early 1980s under the name of Edge-Stabilised Ribbon (ESR) and Edge-Supported Pulling (ESP) at the National Renewable Energy Laboratory and at Arthur D. Little, respectively, before being taken up in 1994 by Evergreen Solar. RGS development was initiated at Bayer, but is currently continuing with ECN of the Netherlands. If successful, a future commercialisation is anticipated by Deutsche Solar in Germany and Sunergy in the Netherlands.

Ribbon and foil technologies must meet the challenges of the photovoltaic marketplace and overcome a number of existing technical barriers if they are to continue to expand manufacturing and to position themselves to remain competitive in the next decade. Challenges to be met are productivity increases on a per furnace basis to drive down labour and overhead (capital) costs, improved mechanical and electronic quality of ribbon wafers together with the development of low-cost solar cell designs that will raise efficiencies to 18 to 20% and reduction of wafer thickness while maintaining high yields in order to reduce demand on silicon feedstock. Achievement of these goals in the next decade can lead to cost decreases, which will drive additional volume expansion for

Table 6.3 Historic record on R&D and manufacturing status of leading ribbon/foil technologies of the past decade

Wafer process/ year started	1990 status level		2000	2001	Schematic
WEB/1967	R&D	<0.1 MW	R&D <0.2 MW	Pilot −0–1 MW	Figure 6.20
EFG/1971 (Ribbon); 1988 (Octagon)	Pilot	1.5 MW	Production −12 MW	Production −20 MW	Figure 6.21
ESP (STR)/1980	R&D	–	Pilot <0.5 MW	Production <5 MW	Figure 6.23
SF/1983	–	–	Pilot −1–2 MW	Production >5 MW	–
RGS/1983	R&D	–	R&D	Pilot <1 MW	Figure 6.24

ribbon and foils and allow these new-generation technologies to become market leaders in silicon wafer production. Technology description, the status of each of the growth approaches and the barriers for each of the technologies to overcome in order to remain competitive are the topics of the following sections.

6.5.1 Process Description

The ribbon technologies that have been proposed over the past three decades and that have survived till the commercial manufacturing and R&D phases (Table 6.3) may be grouped into two basic approaches: "vertical" and "horizontal" growth (pulling) methods. The latter category is further subdivided into methods in which either a substrate is used to assist in the formation of the crystal or foil or those that do not use any substrate material. The horizontal methods refer not so much to the geometrical aspects related to the ribbon-pulling direction as to the disposition of the temperature gradients, which act at the interface and influence growth characteristics. The EFG, WEB and STR methods are examples of the vertical method category, while both the RGS foil and the SF methods grow crystals in a horizontal-pulling configuration with the aid of a substrate. The term "foil" is used interchangeably with wafer, but here we use it to refer more specifically to the RGS wafer to distinguish a unique aspect: the wafer is crystallised upon contact with a substrate, and is then detached and the substrate material recycled.

Ribbon/foil growth techniques have historically been evaluated in a number of variants and modifications of the techniques listed in Table 6.3. Successes and failures in many of these variants often spawned new processes or led to evolution and modifications in old variants. A bibliography and descriptions of the techniques and a detailed historical perspective of the many variant ribbon technologies that have been pursued can be found in the endnote [42] and in References [43, 44].

Fundamental differences exist in the heat transfer and the interface temperature gradients during growth for these two general categories of ribbon and foil production methods. These lead to very different process limits in several important areas: the capacity, or throughput potential in a single furnace configuration, crystallite or grain nucleation characteristics and the pulling speed. The speed is constrained as a consequence of the thermoelastic stress acting on the crystal during growth. The pull speed and stress affect the defect density and electronic quality. For example, for the vertical techniques – WEB, EFG and STR – the crystal growth direction and dominant heat transfer of latent heat from the interface are both parallel to the pulling axis of the ribbon and essentially perpendicular to the growth interface. The latent heat conducted along the ribbon is radiated to the environment. The pulling speed and the interface growth velocity are the same. For RGS and SF, crystals nucleate on the substrate and grow nearly perpendicular to the substrate-pulling direction, while the growth interface tends to be angled towards the pulling axis of the substrate. Thermal conduction of latent heat from the growth interface is augmented in the direction perpendicular to the pulling axis, that is, through the thickness of the ribbon, because of conduction into the substrate. This augmented heat removal allows very high ribbon production rates, whereby low interface growth rates, v_I, are realised with high pull rates, v_P, that is,

$$v_P = v_I / \cos(\theta)$$

where θ is the angle between the normal to the interface and the pull direction and is close to 90°. The low interface growth rate, in turn, reduces the need for the high interface temperature gradients required to maintain growth stability in vertical ribbon growth. The gradients in the vertical methods are the cause of high thermoelastic stresses and set practical productivity limits when low defect densities and flat ribbon are required. Details on the process limits affecting the horizontal growth techniques may be found in other publications [45, 46]. We next give a description of each of the techniques listed in Table 6.3.

WEB. WEB is grown directly from melted silicon in a crucible with no shaping device (Figure 6.21) [47]. A dendritic seed or button is lowered into a supercooled melt. The seed spreads laterally to form a button. When the seed is withdrawn, two secondary dendrites propagate from the ends of the button into the melt, forming a frame to support the freezing ribbon. The dendrites grow into the melt that has been supercooled by several degrees. Very accurate melt temperature control is required in order to maintain the supercooled interface condition and prevent "pull-out", whereby the growth terminates by voiding of the meniscus. The width of the ribbon is controlled by the position of the two dendrites that support the liquid film. The growth velocity is determined by the rate of removal of the latent heat into the ribbon and of the heat conducted through the melt through the meniscus. Typical growth rates are from 1 to 3 cm/min.

In vertical ribbon growth, the meniscus contains the suspended melt volume that connects the bulk melt to the growth interface and crystal. Its shape and the heat conduction taking place within it critically affect impurity segregation and the crystallisation

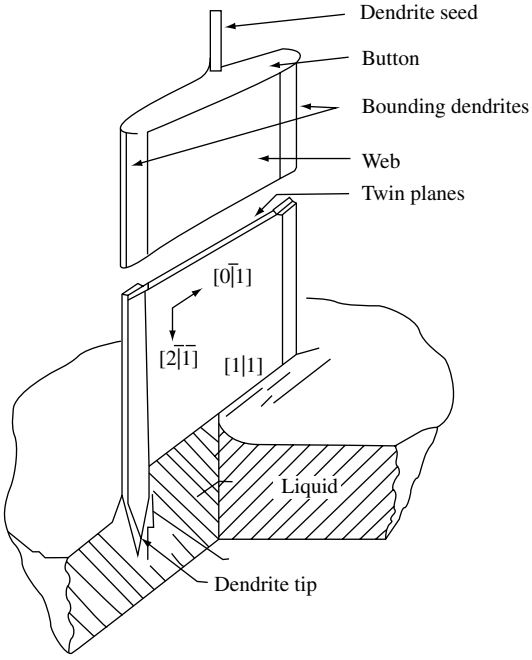


Figure 6.21 Schematic of Dendritic Web (WEB) growth process for ribbon

conditions and shape of the crystal. The meniscus height, h, away from the influence of the dendrites, is fixed by the surface tension, liquid-silicon contact angle and liquid density. This can be calculated from the solution of the Young–Laplace equation requiring a contact angle of $\Theta = 11^\circ$ at the liquid–solid interface that gives

$$h = a[1 - \sin(\Theta)] \quad \text{where} \quad a = (2\sigma/\rho g)^{1/2}$$

where $\sigma = 720$ dyne/cm is the surface tension, $\rho = 2.53$ g/cm^3 is the density of liquid silicon and g is the gravitational acceleration. Because thermal radiation dominates the heat flow from the ribbon, the geometry of the heat shields and the susceptor lid controls the isotherms in the melt and the ribbon.

Accurate temperature control, within a few tenths of one degree, is necessary to ensure a uniform ribbon width and thickness. The temperature of the melt surface must be constant over the width of the growing web to prevent the dendrites from growing in or out. The dominant impurity in the WEB in production today is oxygen since a quartz crucible is used. Typical WEB thicknesses range from 100 to 150 μm and widths up to 8 cm have been grown. Growth lengths between seedings in pilot production extend to many tens of meters.

EFG. In this technique, the geometry of the ribbon is controlled by a slotted graphite die through which silicon is fed via capillary action (Figure 6.22) [48]. A seed crystal is

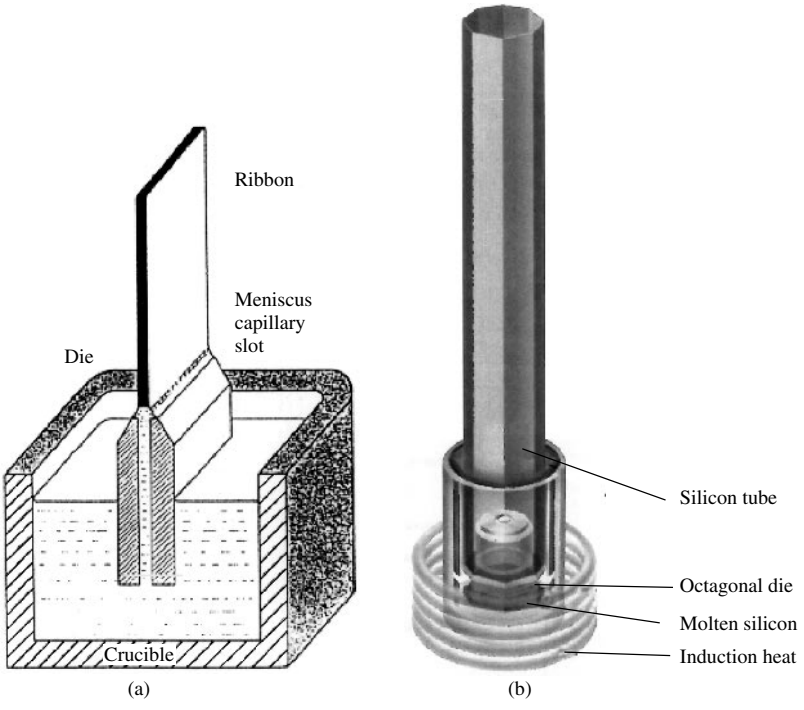


Figure 6.22 Schematics of Edge-defined Film-fed Growth (EFG) growth process: (a) ribbon die and crucible configuration and (b) octagon configuration

lowered until it contacts the liquid in the capillary. The liquid spreads out over the top of the die to the edges where it is pinned by surface tension. The seed is withdrawn, pulling the liquid up while more liquid flows upward through the capillary. As the ribbon is withdrawn, the liquid freezes on the solid crystal. The die and the crucible are integral, that is, made of the same piece of graphite. The thickness of the sheet material is fixed by the width of the die top, distance between the die tip and melt level, meniscus shape, heat loss from the sheet and the pull rate. The shape of the liquid–gas interface, or meniscus, which connects the die to the solidifying ribbon, is described by the Young–Laplace or the capillary equation. As with WEB, the growth rate is controlled by how fast heat can be conducted away from the interface and lost by radiation or convection from the solid crystal. Growth is self-stabilising because the meniscus height increases with an increase in pull rate. The curvature of the meniscus causes the thickness of the crystal to decrease. This increases the rate of heat removal per unit area of the interface, thus increasing the growth rate until it is again equal to the pull rate.

The dominant impurity in EFG ribbon is carbon, which is in supersaturation. Temperature control of a few degrees along the interface is sufficient to prevent ribbon pull-out or freezing of a growing ribbon to the die top. Over time, the die becomes eroded affecting ribbon properties and leading to a non-uniform ribbon thickness and growth difficulties.

Ribbons with thicknesses from 400 μm to as little as 100 μm have been grown. Rather than a single flat ribbon, hollow EFG polygons are grown to enhance the rate of throughput. The favoured geometries for commercial development today are octagons with 10-cm- or 12.5-cm-wide faces, equivalent to growth of up to a 100-cm-wide ribbon from a single furnace. Various closed geometries, including nonagons with 5-cm faces, and large-diameter cylinders have been grown. Growth velocities for the EFG octagon are 1.7 cm/min. The relationships between the EFG process parameters and the silicon ribbon characteristics, including thermal stress and the influence of impurities and defects on the quality of the material, have been extensively examined and are reviewed in Reference [49].

An extension of the EFG process to growth of 50-cm-diameter cylinders has recently been demonstrated [50]. An example of such a cylinder 1.2 m in length is shown in Figure 6.23. The cylindrical geometry offers some relief from the large thermoelastic stresses generated in plane ribbon. This allows consideration of higher productivity furnaces from a combination of larger perimeters and potentially higher growth speeds. Growth of EFG cylinders with average wall thickness down to 100 μ has been demonstrated, and solar cells have been made on this material [51].

STR. In this technique, ribbon growth takes place directly from a pool of melted silicon without a die (Figure 6.24) in a process mirroring the WEB geometrically. Rather than dendrites, as with WEB, the position of the ribbon edges in STR is maintained by two strings fed through holes in the bottom of the crucible. The strings are drawn upward out of the melt to support the meniscus and the ribbon, and their pull rate determines the growth speed of the ribbon. The thickness of the ribbon is controlled by surface tension, heat loss from the sheet and pull rate. An important difference of the STR process from WEB growth is that the constraints of maintaining propagating dendrites and a supercooled melt are eliminated, and this relaxes the high degree of temperature control required in the WEB furnace. The high meniscus, 7 mm (see Equation 2), allows simple control of

Figure 6.23 Experimental 50-cm-diameter EFG cylinder exiting from furnace

the growth process and maximises its stability to mechanical and thermal fluctuations. Depending upon the wetting qualities of the strings and their diameter, the meniscus height at the strings near the edges differs from that at the centre, and it is usually much lower at the edges [52, 53].

For comparable thicknesses, the growth velocities of STR are similar to EFG and WEB. Careful adjustment of the growth parameters can allow very thin ribbon, down to 5 μm, to be grown [54]. Generally passive after heaters are used, but some work on an active after heater has been carried out to allow low-stress, 100-μm-thick ribbon to be grown. This material was sufficiently flat to be made into solar cells. Because of the concave downward meniscus curvature at the string, any grains nucleated at the strings can propagate into the ribbon.

RGS. In this growth technique, the silicon melt reservoir and die are placed in close proximity to the top surface of a substrate, on which the ribbon/foil grows. The substrate may be graphite or ceramic (Figure 6.25) [55]. The principle is to have a large wedge-shaped crystallisation front. The die contains the melt and acts to fix the width

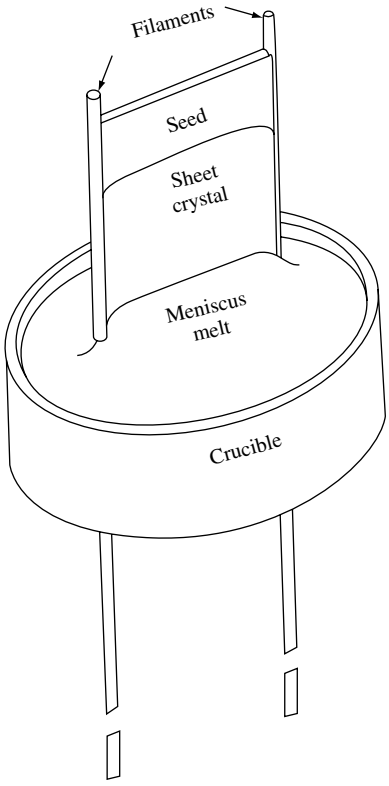


Figure 6.24 Schematic of String Ribbon (STR) growth system

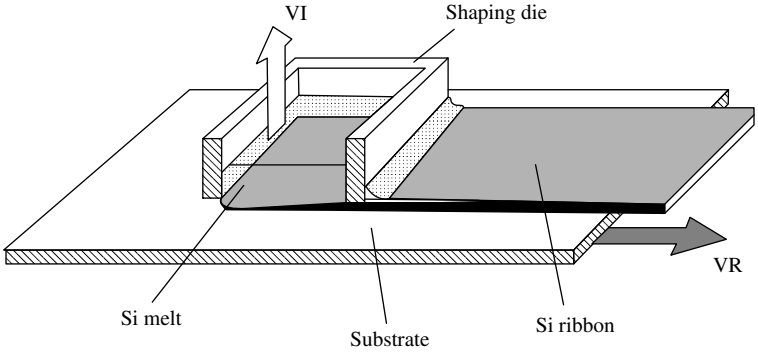


Figure 6.25 Schematic of Ribbon Growth on a Substrate (RGS) configuration

of the foil. The thickness of the foil is controlled by the heat-removal capacity of the substrate, pull rate and surface tension. The direction of crystallisation and growth are nearly perpendicular. The area of the growth interface now can be very large compared to the foil thickness. The latent heat is extracted by conduction into the substrate. The thermal gradients near the interface are small, thus reducing thermally induced stress in

the wafer. Growth rates from 4 to 9 m/min have been demonstrated. One example was an 8.6-cm-wide foil, 300-μm thick, grown at 6.5 m/min.

An important goal in the R&D phase of RGS has been to make a substrate that can be reused. After cooling, the silicon foil may be separated from the substrate by stresses arising from differences in thermal expansion between substrate and silicon. Experimentation with coated foils is in progress and offers the most promise in providing a cost-effective reusable substrate. Thicknesses between 100 and 500 μm have been grown. By working with the lower thermal gradients in the foil thickness direction, but still large enough for rapid growth, fluctuations in the pulling speed and gradient only affect the foil thickness slightly [55].

SF. The details of the SF process are proprietary. The silicon crystal is grown in a thin layer directly upon either an insulating or a conducting substrate, with a barrier layer that promotes nucleation [56]. In the case of an insulating substrate, the barrier layer must also act as a conductor to collect the current generated in the cell. In the case of a conducting substrate, the substrate can also act as an electrical conductor if *vias*, or holes, are provided to connect the thin silicon crystal layer and the substrate. The SF thin film and barrier layer do not separate from the substrate on cooling as in RGS, but become the active part of the solar cell. The grown polycrystalline silicon layer is made very thin ($\ll$100 μm), thus reducing the amount of silicon required. Currently, layers of 20-μm thickness are under development. A variety of substrate materials have been used including steel, ceramics and graphite cloth [56, 57]. It is necessary that the barrier layer prevent the transport of impurities from the substrate into the silicon. The barrier layer allows wetting and nucleation during growth. It should also act to electrically passivate the back surface and have a high optical reflectivity.

An insulating barrier layer has been reported that promotes growth of large columnar grains (greater than 1 mm) through the thickness of the grown SF silicon film [56]. As-grown films on coated ceramic substrates exhibit very low diffusion lengths of less than 10 μm. The new barrier layer and the substrate result in longer diffusion lengths, 20 to 40 μm, and the silicon has an improved response to phosphorous gettering.

6.5.2 Productivity Comparisons

Ribbon crystal growth technology for production of silicon wafers has been historically faced with the evaluation of the trade-off between bulk electronic quality and throughput (productivity per furnace). The choice of crystal growth conditions is made on the basis of wafer cost parameters and the premium imposed by the marketplace on solar cell efficiency. Material quality that can translate into high solar cell efficiencies has always been a primary market driver guiding ribbon growth process development. Ribbon wafers have inherently lower wafer production costs than those obtained from directionally solidified and cast ingots, or Cz boules, because ribbon growth avoids the large material losses due to sawing, which exceed 50% of the starting feedstock. The ribbon geometry has an additional cost advantage in that high levels of radiative cooling allow very rapid pulling rates. On the other hand, the higher wafer cost for the cast ingot or Cz boule production methods demand that these products maintain an advantage in bulk electronic quality, and higher solar cell and module efficiencies, in order to stay competitive with respect

Table 6.4 Single-furnace performance metrics for ribbon technologies under development and in commercialisation

Method/ parameter	Pull speed [cm/min]	Width [cm]	Throughput [cm^2/min]	Furnaces per 100 MW[a]
WEB	1–2	5–8	5–16	2000
EFG Octagon	1.65	8 × 12.5	165	100
STR	1–2	5–8	5–16	1175
SF	[b]	15–30	[b]	[b]
RGS	600–1000	12.5	7500–12 500	2–3

[a]Furnace data are taken from Reference [58], where throughput is normalised for comparison purposes to an overall yield of 90% and cell efficiency of 15% for all processes
[b]Pulling rate parameters for the SF process are not available

to ribbon technology. Superior electronic quality is generally achieved at the expense of throughput in bulk crystal growth from the melt.

A summary of performance metrics for ribbon technologies currently under development is given in Table 6.4. A critical driving parameter in technology development of ribbon methods for large-scale manufacture and commercialisation is the productivity per furnace. Productivity governs the capital cost of installed capacity and direct labour costs, which constitute significant barriers to ongoing commercialisation on a large scale for all ribbon technologies.

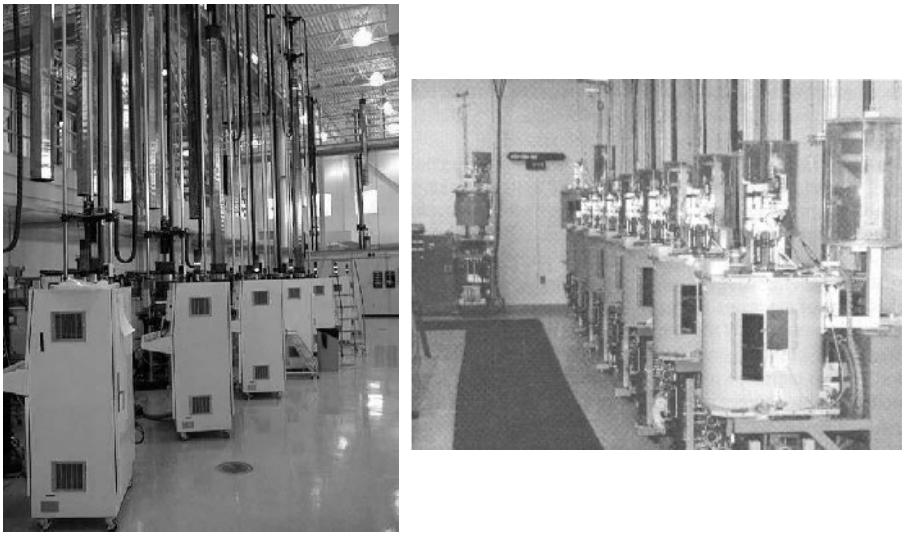
6.5.3 Manufacturing Technology

Table 6.4 shows that development of ribbon technologies is proceeding along two distinct paths. WEB and STR rely on low furnace cost to remain competitive in wafer costs. Development of SF and RGS technologies is focused on achieving superior throughput per furnace.

Scaling of ribbon factories significantly beyond the manufacturing levels practised now, for example, 100 MW, poses different challenges for technology development in these two cases. The low throughput ribbon furnace (WEB, STR) requires a simple and low-cost furnace design, a high level of automation and low infrastructure costs. In contrast, high reliability and uptime of furnaces and the growth process are most critical for the high throughput technologies SF and RGS. EFG technology development is moving in a direction that is trending towards the middle of these two extremes.

Examples of commercial installations and equipment now in manufacturing for EFG and STR technologies are shown in Figure 6.26. Figure 6.26(a) pictures a group of furnaces in the EFG octagon manufacturing line, with a high bay area to accommodate the 5.4-m octagon growth lengths. EFG wafers of 10-cm width and of 10- or 15-cm lengths are standard products and are cut from the octagon tubes using high-speed lasers (not shown). More detail on this technology is given in Reference [59].

Single ribbon furnaces for the growth of 8-cm-wide ribbon of the STR manufacturing line are shown in Figure 6.26(b). Ribbon sections up to a meter long are scribed



(a) (b)

Figure 6.26 Manufacturing crystal growth equipment in commercialisation for (a) EFG and (b) STR technology

from the ribbon while it is growing, and then further cut into wafers of 10-cm length prior to processing.

WEB, SF and RGS ribbon technologies all are in various stages of R&D and pilot demonstrations leading to commercialisation. SF is perhaps the closest to successfully scaling up the technology, as a wider (20 cm) and higher throughput furnace is reaching the final demonstration phase. WEB is basing its expansion to a 1- to 2-MW pilot operation on a single ribbon furnace for producing 5-cm-wide wafers. RGS is moving towards the use of 12.5-cm-wide ribbon in which high sustained throughput technology and consistent high material quality needs to be demonstrated.

6.5.4 Ribbon Material Properties and Solar Cells

Except for WEB, all the growth processes produce multicrystalline ribbon. WEB ribbon grows with (111) crystallographic faces (see Figure 6.21). It typically does not have any grain boundaries, but has a single multiple-twin boundary located about mid-way through the ribbon thickness. Each (111) surface is made up of a single grain, and the dislocation density is the lowest of any ribbon, 10^3 to $10^4/cm^2$.

For the other two vertical ribbon growth cases, EFG and STR, extraneous crystals are generated most often at the sides of the ribbon (i.e. octagon tube corners) and propagate along the growth axis of the ribbon. These crystals form elongated grains often many centimetres in length along the growth axis, and which extend through the ribbon thickness. In EFG, the grains are interspersed with numerous twin boundary arrays. The grains at the ribbon edge in STR are generally smaller than in the centre. Because the meniscus near each string is concave downward, the grains nucleated at the string can

propagate into the ribbon centre. In both EFG and STR, the grain dimensions typically are large compared to the ribbon thickness and the as-grown diffusion length, and the charge collection and solar cell efficiency are minimally influenced by grain boundary recombination.

For SF and RGS, the substrates provide the dominant nucleation sites for crystals. The grains usually are columnar and extend through the ribbon thickness with dimensions that can be made large compared to the diffusion length with proper adjustments of the pulling speed and interface inclination.

Fast movement of the solid–liquid interphase reduces the ability of the freezing process to segregate impurities to the melt. This is represented in Table 6.5 together with the crystalline aspect and the dislocation density of the different technologies.

Stresses produced by thermal gradients during growth generate most of the intragranular dislocations in ribbon material. In the best quality EFG material, it has been shown that the loss in background current is highly correlated with the dislocation density and not grain boundaries [60]. It is not clear if the intrinsic qualities of the dislocations act as recombination centres or if the associated impurity cloud is responsible. Dislocations decorated with SiO_x precipitates have been reported to limit the lifetime in WEB [61] and RGS material [62]. Recent photoluminescence studies suggest similar causes for dislocation recombination activity in EFG material [63].

A critical parameter for solar cell efficiency is the ribbon thickness. As shown by Bowler and Wolf [64], an optimum thickness for peak efficiency occurs. This thickness is dependent on the fabrication technique and material properties, including front and back surface recombination velocities, minority-carrier lifetime and base resistivity among other parameters. For a "typical" $n^+ pp^+$ structure with a 200-μm diffusion length, L_d, a back surface field and a single layer anti-reflection coating, the optimum thickness region consists of a broad peak near 80 μm (Figure 6.27) as calculated using PC-1D [65]. For a 100-μm L_d the optimum thickness peaks at about 50 μm and for a 400-μm L_d it is near 120 μm. A front surface recombination velocity of 10^5 cm/s is assumed.

Table 6.5 Comparison of silicon ribbon material characteristics. In all cases the columnar grains extend through the thickness of the ribbon. An equilibrium segregation coefficient of $k_0 \sim 10^{-5}$ is typical of the most detrimental impurities for ribbon bulk lifetime

Material	Crystallinity	Dislocation density [1/cm^2]	Effective segregation	Thickness [μm]
EFG	Columnar grains in growth direction	10^5–10^6	$k_0 < k_{eff} < 10^{-3}$	250–350
WEB	Single (111) face central twin planes	10^4–10^5	$k_0 < k_{eff} < 10^{-3}$	75–150
STR	Columnar grains in growth direction	5×10^5	$k_0 < k_{eff} < 10^{-3}$	100–300
SF	Columnar grains through thickness	10^4 to 10^5	$k_{eff} < 1$	50–100
RGS	Columnar grains through thickness	10^5–10^7	$k_{eff} < 1$	300–400

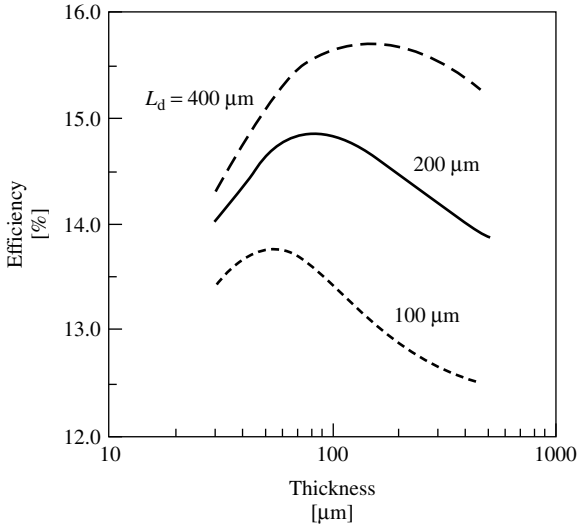


Figure 6.27 Solar cell efficiency versus thickness. (See the text for a description of the solar cell parameters)

The thickness of WEB and SF is closer to the optimum than the other three ribbon growth techniques. Light trapping will move the optimum to a thinner base, but such optical structures on multicrystalline ribbon are not yet practical. For growth on a substrate, it is possible to texture the substrate to trap light. This has been shown on SF wafers [57].

Solar cell fabrication processes used for conventional Cz and cast material wafers are commonly applied to silicon ribbon. If the ribbon is doped *p*-type with boron, the *n*-type emitter typically is formed by phosphorus diffusion either from $POCl_3$, PH_3 or a spin-on source. Front contacts are usually screen-printed or evaporated with diffused or alloyed aluminium as back contact to produce a back surface field. A double or single layer anti-reflection coating may be used. For SF grown on an insulating substrate, contact with the back surface requires etching holes to allow contact with the conducing barrier layer. Table 6.6 summarises material characteristics and solar cell performance potential of the various forms of ribbon material. Boron dopes the ribbon *p*-type. Antimony can be used to produce *n*-type material as reported for WEB.

Table 6.6 Some "best" solar cell efficiency levels for various ribbon technologies

Material	Resistivity [Ω cm]	Carbon [1/cm^3]	Oxygen [1/cm^3]	Efficiency [%]
EFG (Reference [66])	2–4, *p*-type	10^{18}	$<5 \times 10^{16}$	15–16
WEB	5–30, *n*-type	Not detected	10^{18}	17.3
STR	1–3, *p*-type	4×10^{17}	$<5 \times 10^{16}$	15–16
SF (Reference [67])	1–3, *p*-type	5×10^{17}	5×10^{17}	16.6
RGS (Reference [68])	2, *p*-type	10^{18}	2×10^{18}	12.0

Ribbon cell processing, nevertheless, needs to recognise the unique growth constraints of all of the techniques. As noted above, a common material characteristic for ribbon materials historically has been the compromised as-grown bulk electronic quality, dictated by the development of desired high-throughput growth configurations. This strategy has its base in a commercial demand for very low cost wafers that must compete at relatively low volumes with already established dominant products based on single-crystal Cz wafers or directionally solidified and cast ingots. As-grown ribbon diffusion lengths most often are less than 100 μm. To obtain the maximum cell efficiency on this ribbon, with higher dislocation densities and contaminating impurities than in competitor wafers, a solar cell processing strategy was devised early in the history of ribbon technology development that incorporates special bulk lifetime upgrading steps. For example, bulk lifetime upgrading via aluminium alloying and hydrogen is particularly effective for EFG material [69, 70]. Another approach is to use plasma-enhanced chemical vapour deposition (PECVD) of silicon nitride to generate hydrogen for passivating the silicon bulk [71].

6.5.5 Ribbon/Foil Technology – Future Directions

Ribbon/foil wafer production is poised to move on to face a new round of challenges in the construction of large (50–100 MW) manufacturing facilities for crystalline silicon ribbon wafers. The RGS foil technology, with the greatest potential of all ribbon methods for cost reduction on the basis of a high throughput per furnace, is entering a pilot demonstration phase. This process faces challenges in process and equipment development before it can enter high-volume manufacturing of wafers. In the next pilot phase, we may expect that RGS will demonstrate a consistent material quality sufficient for improving cell efficiency to greater than 12% from the current 10 to 11%; process control capable of reproducibly producing a low stress, regular structure, with a shaped 12.5-cm-wide wafer suitable for high-yield cell processing at about a 300-μ thickness and a reliable prototype furnace with melt replenishment to enable continuous production, which will gain full benefit from the high throughput growth concept.

The future focus of WEB and STR ribbon development is on process automation and capital cost reduction for furnaces and infrastructure based on a concept of a low throughput (per furnace) process. Production will probably grow to between 1 and 10 MW for each of these approaches over the next several years. Process parameters that will be practised in this next round of manufacturing equipment expansion for both of them are narrowed down to a single ribbon per furnace concept with similar throughput parameters – a ribbon width of about 8 cm and a pull speed in the 1 to 2 cm/min range. The WEB ribbon technology is embarking on its pilot expansion with a unique process for the growth and manufacturing of solar cells at a 100-μm wafer thickness. STR is expanding its manufacturing with a 300-μm-thick wafer. Although wafer bulk quality is demonstrated on an R&D level to be capable of achieving 15 to 16% cell efficiencies for STR, and over 17% for WEB, quality and cell efficiency levels on a multi-megawatt scale are yet to be established. Both approaches will attempt to demonstrate the cost-effectiveness of operating on a multi-MW level in the next few years. R&D directions, which would appear to have the most potential for the reduction of wafer material costs for these techniques, are growth of wider ribbons and more ribbons per furnace.

EFG and SF ribbon technology have successfully completed their initial scale up of wafer production to the multi-megawatt level. Process control and equipment reliability improvements, which can drive throughput and yield higher, become increasingly more dominant in determining the manufacturing cost. As throughput per furnace increases, capital cost impact on variable manufacturing costs from the growth furnace decreases. There is pressure on all ribbon technologies to concentrate on reducing the capital cost of the wafer production equipment if the transition to large-scale wafer manufacturing of 50- to 100-MW annual capacity factories is to be sustained.

Process variable ranges are firmly established for the EFG process. Octagon tube length, throughput and wafer thickness parameters will remain within the ranges given in Table 6.4 for the next generation of equipment, while octagon face width, and hence the EFG wafer dimension, will increase from 10 to 12.5 cm. The major thrust in R&D on the EFG process in this phase will be on process control and process and equipment automation.

The benefits of the savings in silicon feedstock and potential gains in cell efficiency with a reduction of the ribbon/foil thickness are well understood for all these technologies. However, the pressure to carry out R&D in this direction for the case of wafers made from ribbons is not as acute as for conventional crystalline silicon wafer manufacturing methods because of the large benefit in feedstock savings already realised for ribbons on account of their favourable geometry. The R&D for the next generation of vertical ribbon technology beyond about five years will target the demonstration of production methods for very thin wafers. A strong motivator driving thickness reduction will be the pressure to increase the cell efficiency, which is seen to be capped in the 16 to 17% range (see Table 6.6) for current cell designs and wafer bulk quality. Low-cost cell designs, which can break this barrier and achieve desired targets of 18 to 20% for ribbon, are most easily found for thinner wafers, but this also requires improvements in bulk electronic quality to be achieved concurrently.

The major problem in this development for all vertical growth techniques will be to find methods to reduce the effects of thermal stress. At present, the only means by which this can be done is to reduce the pull speed. The cylinder geometry has the potential to offer some relief to the EFG process at the expense of having to work with thin curved wafers in cell and module processing. Although thermal stress is not a problem with substrate-assisted growth techniques, there probably will be a trade-off between good bulk quality with large grains and throughput.

6.6 NUMERICAL SIMULATIONS OF CRYSTAL GROWTH TECHNIQUES

Commercial finite element simulation tools for structural analysis in computer-aided engineering started to develop at the beginning of the seventies. Today, simulation tools are an essential part in various industry productions; see crash test simulation for automobile development or airflow simulations in the aerospace industry. As an advanced application the descriptions of whole production processes are the goal of the strategies for simulations. If these strategies are successful, computer modelling opens the opportunity to shorten development time for production facilities, to reduce the costs for the

engineering and to speed up process optimisation. In this chapter we will report on those simulation tools, various thermal models and examples of numerical simulations of silicon crystallisation processes.

6.6.1 Simulation Tools

Numerical simulation tools can be distinguished in universal and special-purpose programs. Examples of commercial universal-purpose programs are ABAQUS [72], ANSYS [73] and MARC [74] with a wide range of applications in structural analysis, thermal and fluid-flow simulations or electromagnetic field simulations. The number of special-purpose programs cannot be estimated seriously. Many universities and companies are working with specially developed software tools to obtain solutions of their specific problems. Recently, the large commercial programs both compromise and enable the user to add their specific subroutines to a program run.

The main structure of most of the simulation tools is similar: A pre-processing is designed to define the initial and boundary conditions of a simulation run and includes the generation of the simulation domain (finite element mesh) as well as a set of physical data that describes the material properties. The main-processing is normally not interactive and contains the solver of the mathematical formulations. The post-processing visualises the simulation results.

The demand for simulation tools depends on the complexity of the physical problem or on the technical process that the user wants to simulate. In general, the description of all physical relationships is reachable only in relatively simple and well-known problems. The full description of an industrial production facility by numerical simulations is not possible today, and neither is it reachable in the near future because too many details are too complex to be described by the numerical models. Therefore, the development of useful simplifications is one of the important keys to a successful simulation. This demand requires an integrated teamwork between the user of a simulation tool and the operators at the production facility and other process specialists.

Not the another important requirement is the validation of simulation results by experimental data. At least two experiments are necessary to validate simulation results concerning the process behaviour of a production facility. This means that the simulation model should be validated by measurements during a standard process and in a worst-case scenario to ensure the correctness of the results in an enlarged area of validity. Normally, these experiments are expensive and difficult to realise during a running production, but otherwise, running a non-optimised production would be quite more expensive. Anyhow, the validation of simulation results is necessary to ensure the success of the simulation method.

6.6.2 Thermal Modelling of Silicon Crystallisation Techniques

The wafer material for crystalline silicon solar cells can be divided into those from ribbon and bulk crystals. For most of wafer production processes, numerical simulations are in use to describe the thermal conditions during the crystallisation. In the case of ribbon crystals, only the EFG [75, 76] and the STR process [77] have reached a market

production. The RGS process [78] is now in preparation for a commercial production. The Cz crystal-pulling technique is the standard process for microelectronic single-crystal wafers and covers an essential part of the PV market share [79, 80]. The TriSi crystal is a new variation of this process, especially for photovoltaic applications [81]. The characteristics of ingot crystallisation can be explained by the shape of their liquid–solid interface. Anyhow, today's ingot crystallisation goes more and more towards a mostly planar solidification. For the use of numerical simulations of the Cold Wall process, see [82, 83]; for the Heat Exchange Method (HEM), see [84] and for the Solidification by Planar Interface (SOPLIN) processes, see [85, 86].

To simulate the temperature history during crystallisation, various thermal effects must be taken into account. In Figure 6.28 the scheme of thermal conditions for the ribbon growth and ingot crystallisation is presented. The biggest difference between the two is the strong variation of the cooled surface to volume relation (SV) during crystal growth. This relationship can be used to qualify the cooling behaviour of the different crystals in an equivalent surrounding. For ribbon growth SV is given as 2/ribbon thickness and for ingots as 1/ingot height. The high number for ribbon growth (e.g. SV = 66/cm) means that the surface affects the crystallisation, while the low number for an ingot geometry (e.g. SV = 0.033/cm) shows that volume effects are more important for crystallisation. By this, the SV parameter characterises the requirements for the modelling of different crystallisation techniques. In the case of bulk crystallisation, the latent heat at the liquid–solid interface must be lead away by a heat sink at the bottom of the ingot. By this, the crystallisation is propagated by a conductive heat flow through the solid ingot volume and the temperature gradients inside the volume have to be simulated with high attention. In the case of ribbon growth, heat flow by convection and radiation at the silicon surface is the dominant heat-transport mechanism to lead away latent heat and propagate the solidification. Therefore, simulation results are very sensitive to heat-transition coefficients and the emission behaviour at the ribbon surface.

Furthermore, both techniques can be distinguished into quasi-steady state and moving boundary processes. Assuming a constant pulling speed, the ribbon growth is

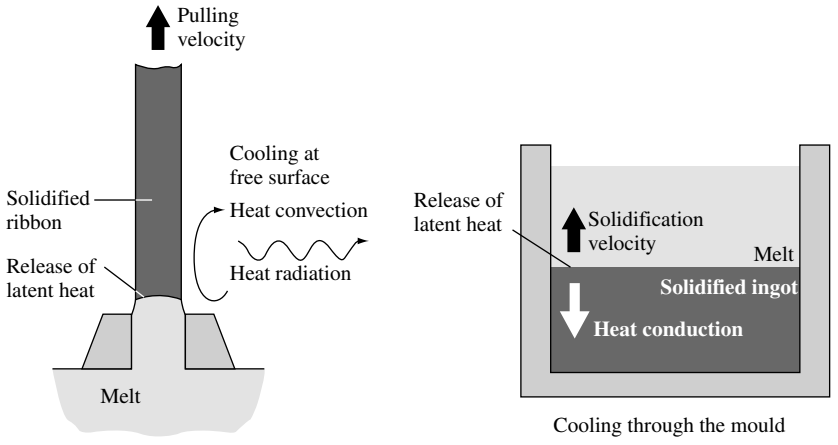


Figure 6.28 Scheme of thermal effects during ribbon growth and ingot crystallisation

characterised by a steady-state temperature field and the liquid–solid phase boundary can be modelled by a fixed-temperature boundary condition, as the silicon melting temperature of 1410°C. In the case of the ingot casting, the phase boundary moves through the crystal and the release of latent heat can be modelled by an enthalpy formulation. By this, the release of the latent heat of finite elements can be taken into account directly after their total solidification, or the fraction of latent heat must be considered for partly solidified elements [87, 88]. The importance of an accurate modelling of the release of latent heat may become more clear by estimating the crystallised volume rate in typical ingot processes to be around 9000 cm^3 per hour, which means a latent heat source of more than 8 kW at the location of the phase boundary. Pulling one 10-cm-wide ribbon, the crystallised volume rate is about 30 cm^3 per hour with a latent heat release of 0.03 kW.

The Czochralski and TriSi crystal-pulling techniques can be classified between ribbon and ingot crystallisation. The temperature profile can be assumed to be stationary and the SV parameter, given as 1/crystal diameter, lies, for example, in the range of 0.066/cm.

In general, the heat flow in silicon during crystallisation can be described by the heat-transport equation [89–91]:

$$\rho c_p \frac{\partial T}{\partial t} = \lambda \nabla^2 T + L \frac{\partial f_c}{\partial t}$$

with the silicon data:

density of solid silicon	$\rho_{(1410°C)}$	=	2.30 [g/cm^3]
density of liquid silicon	$\rho_{(1411°C)}$	=	2.53 [g/cm^3]
heat capacity	$c_{p(20°C)}$	=	0.83 [J/g K]
	$c_{p(1410°C)}$	=	1.03 [J/g K]
heat conductivity	$\lambda_{(20°C)}$	=	1.68 [W/cm K]
	$\lambda_{(1410°C)}$	=	0.31 [W/cm K]
latent heat of phase change	L	=	3300 [J/cm^3]

The time t and the temperature T are variable and result from the simulation. For the moving boundary case the solid fraction f_c becomes important. This parameter depends on the finite element temperature and varies between zero for a completely liquid finite element and one for a solid element.

Additionally to these material properties and the heat flow mechanisms in the silicon material, the description of the internal furnace construction must be taken into account to perform simulations of crystallisation facilities. This includes the geometrical description and material properties of the internal set-up as well as the radiative heat exchange with heaters and cooling facilities.

6.6.3 Simulation of Bulk Silicon Crystallisation

As an example of the temperature simulation of silicon ingot crystallisation, the SOPLIN casting technique is selected. To simulate this process, a finite element mesh of about 230 000 elements was built to describe the furnace geometry. This mesh includes the silicon ingot, the mould, all insulation materials and active heating and cooling facilities,

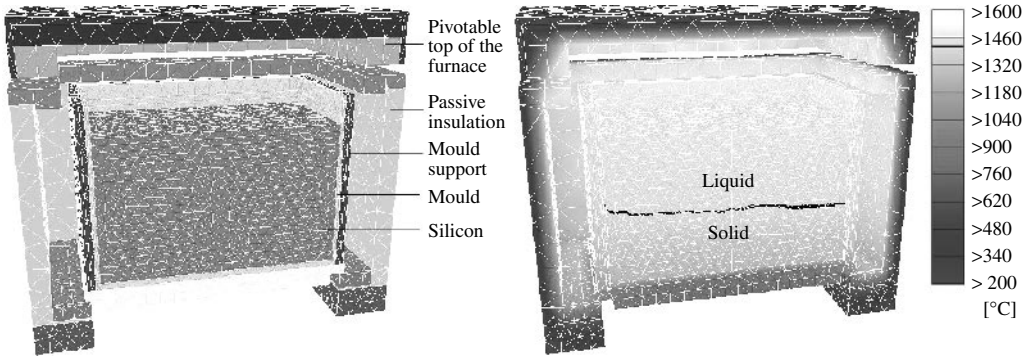


Figure 6.29 Finite element geometry of an ingot casting furnace and simulated temperature distribution during a reference process. The liquid–solid interface is marked by the black line

as shown in Figure 6.29. Because of confidentiality agreements with the industry, the heating and cooling systems are not shown in detail in this figure. All heat conductance and capacity effects as well as the non-stationary release of latent heat are taken into account. All material contact regions between silicon, mould or insulation materials are modelled by heat flow–resistance parameters. To describe the heat flux by radiation inside the furnace, a view-factor model is included in the software. All material data are treated in their temperature dependency and all the internal control systems of the furnace are added to the simulation software.

To start one simulation run, only the cooling water temperature and the time-dependent process control information are necessary as input data, as they are entered in the crystallisation furnace. Output from one calculation is the three-dimensional temperature history in the furnace, beginning after pouring the melt and ending with a homogeneous temperature of about 300°C inside the ingot. This calculation needs less than 6 h on a common one-processor workstation.

In Figure 6.29, an example of the temperature distribution during a reference process is shown in the middle, cut through the furnace. The liquid–solid interface is marked by the melting temperature isotherm. The solidification front is mostly flat, and a slight non-symmetry is caused by the specific construction of the heating system. These simulation results are verified in an experimental crystallisation furnace with good agreement to the measurement in the ingot volume during crystallisation.

In general, the shape of the solidification front is controlled by the lateral heat flux, while the vertical heating and cooling conditions control the solidification velocity. To investigate these general reflections for the described furnace, variations of the process control were simulated. In Figure 6.30, two variations are presented. By a 30% raise of heating power at the side walls of the ingot, the shape of the solidification front becomes more convex. Otherwise, a reduction of heating power by about 20% turns the solidification front to a more concave shape. Additionally, to this more or less predictable effect, simulation results show an increase in the solidification time for the convex crystallisation of 44% and a 30% reduced processing time for the concave solidification. Both effects are due to the total varying power input in the furnace. These simulation results enable

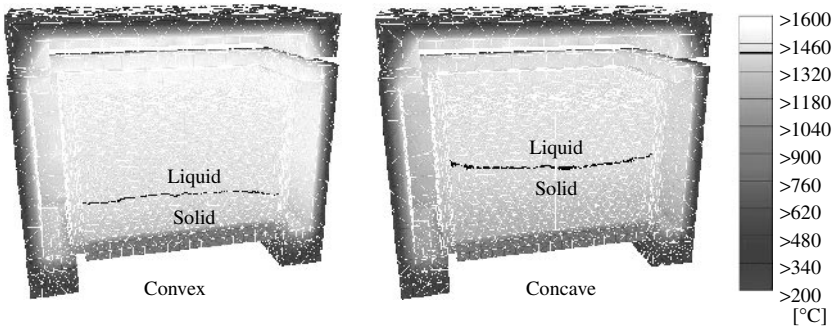


Figure 6.30 Examples of convex and concave liquid–solid interfaces due to the variation of side wall heating power. Both pictures are taken at the same process time

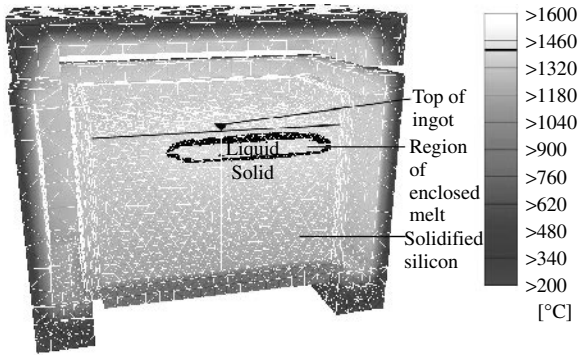


Figure 6.31 Simulation result representing a remarkable decrease of heating power at the top region of the ingot. By this, the solidification time is reduced to half, but solidification ends with an inclusion of silicon melt

the furnace operator to find the balance between material quality, which is known to be high in the case of planar solidification, and process economy.

In Figure 6.31, simulation results are shown, representing a noticeable reduction of heating power at the ingot top. By this, the solidification velocity can be speeded up and the time for solidification is reduced to half. However, in the simulated case study, the solidification ends with an encapsulation of the melt by solidified silicon. Because of the 10% higher density of liquid silicon with respect to the solid phase, this process scenario causes a burst out of melt from ingots volume. This can lead to a crack in the mould and to a damage of the furnace. These case-study simulations can find worst-case process conditions that must be avoided in production. For more simulation results of the SOPLIN process, see [92–94].

6.6.4 Simulation of Silicon Ribbon Growth

As a second example of silicon crystallisation processes, the RGS is taken. The basic idea of this process is the de-coupling of the pulling direction of substrates on which silicon

solidifies and the solidification direction of the silicon itself, as shown in Figure 6.32. By this, a very high production rate of one wafer per second is realisable. For this process numerical simulations were performed describing the crystallisation of the silicon ribbon in further detail. This simulation is realised by a phase-field approach [95]. In Figure 6.33 two nucleation states of the silicon on the substrate are compared by their temperature field in two-dimensional simulations. In the first case a supercooled region in front of the tip of the growing crystal leads to a more dendritic growth mode of the crystal, because the liquid–solid interface is morphologically non-stable. In the second crystallisation mode,

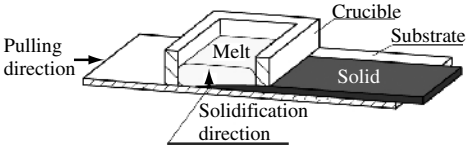


Figure 6.32 Scheme of the RGS process. The latent heat is removed through the substrate. By this, solidification is propagated vertical to the substrate and is de-coupled from substrates' pulling direction

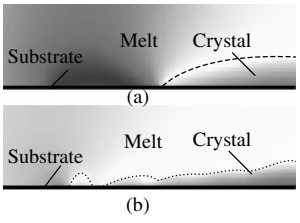


Figure 6.33 Simulated temperature profile on the RGS substrate. Light grey scales indicate high temperatures. The liquid–solid interface is marked with the dotted line. Unstable crystal growth into a supercooled melt at the tip of the ribbon. Nucleation of new grains limits the supercooling and leads to a stable columnar grain growth

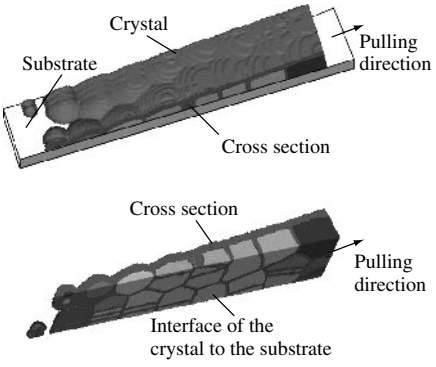


Figure 6.34 Simulation results of the growth of silicon grains on the RGS substrate during solidification. Different grains are marked by different grey scales. The liquid–solid interface is marked by a darker grey scale and envelops the grains. For a better visibility, the melt is not shown in this figure

the supercooling decreases owing to a nucleation of new grains on the substrate surface, which leads to a more columnar growth of the silicon sheet. Both crystallisation modes depend on the surface of the substrate and on the heating power controlled temperatures of the substrate and the melt. Numerical simulations allow investigating this crystal-growth tendency as well as the temperature field at the contact region of the ribbon on the substrate. In Figure 6.34 an example of the simulation of single silicon grain growth on the substrate is given [96]. In this way, numerical simulations can study the grain growth under various temperature conditions and grain-selection mechanisms of silicon crystals.

6.7 CONCLUSIONS

At the present time, the PV industry relies on solar cells made on crystalline silicon wafers, which provide around 90% of the total PV power installed. It is expected that monocrystalline and multicrystalline solar cells will continue dominating the industry for the next 10 years.

With rejects from the microelectronic industry as feedstock, the PV industry grows monocrystalline ingots by the Czochralski technique. Owing to more relaxed specifications than in microelectronics, the throughput of PV Cz pullers can be increased and still produce high-quality silicon, allowing the achievement of 15 to 17% efficient solar cells.

Tri-crystalline silicon (tri-Si) can be grown in standard production Cz growers using a quasi-continuous pulling with multiple recharging with high productivity and feedstock usage. Tri-Si allows slicing of ultra-thin wafers with higher mechanical yield than monocrystalline Si and obtaining solar cells of similar performance.

Multicrystalline Si can be manufactured at a lower cost than monocrystalline Si, but produces less efficient cells, mainly owing to the presence of dislocations and other crystal defects. With the introduction of new technologies, the gap between multicrystalline and monocrystalline solar cells is reducing.

Si ingots are sliced into thin wafers with multi-wire saws, with throughputs of about 500 to 700 wafers per day and per machine. Sawing is responsible for high material losses, and amounts to a substantial part of the wafer production cost. Understanding the microscopic processes of wire sawing allows optimising the technique and improving the sawing performance.

Silicon ribbon wafer/foil technologies have matured in the past decade to where they are serious contenders for competing on a scale equal to that of conventional silicon wafers. Several ribbon technologies have already demonstrated robust and reproducible processes, which have been scaled up to megawatt levels. The next round of expansion will probably reach the 50 to 100 MW factory size for individual technologies within 5 years. Factories of this scale will require considerable development of automated equipment and infrastructure in addition to continuous improvement on the basic process control and material quality. EFG and SF ribbon technologies are most notably in a position today to manufacture wafers on this scale and lead the anticipated growth of the photovoltaic industry.

During the last decade, computer power has been increasing strongly and there is a high progress in the modelling of physical phenomena and in the development of

simulation tools. By this, computer simulations become a powerful tool in science and industrial applications. The simulation results of industrial crystallisation processes that are shown and the detailed study of the crystallisation mode by numerical simulations are some examples of the possibilities today. These numerical simulations offer a wide range of possibilities to increase the knowledge about the basic physics of crystallisation and technical processes. One insistent demand on computer simulations is to close the gap between science and engineering to get a closer picture of reality.

6.8 ACKNOWLEDGEMENTS

This chapter has been coordinated by W. Koch. Section 6.2 has been prepared by A.L. Endrös, Section 6.3 by C. Häßler, Section 6.4 has been prepared by H. J. Möller, Section 6.5 by J. P. Kalejs and Section 6.6 by D. Franke. The editor also wants to recognise the work of C. del Cañizo, senior researcher at his institute (IES-UPM), who greatly reduced the original text to keep it under the budgeted extension without losing readability and homogeneity.

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7

Crystalline Silicon Solar Cells and Modules

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7.1 INTRODUCTION

Crystalline silicon solar cells and modules have dominated photovoltaic (PV) technology from the beginning. They constitute more than 85% of the PV market today, and although their decline in favor of other technologies has been announced a number of times, they presumably will retain their leading role for a time, at least for the next decade.

One of the reasons for crystalline silicon to be dominant in photovoltaics is the fact that microelectronics has developed silicon technology greatly. On the one hand, not only has the PV community benefited from the accumulated knowledge but also silicon feedstock and second-hand equipment have been acquired at reasonable prices. On the other hand, Microelectronics has taken advantage of some innovations and developments proposed in Photovoltaics.

For several decades, the terrestrial PV market has been dominated by *p*-type Czochralski silicon substrates. Continuous improvements in performance, yields and reliability have allowed an important cost reduction and the subsequent expansion of the PV market. Because of the lower cost of mc-Si wafers, multicrystalline (MC) silicon cells emerged in the 1980s as an alternative to single-crystal ones. However, their lower quality precluded the achievement of similar efficiencies to those of Cz, so that the figure of merit \$ W^{-1} has been quite similar for both technologies over a long time (see Table 7.1).

Deeper understanding of the physics and optics of the mc-Si material led to improved device design, which allowed a wider spread of the technology. A combination

Handbook of Photovoltaic Science and Engineering. Edited by A. Luque and S. Hegedus
 ISBN: 0-471-49196-9

Table 7.1 Breakdown of costs of fabrication of single-crystalline (SX) and multicrystalline (MC) solar cells (corresponding to year 1990) [1]

Item	SX	MC
Pure Si	38	38
Ingot formation	115	35
Sawing	77	77
Wafer cost	**230**	**150**
Cell fabrication	80	80
Total components	310	230
Yield	0.95	0.9
Cell cost	**326**	**256**
Module assembling	75	75
Lamination	75	75
Module cost (Euro m^{-2})	**476**	**406**
Efficiency	0.14	0.12
Module cost (Euro Wp^{-1})	**3.40**	**3.38**

Table 7.2 Market share of monocrystalline and multicrystalline solar cells [2]

Year	Cz-Si solar cells		MC-Si solar cells	
	Output [MW]	Market share [%]	Output [MW]	Market share [%]
1996	48.7	55	28.4	32
2000	92.0	32	146.7	51

of improved material quality and material processing has allowed higher efficiencies at a still lower cost, increasing the share of MC in the PV market, well ahead of monocrystalline. Recent evolution of the market can be seen in Table 7.2 [2].

This chapter offers an overview of silicon solar cell and module technology. First, Si properties justifying its use as photovoltaic material are presented. Then, design of Si solar cells is reviewed, highlighting the benefits and limits of different approaches. Manufacturing processes are described, paying special attention to technologies that are currently implemented at the industrial level, mostly based on screen-printing metallization technology. Considerations of ways of improving solar cell technology are also specified. Peculiarities of multicrystalline material are explained in Section 7.6, while other approaches that are already in industrial production are also described briefly. Next, crystalline Si modules are reviewed, pertaining to electrical performance, fabrication sequence and reliability concerns.

7.2 CRYSTALLINE SILICON AS A PHOTOVOLTAIC MATERIAL

7.2.1 Bulk Properties

Crystalline silicon has a fundamental indirect band gap $E_G = 1.17$ eV and a direct gap above 3 eV [3] at ambient temperature. These characteristics determine the variation of optical properties of Si with wavelength, including the low absorption coefficient for carrier generation for near band gap photons [4]. At short ultraviolet (UV) wavelengths in the solar spectrum, the generation of two electron–hole pairs by one photon seems possible, though quantitatively this is a small effect [5]; at the other extreme of the spectrum parasitic free-carrier absorption competes with band-to-band generation [6]. The intrinsic concentration is another important parameter related to the band structure; it links carrier disequilibrium with voltage [7].

At high carrier densities, doping- or excitation-induced, the band structure is altered leading to an increase in the effective intrinsic concentration: this is one of the so-called heavy doping effects that degrade the PV quality of highly doped regions [8].

Recombination in Si is usually dominated by recombination at defects, described with Shockley–Read–Hall (SRH) lifetimes. The associated lifetime τ (which can also be described in terms of diffusion length L) increases for good quality materials. Auger recombination, on the contrary, is a fundamental process that becomes important at high-carrier concentration [9]. The Auger coefficients are reported to be higher at moderate carrier densities due to excitonic effects [10]. Band-to-band direct recombination is also a fundamental process but quantitatively negligible (it is instructive, however, to notice that record-efficiency solar cells have such extraordinarily low SRH recombination levels that they perform as 1%-efficient light-emitting diodes, that is, radiative recombination is significant [11]).

At low and moderate doping, electrons present mobilities about three times higher than holes, both limited by phonon scattering. Impurity scattering dominates for higher doping densities [12, 13]. Carrier–carrier scattering affects transport properties in highly injected material [14].

7.2.2 Surfaces

7.2.2.1 Contacts

Contacts are structures built on a semiconductor surface that allow charge carriers to flow between the semiconductor and the external circuit. In solar cells, contacts are required to extract the photogenerated carriers from the absorbing semiconductor substrate. They should be selective, that is, should allow one type of carrier to flow from Si to metal without energy loss while blocking the transport of carriers of the opposite type.

Direct Si-metal contacts, in general, do not behave this way. As an exception, good hole contacts to highly doped p-Si substrates with aluminum are possible. But the

most used approach is to create heavily doped regions under the metal, p-type for hole extraction and n-type for electron extraction. Majority carriers in this region can flow through the contact with low voltage loss. The transport of minority carriers is described by a surface recombination velocity (SRV), S. Although the SRV is high, limited only by thermal diffusion so that $S \cong 10^6$ cm·s^{-1} [15], the concentration of minority carriers, for a given pn product, is suppressed by the high doping and the flow is reduced.

As will be seen later on, the contact for the minority carriers is usually placed at the front (illuminated) face of the substrate, and the corresponding heavily doped layer is usually called *emitter*. The doped region under the majority carrier contact at the back is called a *Back Surface Field* (BSF).

Recombination at these heavily doped regions is described by the saturation current density J_0 that includes volume and true contact recombination. Their thickness w should be much higher than the minority-carrier diffusion length L so that few excess carriers reach the contact, and the doping level must be very high to decrease contact resistance and the minority-carrier concentration, although heavy doping effects may limit the doping level advisable for such regions. The recombination activity of BSF layers is often described in terms of an effective SRV instead of the saturation current density.

Typical 10^{-13} to 10^{-12} A·cm^{-2} J_0 values are achieved [16, 17]. Diffused phosphorus is used for n-contacts. Aluminum alloying has the advantages over boron for p-contacts that very thick p^+ layers can be formed in a short time at moderate temperatures and that gettering action is achieved [18]. As a shortcoming, the p^+ layer is nonhomogeneous and can even be locally absent; the obtained J_0 is larger than expected for a uniform layer. In comparison to aluminum, boron offers higher doping levels because of a larger solubility [19] and transparency to light so that it can also be used at illuminated surfaces.

Other structures have been tested to obtain selective contacts: metal-insulator-semiconductor (MIS) contacts [20], polysilicon contacts [21] and heterojunction to a-Si or other wide band gap material [22].

7.2.2.2 Noncontacted surfaces

Because of the severe alteration of the bonding of Si atoms, a large number of band gap states exist at a bare Si surface which, acting as SRH recombination centers, make the SRV very large, around 10^5 cm·s^{-1} [23, 24]. In order to reduce surface recombination, two main approaches are followed [25].

In the first one, the density of electron surface states in the gap is decreased. This is accomplished by depositing or growing a layer of an appropriate material that partially restores the bonding environment of surface Si atoms. This material must be an insulator.

Thermal SiO_x is grown in an oxygen-rich atmosphere at the expense of substrate Si atoms at high temperatures around 1000°C. SiN_x is deposited by plasma-enhanced chemical vapor deposition (PECVD) [26] at low temperatures between 300 and 400°C range. The quality of both techniques is very sensitive to subsequent treatments, with hydrogen playing a major role in obtaining low SRV values below 100 cm·s^{-1}.

As a general rule, S increases with the doping of the substrate [23, 24]. It also depends on the injection level and doping type, because the interfaces contain positive

charges that affect the number of carriers at the surface, and because the capture probability for electrons and holes is different [27]. N-type or intrinsic surfaces are usually better than p-type ones. Stability under UV exposure is another fundamental concern.

In the second approach, the excess carrier density at the interface is decreased relative to the bulk. This effect has already been commented upon with respect to contacts and results in a reduced effective SRV at the bulk edge of the corresponding space charge region. It can be produced by charges in the surface layer, by the electrostatics associated to a MOS structure [28] or by doping.

The surface layer can be accumulated or inverted, or, correspondingly, doped with the same or the opposite type of the substrate. Its recombination activity is better described by a constant saturation current density, J_0, whose minimization follows the same rules as mentioned for the contacts if S at the surface is high. On the contrary, if S is low when compared to D/L for minority carriers (with D the diffusion constant and L the diffusion length in the substrate) in the surface layer, it is better for it to be thin or "transparent" to minority-carrier flow ($w < L$). The optimum doping level is a compromise between reduction of the excess carriers, and heavy doping effects and the increase of the SRV with doping. Moderate doping levels are favored in this case. Under passivated surfaces, J_0 values around 10^{-14} A·cm^{-2} are achievable, with phosphorus-doped substrates giving better results than boron-doped ones [16, 17].

In conclusion, recombination at a noncontacted surface can be made much smaller than at a metallized one, and this has a deep influence in the evolution of Si solar cell design.

7.3 CRYSTALLINE SILICON SOLAR CELLS

7.3.1 Cell Structure

Several studies have been carried out to find the limiting efficiency and the optimum structure of a-Si solar cell [29–31]. All avoidable losses are assumed to be suppressed:

1. no reflection losses and maximum absorption as achieved by ideal light-trapping techniques,
2. minimum recombination: SRH and surface recombination are assumed avoidable and only Auger recombination remains,
3. the contacts are ideal: neither shading nor series resistance losses,
4. no transport losses in the substrate: the carrier profiles in the substrate are flat so that recombination is the minimum possible for a given voltage.

The optimum cell should use intrinsic material, to minimize Auger recombination and free-carrier absorption, and should be around 80-μm thick, the result of the trade-off between absorption and recombination. It could attain nearly 29% efficiency at one sun AM1.5 Global, 25°C [30].

This ideal case does not tell us where to put the contacts. To realize Condition 4 mentioned above, the contacts should be located at the illuminated or the front face, closest to photogeneration (Figure 7.1a). Because of metal shading losses this threatens

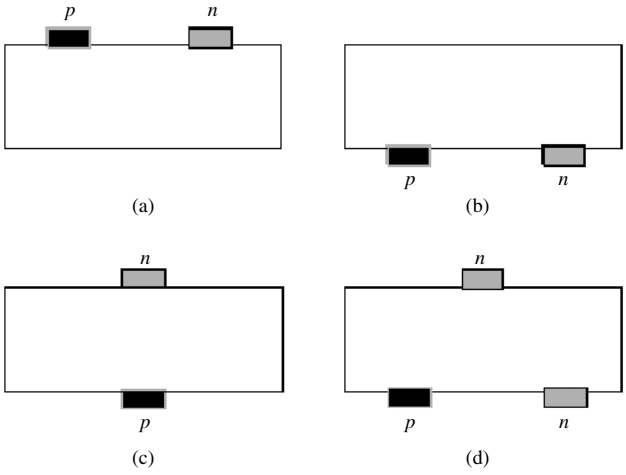

Figure 7.1 Contacting structures: (a) both contacts at the front; and (b) at the back; (c) both faces contacted; and (d) one carrier extracted at both faces. The structures with interchanged *n*- and *p*-types are also possible

Condition 3 mentioned above. This solution is being considered for concentration [32]. Putting both contacts at the back works the other way round (Figure 7.1b). Back-contacted cells exhibit record efficiencies under concentration and demonstrate very high values near 23% at one sun [33].

In most cells, each contact is placed on a different face, which is technologically simpler (Figure 7.1c). Minority carriers in the substrate are usually collected at the front since their extraction is more problematic because of their low density. The diffusion length describes the maximum distance from where they can be collected. Majority carriers can drift to the back contact with low loss. Several designs extract minority carriers both at the front and at the back (Figure 7.1d) [34], thus increasing the volume of profitable photogeneration.

Bifacial cells are designed to collect light incident at both faces, which allows a boost in output power if there is a significant albedo component. They can be implemented with any structure in Figure 7.1 on the condition that both surfaces allow light through [35].

Both 24.7% record-efficiency laboratory solar cells [36] (Figure 7.2a) and mass-produced industrial devices (Figure 7.2b), typically 15% efficient, display the contacting structure in Figure 7.1(c). They will be described in the paragraphs that follow with the aim of illustrating the amplitude and the reasons for the performance gaps between the ideal and the best Si cell, and between this cell and industrial cells.

7.3.2 Substrate

7.3.2.1 Materials and processing

Highest efficiencies are achieved with monocrystalline float zone (FZ-Si) material, which in addition to extreme crystalline perfection shows the lowest contamination levels of both

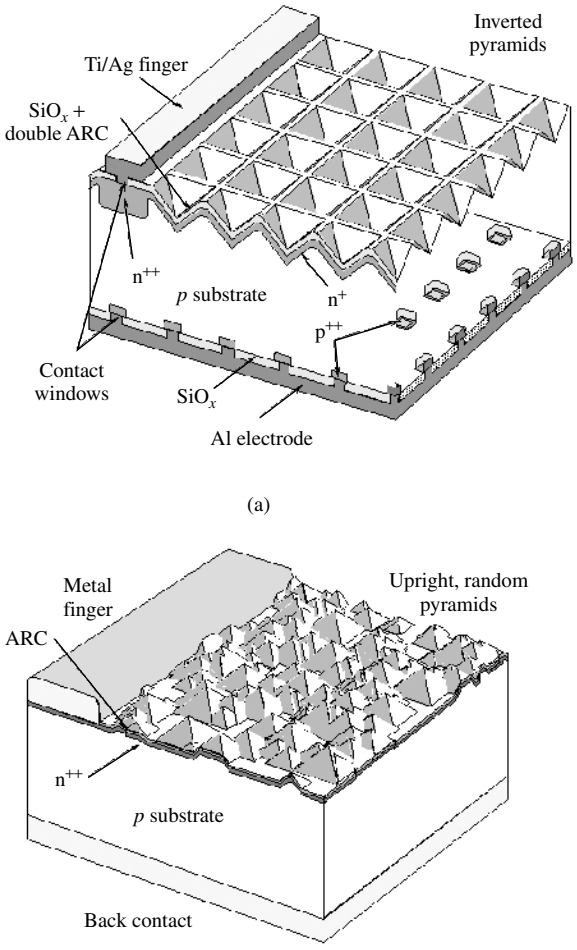

Figure 7.2 (a) Passivated emitter and rear locally diffused (PERL) cell; and (b) industrial cell with screen-printed contacts. (Not to scale)

metallic and light (O, C, N) impurities. This translates into the longest post-processing SRH lifetimes in the millisecond range, but still shorter than the Auger limit. Magnetic Czochralski (MCz) material contains much less oxygen than conventional Czochralski and also allows very high efficiencies to be obtained [36].

Industrial cells use Czochralski (Cz-Si) wafers because of their availability. Cz wafers are also perfect crystals but they contain a high concentration of oxygen that affects lifetime in several ways [37]. Some commercial devices are made on multicrystalline (mc-Si) substrates grown in blocks or ribbons with procedures specially developed for photovoltaics. In addition to crystal defects, such as grain boundaries and dislocations, the potential content of metallics is higher because of lower segregation to the melt during the faster solidification process. As a result, the lifetime of mc-Si is lower.

But lifetime is important at the end of solar cell fabrication during which it can undergo strong variations. This issue is handled in different ways in a laboratory and a factory environment. In the laboratory, measures are taken to maintain long initial lifetimes by avoiding contamination during high-temperature steps: furnace cleaning, ultra pure chemicals and so on. In a rough, industrial environment and with defect-containing (Cz- and mc-Si) materials, the problem is more complex: in addition to contamination from the surroundings, impurities and defects in the substrate move, interact and transform at high temperature. The solution is to integrate gettering steps [38] in the fabrication flow that reduce the impact of contamination, and to tailor the thermal treatments to the peculiarities of the material. Final substrate lifetimes of industrial cells range from 1 to 10 μs.

Gettering techniques eliminate or reduce contaminant impurities in a wafer, and so neutralize the effect of lifetime reduction. Although gettering processes are not always well understood, it is admitted, in general, that in a gettering process a sink region is formed, which is able to accommodate the lifetime-killing impurities in such a way that they are not harmful to the device being manufactured, or at least they are where they can be easily removed.

In solar cell fabrication, we take advantage of the fact that phosphorus and aluminum diffusions, appropriate candidates for emitter and BSF layers, respectively, produce gettering in certain conditions [39]. Other techniques have been explored [40, 41], but their integration in a solar cell process is not so straightforward.

P gettering effect has been proved for a wide variety of P diffusion techniques (spin-on, $POCl_3$, PH_3 etc), provided diffusion is done in supersaturation conditions (i.e. over its solid solubility in silicon). Unfortunately, this leaves a "dead layer" of electrically inactive phosphorus near the surface, which reduces UV response of the cells in case it is not etched away [42]. Another phenomenon related to this supersaturated P is the injection of silicon self-interstitials to the bulk of the material, which is responsible for an enhancement of the gettering effect [43].

When Al is deposited on Silicon (by different techniques such as sputtering, vacuum evaporation or screen printing) and annealed over the eutectic temperature (577°C), a liquid Al-Si layer is formed, where impurities tend to segregate because of their enhanced solubility [44]. They will remain in this gettering layer while cooling, so that bulk lifetime will improve after the process.

Another approach to improve material quality is "bulk passivation", a treatment with hydrogen, for example, during SiN_x deposition, to which some defected materials respond very well [45].

7.3.2.2 Doping level and type

Both laboratory record-efficiency and industrial cells use boron-doped substrates. Rather than fundamental advantages [46], there are practical (properties of P diffusion, easiness of Al alloying) and historical reasons for this preference [47]. However, the situation may change once the role of boron in the degradation of Cz-Si cells under illumination has been established [48].

The optimum substrate doping depends on the cell structure and dominant recombination mechanism. Though intrinsic substrates present the advantage of highest Auger-limiting lifetimes, higher doping is favored when SRH recombination is present, since recombination is proportional to the excess density that decreases, for a given voltage, as doping increases [29]. This is balanced with a reduction of the lifetime itself.

A high doping also helps in minimizing the series resistance losses associated to the transport of carriers to the back face in thick cells with the majority carrier contact at the back.

Doping levels in the 10^{16} cm^{-3} range are found in the substrate of industrial cells. Very high efficiencies have been obtained with both low (1 Ω·cm for PERL cells) and high substrate resistivities, as in the point-contact cells [33].

7.3.2.3 Thickness

From the point of view of electrical performance, the choice of the optimum substrate thickness also depends on the structure and the quality of the materials and involves several considerations. In cells with diffusion lengths longer than the thickness, the most important issue is surface recombination: if S at the back is higher than D/L for the minority carriers in the substrate (around 250 $cm \cdot s^{-1}$ for the best cells), thinning the cell increases recombination at a given voltage, and vice versa. Thinner cells always absorb less light as well, which is attenuated by light-trapping techniques. Passivated emitter and rear locally diffused (PERL) cells were reported to improve when going from 280- to 400-μm thickness because of a (relatively) high rear surface recombination and nonideal light-trapping [49].

The losses associated with the transport of carriers extracted at the nonilluminated face decrease with thinning: in conventional structure cells; this leads to decreased series resistance. In back-contacted cells, both types of carriers benefit from thinning and the trade-off in absorption leads to lower w values, around 150 to 200 μm.

The diffusion length of industrial cells (around 100 μm) is generally lower than thickness. These cells are rather insensitive to thinning because they collect only the generation near the contact and are not affected by rear surface recombination. The driving criteria are cost and fabricability. A thickness in the 200- to 300-μm range is usually employed but there is a clear trend toward thinner wafers for saving expensive silicon material [47], and advanced wafering techniques and procedures to process very thin, large-area substrates without breaking are being developed: light-trapping and back recombination will become increasingly important.

7.3.3 The Front Surface

7.3.3.1 Metallization techniques

Metal grids are used at the front face to collect the distributedly photogenerated carriers. The compromise between transparency and series resistance requires metallization technologies able to produce very narrow but thick and highly conductive metal lines with

a low contact resistance to Si. Laboratory cells use photolithography and evaporation to form 10- to 15-μm metal fingers. Ti/Pd/Ag structures combine low contact resistance to *n*-Si and high bulk conductivity. These processes are not well suited to mass production that relies on thick-film technologies. Ag pastes are screen printed, resulting in over 100-μm wide lines with higher bulk and contact resistance. Laser-grooved buried-grid (LGBG) industrial cells implement a finer metallization technology [50], which will be presented in Section 7.7.3.

Coarser metallization techniques imply higher shading and resistance losses, and restrict the efficiency enhancement that could be achieved by internal cell design.

7.3.3.2 Homogeneous emitters

Under the metal lines, the substrate must be heavily doped to make the contact selective. Usually the doped region, the emitter, extends all across the front surface, acting as a "transparent electrode" by offering minority carriers in the substrate a low resistance path to the metal lines.

When the exposed surface is not passivated (Figure 7.3a), the emitter should be as thin as possible, because the high SRV makes the light absorbed in this region poorly collected, and also highly doped to decrease recombination. On the other hand, a sufficient low-sheet resistance is to be achieved. The solution is to make very thin and highly doped emitters.

If the surface is passivated (Figure 7.3b), the collection efficiency of the emitter can be raised by lowering the doping level thus avoiding heavy doping and other detrimental

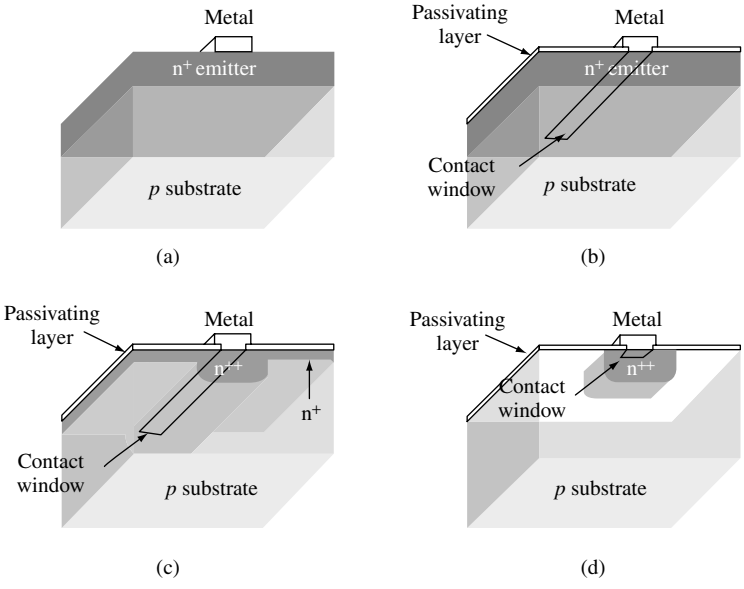

Figure 7.3 Different emitter structures: (a) homogenous emitter without surface passivation; (b) homogenous emitter with surface passivation; (c) selective emitter; and (d) localized emitter

effects. This must be balanced with contact resistance. Etching off of the passivating layer before metallization is usually needed (not in screen-printed cells). To maintain low sheet resistance and diminish recombination at the metallized fraction, the emitter is deep (around 1 μm). Note that the collection of carriers near the surface implies that the emitter is thin in terms of the minority-carrier diffusion length ($w < L$) and so it is very sensitive to surface recombination. Recombination is further reduced, by making the contact window narrower than the finger width, as illustrated in Figure 7.3 [51].

Control of both the surface concentration and the depth of the emitter, is achieved by depositing, in a thermal step, the desired amount of phosphorus or boron (predeposition) and then diffusing it into the substrate (drive-in) during subsequent furnace steps. The MIS solar cell, on the contrary, uses no diffusion for the n region, which is electrostatically induced by charges on top of the surface [20].

The J_0 of the emitter is the average, weighted by the contacted area, of the J_0 of contacted and noncontacted portions.

7.3.3.3 Selective and point emitters

A further improvement involves making separate diffusions for the different regions since the requirements are so different (Figure 7.3c) [52]: a heavily doped and thick region under the contacts, a thin and lowly doped region under the passivating layer. These structures, known as "selective emitters", come at the expense of more complicated processing usually involving photolithographic delineation and alignment of the diffusions (not in LGBG cells to be seen later).

If a very low SRV is possible, it would be best to have no emitter at all since doping always degrades bulk lifetime (Figure 7.3d). Examples are the back point-contact solar cell and the point-emitter design with bifacial contact [53], originally designed for concentration but capable of very high one-sun efficiency as well.

With localized contacts, surface recombination decreases with the penalty of an increase in transport losses in the substrate: deeper gradients for minority carriers, or increased series resistance for majority carriers, because of current crowding near the contacts. The trading is more favorably solved as the contact size shrinks [54]. Light and/or localized diffusions also have the drawback of decreased gettering action.

7.3.3.4 Industrial cells

Screen printing drastically affects the design of the emitter: it must be very highly doped to decrease the high-contact resistance and not very shallow so that it is not perforated during paste firing, which would short-circuit the junction [55]. Besides, the wide metal lines must be placed well apart; and in order to keep shading losses moderate, the emitter lateral conductance must be high, which also advises deep and highly doped regions. These characteristics are good to decrease recombination at the contacts, but are far from optimum at the exposed surface.

Industrial phosphorus emitters, typically, feature surface concentrations over 10^{20} cm^{-3} and 0.4-μm depth, and result in a sheet resistance around 40 Ω. As already

mentioned, the very highly doped region exhibits almost no photovoltaic activity due to the presence of precipitates ("dead layer"). As a result, the collection of short-wavelength light is very poor and the J_0 large, irrespective of a hypothetical surface passivation is therefore not implemented. The advantage is that heavy phosphorus diffusions produce very effective gettering. Some ways of incorporating selective emitters to screen-printed cells are being considered, SiN_x appearing very well suited for surface passivation [55]. This, however, must be accompanied by a decrease in the finger width so that lower sheet resistances are tolerated.

7.3.4 The Back Surface

The majority carrier, back p-contact of industrial solar cells is usually made by printing, and subsequently, firing an aluminum-containing Ag-conducting paste.

The p^+ layer would be useful in decreasing contact recombination, as explained, but this is immaterial to the electrically thick ($w > L$) present industrial cells and it is not optimized for this purpose.

For high-efficiency cells, contact passivation is essential. A BSF is a first step (Figure 7.4a). Localized contacts, as shown in Figure 7.4(b), further reduce recombination. This structure is presented by some of the bifacial cells [56].

If the surface passivation is good, the BSF is restricted to point contacts, some microns in size, as in PERL and similar cells (Figure 7.4c) [57]. The back face of bifacial cells passivated with SiN_x is shown in Figure 7.4(d).

A shallow and light diffusion helps in decreasing surface recombination (Figure 7.4e). The diffusion can be the same type of the substrate, or the opposite one: so-called PERT (Passivated emitter rear totally diffused) [36] and PERF (Passivated emitted rear floating junction) [58] cells demonstrate these concepts. The latter structure benefits from the lower J_0 values of n^+ layers, and it is essential that no electron flow is injected from the n region to the p contact: the junction must be in open-circuit (a "floating" junction). Note that this structure has nothing to do with structures sometimes found at the back of industrial cells (Figure 7.4f) where a coarse metal mesh is fired through the parasitic n^+ layer formed during front diffusion. A mesh is preferred to a continuous layer for mechanical reasons. The junction is shorted and presents to the substrate a high SRV.

7.3.5 Size Effects

Substrate edges are highly recombining surfaces that adversely affect cell performance, especially for small size, large diffusion length devices. For laboratory cells, efficiency is defined on the basis of a design area. The emitter is limited to it by planar masking or mesa etching. The true edge is thus placed far away from the cell limit, and then recombination is reduced. For real applications, on the contrary, only the substrate area counts, and edge optimization is more complex. Advanced passivation schemes such as edge diffusions are being considered [59, 60]. In large industrial cells, this recombination is much less important.

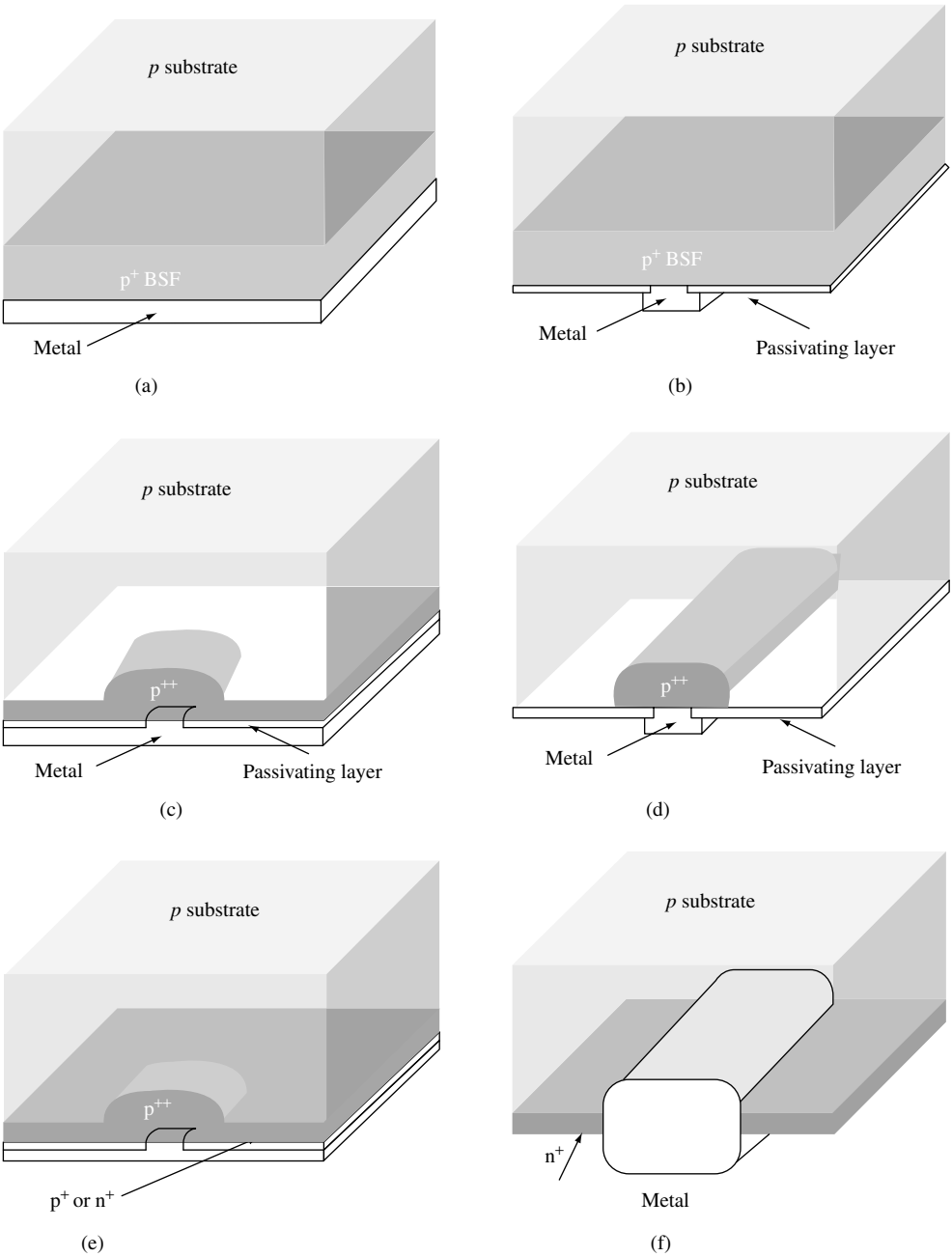

Figure 7.4 Rear contact structures: (a) continuous BSF; (b) bifacial cell; (c) local BSF; (d) local BSF, bifacial cell; (e) selective emitter or floating junction passivation; and (f) shorted junction at the back face of industrial cells

Large cell sizes are preferred by the industry, 10×10 cm^2 or 12.5×12.5 cm^2 being standard. Apart from fabricability concerns, a bigger cell means that more current must be collected at the terminals, making Joule losses grow: the longitudinal resistance of the metal lines increases quadratically with their length. This problem, more severe for coarser metallization techniques, decreases efficiency with increasing size. To alleviate series resistance at the price of increased shading, terminals are soldered to metal bus bars inside the cell's active area, thus decreasing the distance from where current must be collected along the fingers.

7.3.6 Cell Optics

Flat plate solar cells in operation are illuminated from a large portion of the sky, not only because of the isotropic components of radiation, but also because of the sun's apparent motion over the day and the year. So, with regard to angular distribution, these cells must accept light from the whole hemisphere. The spectral distribution also varies with time, weather conditions, and so on. For calibration purposes, a standard spectral distribution AM1.5 Global is adopted as a representative condition, usually specified at 0.1 W·cm^{-2}.

A solar cell should absorb all useful light. For nonencapsulated cells, the first optical loss is the shading by the metal grid at the illuminated face, if any. This loss can amount to more than 10% for industrial cells while for laboratory cells using fine metallization it is much lower. Though several techniques have been proposed to decrease the effective shading, such as shaped fingers, prismatic covers, or cavities [61], their efficacy depends upon the direction of light and so they are not suited to isotropic illumination.

7.3.6.1 Antireflection coatings

Next, loss comes from the reflectance at the Si interface, more than 30% for bare Si in air due to its high refraction index. A layer of nonabsorbing material with a lower refraction index (n_{ARC}) on top of the Si substrate decreases reflectance: this is a step toward the zero-reflection case of a smoothly varying refraction index. If the layer is thick in terms of the coherence length of the illumination, around 1 μm for sunlight, there are no interference effects inside it. The encapsulation (glass plus lamination) belongs to this category.

Antireflection coating (ARC) means an optically thin dielectric layer designed to suppress reflection by interference effects. Reflection is at a minimum when the layer thickness is (an odd multiple of) $n_{ARC}\lambda_0/4$, with λ_0 the free space wavelength, since in this case reflected components interfere destructively. At other wavelengths reflection increases, but is always below the value with no ARC or, at most, equal [62]. The ARC is usually designed to present the minimum at around 600 nm, where the flux of photons is a maximum in the solar spectrum. For reflection to become zero at the minimum, the coating index should be the geometric average of those of air and silicon, that is, 2.4 at 600 nm for nonencapsulated cells.

The industry uses TiO_x deposited by chemical vapor deposition (CVD). PECVD SiN_x is very interesting since it also serves as a passivating layer, as explained earlier.

By using double layer coatings with $\lambda/4$ design, with growing indices from air to silicon, the minimum in reflection is broader in wavelength. Evaporated SZn and MgF_2

are used in laboratory high-efficiency cells. The low index of passivating SiO_x in contact with Si degrades the performance of the ARC. The SiO_x layer is then made as thin as is compatible with efficient passivation [63].

7.3.6.2 Texturing

Alkaline (KOH or NaOH-based) solutions etch anisotropically a-Si crystal exposing {1 1 1} planes on which the etching rate is lowest. On [1 0 0]–oriented wafers, randomly distributed, square-base pyramids are formed, whose size is adjusted to a few microns by controlling etching time and temperature. In a textured face, a ray can be reflected toward a neighboring pyramid (Figure 7.5a) and hence absorption is enhanced. Though calculation of reflection requires ray tracing, a rough estimate of near-normal incidence can be derived, by assuming that each ray strikes twice the Si surface so that reflection is the square of the untextured case.

Texturing is incorporated into both industrial and laboratory Si solar cells, and, in combination with antireflection (AR) coating, reduces reflection losses to a few percent. In the latter case, in order to better control the pyramid geometry and to allow delineation of fine features on the surface, photolithographic techniques are used to define inverted or upright pyramids at the desired positions. It has to be noted that in this case the reflectivity is similar to that of a random texture [64].

Light entering the substrate at a textured surface is tilted with respect to the cell normal. This means that photogeneration takes place closer to the collection junction, which is very beneficial for low-diffusion length cells, by enhancing the collection efficiency of medium- to long wavelengths (Figure 7.5a). The effect is equivalent to an increase of the absorption coefficient. As a drawback, textured surfaces present higher SRVs.

7.3.6.3 Light-trapping

Long-wavelength photons are weakly absorbed in silicon, and, unless internal reflectances are high, they will escape the substrate without contributing to photogeneration. The aim of light-trapping or light confinement techniques is to achieve high internal reflectances.

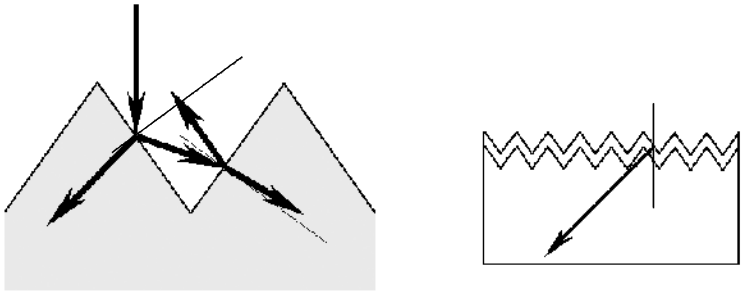

Figure 7.5 Effects of surface texturing: (a) decreased reflection; and (b) increased photogeneration in the base

Practical back mirrors that are fully compatible with the cell electrical design, can be implemented, such as those schematized in Figure 7.4. A metal can make a good reflector, but Al, especially after heat treatment, gives low reflectance. The Si-oxide-metal structure in Figure 7.4(c) can present a high reflectance by capitalizing on interference effects [65].

At the front, the metal mirror is not applicable because the ray paths must be kept open for the entering light. Still, high front reflectance can be achieved because of total internal reflection [61]. Rays striking the surface at angles larger than the critical air-Si one are totally reflected. Texturing one or both surfaces with macroscopic or microscopic features serves this purpose by tilting the rays. Even in the case of geometric texturing with well-defined surface orientations, after a few internal reflections, the direction of rays inside the wafer is randomly distributed: this is the lambertian case, useful analytic approximation to light-trapping. Bifacial structures in Figure 7.4 can, for the same reason, be very efficient at confining the light [66].

Light-trapping increases the effective thickness of the wafer for absorption. In the geometrical optics regime, it has been shown that for one-side isotropic illumination the maximum enhancement factor (though perhaps not realizable) is 4 $(n_{Si}/n_{air})^2$, that is, each ray traverses 50 times the cell thickness before escaping [67]. The corresponding enhancement in photogeneration will be lower because of the competition of the absorption by free carriers at long wavelength.

Light-trapping is essential for thin cells. Even in the thick PERL design it can suppose around 1 $mA \cdot cm^{-2}$ enhancement in short-circuit current with respect to the case where the internal reflectances were zero.

7.3.7 Performance Comparison

For illustration purposes, Table 7.3 collects relevant parameters of the Auger-limited ideal Si solar cell [30], the best one-sun PERL cell [36] and a typical screen-printed, industrial cell on Cz-Si. The different concepts behind each set of data must be accounted for when comparing the figures. For instance, the ideal cell is assumed as being isotropically illuminated, while measurements are made for near-normal incidence.

Table 7.3 Cell performance (25°C, AM1.5 Global 0.1 $W \cdot cm^{-2}$)

Cell type	Ideal (calculated)	PERL (measured)	Industrial (typical)
Size (cm^2)	–	4	100
Thickness (μm)	80	450	300
Substrate resistivity (Ω·cm)	Intrinsic	0.5	1
Short-circuit current density, J_{SC} ($A \cdot cm^{-2}$)	0.0425	0.0422	0.034
Open-circuit voltage, V_{OC} (V)	0.765	0.702	0.600
Fill factor, *FF*	0.890	0.828	0.740
Efficiency, η (%)	28.8	24.7	15.0

The most striking difference between the best and the ideal solar cell is the difference in design: thick and low injection *versus* thin and high injection. The PERL cell is surely the best design for the currently achievable levels of surface recombination, which limit open-circuit voltage and shift the optimum thickness to high values. The low resistivity follows then from transport considerations for the chosen structure. The very high fill factor of the ideal cell is characteristic of high injection, Auger-limited operation.

Reduction of surface recombination in the best laboratory cells relies on surface passivation and the restriction of very heavily doped regions to a minimum. In the end, this is possible because of the possibility of defining and aligning very small features on the surfaces.

The very heavily doped emitter, along with lower substrate lifetimes, is responsible for the reduced short-circuit current and open-circuit voltage in the industrial cell. The fill factor is affected by the large device area in conjunction with the limitations of the metallization technique, which further reduces the current because of shading.

Continuous improvement in material quality and cost-driven thinning of the substrates will increase the need for industrial cells to implement surface passivation schemes. This will require the refinement of the metallization technique; another issue is that substrate lifetimes in an industrial environment depend on the gettering action of very heavy diffusions, which are not compatible with optimum surface performance. The PERL approach – high-temperature processes and delineation of fine features – is the most successful path to high efficiency, but it is not the only one that can inspire the forthcoming developments in industrial cells. It is worth noting, in this respect, that heterojunction with intrinsic thin-layer (HIT) solar cells have entered the exclusive club of more than 20% efficiency with a different approach (see Section 7.7.2).

7.4 MANUFACTURING PROCESS

7.4.1 Process Flow

Figure 7.6 shows the main steps of a simple process for solar cell fabrication based on screen printing. With more or less minor modifications, this process is currently used by many manufacturers. The main virtues of this 30-year-old PV technology are easy automation, reliability, good usage of materials and high yield. The drawback, as explained in preceding sections, is the efficiency penalty derived from the coarse and aggressive metallization technique. Some specific treatments worked out for mc-Si will be explained in Section 7.6.

Each step is briefly described in the following text with illustrative purposes: values of temperature, time and so on will only be indicative.

1. *Starting material*: The industry uses so-called solar grade Cz-Si wafers, round in origin but very often trimmed to a pseudo-square shape, or multicrystalline square wafers. Wafer dimensions are between 10- and 15-cm side and between 200- and 350-μm thickness. Doping is *p*-type (boron) to a resistivity of around 1 Ω·cm.
2. *Saw damage removal*: The sawing operation leaves the surfaces of "as cut" wafers with a high degree of damage. This presents two problems: the surface region is of

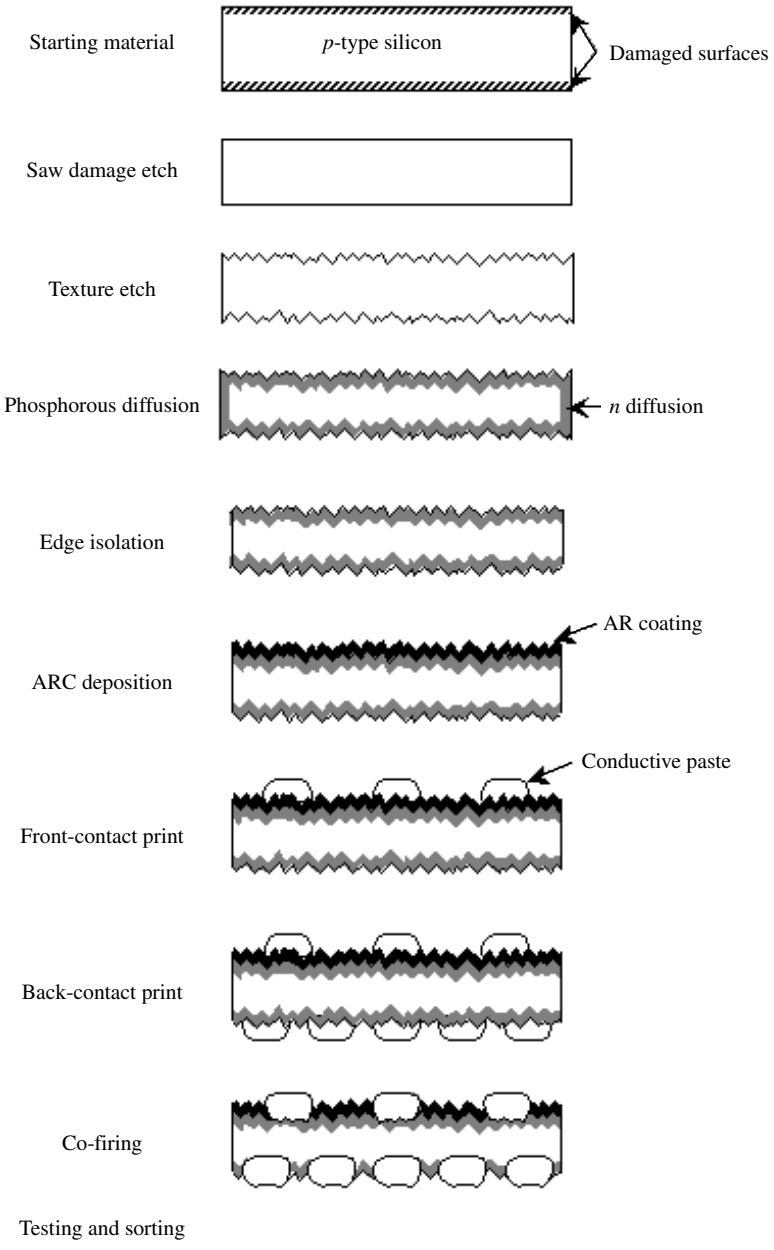

Figure 7.6 A typical processing sequence with schematic illustrations of the resulting structures

a very bad quality and the defects can lead to wafer fracture during processing [68]. For this reason, about ten microns are etched off from each face in alkaline or acid solutions. The wafers, in Teflon cassettes, are immersed in tanks containing the solution under temperature and composition control. Alkaline etches are preferred to acid solutions due to considerations of waste disposal.

3. *Texturization*: NaOH etching leading to microscopic pyramids is commonly employed. Their size must be optimized, since very small pyramids lead to high reflection, while very large ones can hinder the formation of the contacts. To ensure complete texturing coverage and adequate pyramid size, the concentration, the temperature and the agitation of the solution and the duration of the bath must be controlled (in fact NaOH at a higher concentration and at a higher temperature is commonly used as an isotropic etch for saw damage removal). Alcohol is added to improve homogeneity through an enhancement of the wettability of the silicon surface. Typical parameters are 5% NaOH concentration, 80°C and 15 min [69].
   Texturing alternatives for multicrystalline material are presented in Section 7.6.
4. *Phosphorus diffusion*: Phosphorus is universally used as the *n*-type dopant for silicon in solar cells. Since solid-state diffusion demands high temperature, it is very important that the surfaces are contamination-free before processing. To this end, after the texturing the wafers are subjected to acid etch to neutralize alkaline remains and eliminate adsorbed metallic impurities.

   The industry uses a number of procedures to perform the phosphorus diffusion. The following classification is based on the type of furnace in which the high-temperature step takes place:

   Quartz furnaces: The cells to be diffused, loaded in quartz boats, are placed in a quartz tube with resistance heating and held at the processing temperature (Figure 7.7a). The cells enter and exit the furnace through one end, while gases are fed through the opposite one. Phosphorus itself can be supplied in this way, typically by bubbling nitrogen through liquid $POCl_3$ before injection into the furnace. Solid dopant sources are also compatible with furnace processing. Five to fifteen minutes at temperatures in the range from 900 to 950°C can be considered representative. As suggested in Figure 7.6, both surfaces and the edges of the wafer will be diffused.

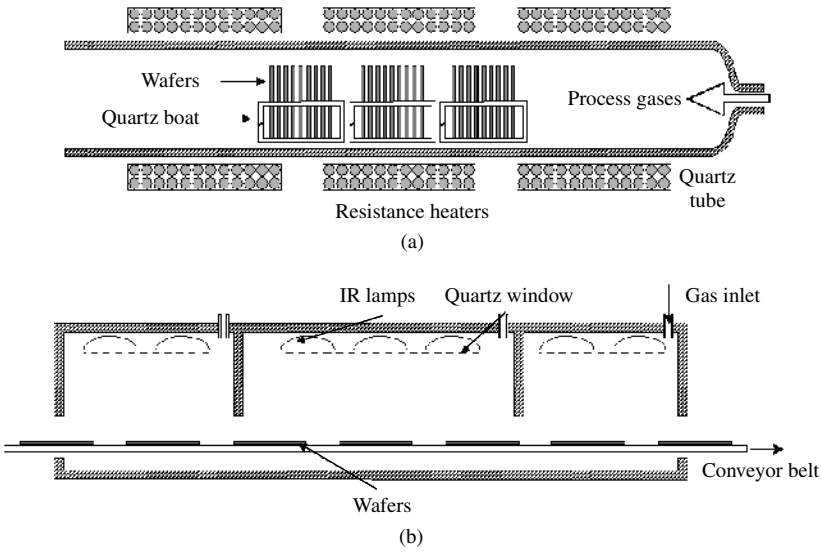

Figure 7.7 (a) A quartz furnace; and (b) a belt furnace for the diffusion of phosphorus

Belt furnaces: In this case, solid phosphorus sources are used: screen printed, spun-on or CVD pastes containing phosphorus compounds are applied on one wafer face and, after drying, placed in a conveyor belt passing through the furnace (Figure 7.7b). The temperature inside it can be adjusted in several zones and, though the furnace is open, gases can be supplied. The temperature cycle undergone by the wafer will mimic the temperature profile along the furnace with the time scale set by the advancing speed of the belt. A cycle begins with several minutes at around 600°C with clean air to burn off the organic materials of the paste, followed by the diffusion step in nitrogen at 950°C for 15 min. Only one face of the wafer is diffused, but the parasitic junction formed at the edges is also present in this technique due to diffusion from the gas phase. Resistance or infrared heating can be employed, the latter offering the possibility of faster heating–cooling rates of the wafer.

The main benefit of the quartz furnace is cleanliness, since no metallic elements are hot and no air flows into the tube. Though this is a batch step, high throughput can be achieved since many wafers can be simultaneously diffused in each tube, commercial furnaces consisting of stacks of four tubes. In a belt furnace, the ambient air can get into the furnace and the hot conveyor belt is a source of metallic impurities. The assets of belt furnaces are found in automation and in-line production, throughput and the ability to implement temperature profiles. New designs try to reconcile the advantages of both types of equipment [70].

After diffusion, an amorphous glass of phospho-silicates remains at the surface that is usually etched off in diluted HF because it can hinder subsequent processing steps.

5. *Junction isolation*: The *n*-type region at the wafer edges would interconnect the front and back contacts: the junction would be shunted by this path translating into a very low shunt resistance. To remove this region, dry etching, low temperature procedures are used.

   For the widely employed etch with plasma, the cells are coin-stacked and placed into barrel-type reactors. In this way, the surfaces are protected and only the edges remain exposed to the plasma. This is obtained by exciting with an RF field a fluorine compound (CF_4, SF_6), which produces highly reactive species, ions and electrons that quickly etch the exposed silicon surface [71]. Though this is a batch step, a large number of wafers can simultaneously be processed allowing high throughput. Laser cutting of the wafer edges is an alternative in industrial use.

6. *ARC deposition*: Titanium dioxide (TiO_2) is often used for creating the antireflecting coating due to its near-optimum refraction index for encapsulated cells. A popular technique is atmospheric pressure chemical vapor deposition (APCVD) from titanium organic compounds and water: the mixture is sprayed from a nozzle on the wafer held at around 200°C and the compound is hydrolyzed on the surface [72]. This process is easily automated in a conveyor-belt reactor. Other possibilities include to spin-on or screen print appropriate pastes.

   Silicon nitride is also used as AR coating material with unique properties that will be described in Section 7.6.

7. *Front contact print and dry*: The requirements for the front metallization are low contact resistance to silicon, low bulk resistivity, low line width with high aspect ratio, good mechanical adhesion, solderability and compatibility with the encapsulating

materials. Resistivity, price and availability considerations make silver the ideal choice as the contact metal. Copper offers similar advantages, but it does not qualify for screen printing because subsequent heat treatments are needed during which its high diffusivity will produce contamination of the silicon wafer.

Screen printing compares very unfavorably with vacuum evaporation in the first three requirements. It has been already commented how this affects the cell design and leads to a significant efficiency gap between laboratory and commercial cells. But throughput and cost compensate for it.

Screen printing will be described in more depth in the following section. It is used to stick a paste containing silver powder to the front face of the wafer in the comblike (fingers plus bus bars) pattern. Automatic screen printers are available that are capable of in-line, continuous operation with high throughput. These machines accept wafers from packs, cassettes or a belt line, place them with sufficient accuracy under the screen and deliver the printed wafers to the belt line. The paste is a viscous liquid due to the solvents it contains; these are evaporated in an in-line furnace at 100 to 200°C. The dried paste is apt for subsequent processing.

8. *Back contact print and dry*: The same operations are performed on the backside of the cell, except that the paste contains both silver and aluminum and the printed pattern is different.

   Aluminum is required because silver does not form ohmic contacts to p-Si, but cannot be used alone because it cannot be soldered. The low eutectic temperature of the Al-Si system means that some silicon will be dissolved and then recrystallize upon cooling in a p-type layer.

   Though in principle a continuous contact will give better electrical performance (lower resistance), most commercial wafers feature a back contact with a mesh structure: apart from paste-saving considerations, this is preferred to a continuous layer because the different expansion coefficients would produce warp of the cell during the subsequent thermal step.

9. *Cofiring of metal contacts*: A high-temperature step is still needed: organic components of the paste must be burnt off, the metallic grains must sinter together to form a good conductor, and they must form an intimate electric contact to the underlying silicon. As Figure 7.6 shows, the front paste is deposited on an insulating layer (the AR coating) and the back contact on the parasitic n-type rear layer.

   Upon firing, the active component of the front paste must penetrate the ARC coating to contact the n-emitter without shorting it: too mild a heat treatment will render high contact resistance, but too high a firing temperature will motivate the silver to reach through the emitter and contact the base. In extreme situations, this renders the cell useless by short-circuiting it. In more benign cases, small shunts appear as a low shunt resistance or dark current components with a high ideality factor that reduces the fill factor and the open-circuit voltage.
   The back paste, in its turn, must completely perforate the parasitic back emitter to reach the base during the firing.
   In order to comply with these stringent requirements, the composition of the pastes and the thermal profile of this critical step must be adjusted very carefully.

10. *Testing and sorting*: The illuminated $I-V$ curve of finished cells is measured under an artificial light source with a spectral content similar to sunlight (a sun simulator)

at a controlled temperature of 25°C. Defective devices are then rejected, and the rest are classified according to their output. The manufacturer establishes a number of classes attending, typically, to the cell current at a fixed voltage near the maximum power point. Modules will subsequently be built with cells of the same class, thus guaranteeing minimal mismatch losses. If, for instance, cell currents within a class must be equal within 5%, the accuracy and stability of the system must be better than that. Automatic testing systems that meet the very demanding requirements of high throughput processing are available.

7.4.2 Screen-printing Technology

Screen printing is a thick-film technology, a terminology that opposes it to the usual microelectronic procedures of evaporation of thin films. It consists in translating a layer of a material in a desired pattern to the surface of the wafer. Though it can be employed for virtually any step in solar cell manufacturing, contact formation constitutes the most demanding, frequent and conspicuous application of screen printing. Screens and pastes are the essential elements of this technology [68].

1. *Screens*: Screens are tight fabrics of synthetic or stainless steel wires stretched on an aluminum frame, as sketched in Figure 7.8. The screen is covered with a photosensitive emulsion, which is treated with photographic techniques in such a way that it is removed from the regions where printing is desired.

   For printing fine and thick layers, as is needed for the front contact of a solar cell, the wires must be very thin and closely spaced [73]. On the other hand, the opening of the reticule must be several times larger than the largest particle contained in the paste to be printed. Screens for solar cell production typically feature 200 wires per inch, wire diameter around 10 μm, mesh opening around 30 μm, corresponding to

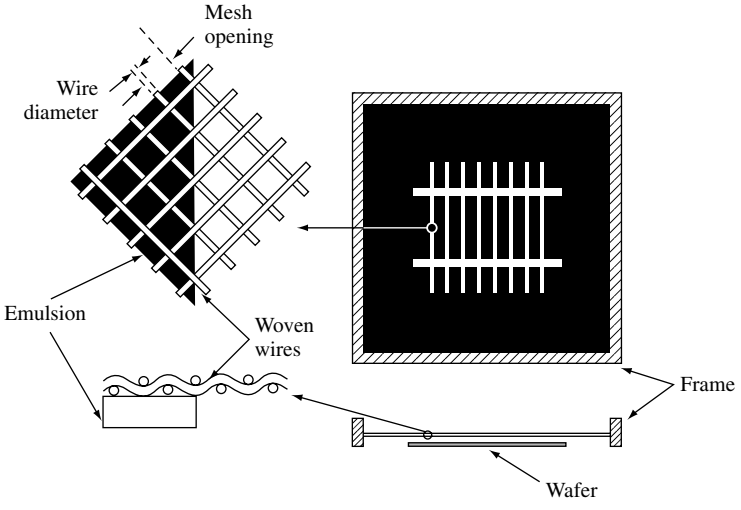

Figure 7.8 A screen for transferring the top contact pattern to a solar cell

nearly 50% open surface, that is, not intercepted by wires and a total thickness (woven wires plus emulsion) of around 100 μm.

2. *Pastes*: The pastes are the vehicles that carry the active material to the wafer surface. Their composition is formulated to optimize the behavior during printing. A paste for the metallic contacts of the solar cell is composed of the following:

   Organic solvents that provide the paste with the fluidity required for printing
   Organic binders that hold together the active powder before its thermal activation
   Conducting material, which is a powder of silver composed of crystallites of a size of tenths of microns; for the *p*-contact, aluminum is also present. This amounts to 60 to 80% in weight of the paste
   Glass frit, 5 to 10% in weight, a powder of different oxides (lead, bismuth, silicon etc.) with a low melting point and high reactivity at the process temperature, that enables movement of the silver grains and etches the silicon surface to allow intimate contact.

   The paste composition is extremely important for the success of the metallization and is critically linked to the heat treatment.

3. *Printing*: Figure 7.9 illustrates the process of printing a paste through the patterned emulsion on a screen. The screen and the wafer are not in contact, but a distance apart called the *snap-off*. After dispensing the paste, pressure is applied to the squeegee, which can be made of metal or rubber: this puts the screen in contact with the wafer. The squeegee is then moved from one side of the screen to the opposite one, dragging and pressing the paste in front of it. When an opening is reached, the paste fills it and sticks to the wafer, remaining there after the squeegee has passed and the screen has elastically retired.

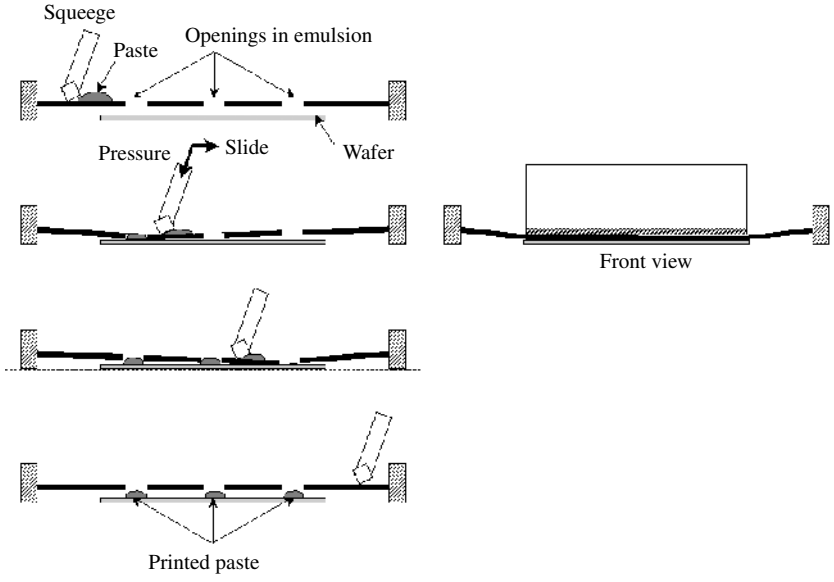

Figure 7.9 Illustration of a printing sequence

The amount of printed paste depends on the thickness of the screen material and the emulsion and the open area of the fabric. It also depends on the printed line width.

The viscous properties are of utmost relevance: when printing, the paste must be fluid enough to fill without voids all the volume allowed by the fabric and the emulsion, but after being printed it must not spread over the surface.

Critical parameters of this process are the pressure applied on the screen, the snap-off distance and the velocity of the squeegee.

4. *Drying*: Solvents are evaporated at 100 to 200°C right after printing so that the wafer can be manipulated without the printed pattern being damaged.

5. *Firing*: Firing of the pastes is usually done as a three-step process in an IR belt furnace. In the first step, when heating up, the organic compounds that bind the powder together are burnt in air. In the next step, the highest temperature between 600 and 800°C is reached and maintained for a few minutes. Higher temperatures are needed if an AR coating must be penetrated; crystal orientation and paste composition must be considered too. In the last step, the wafer is cooled down.

   The phenomena that take place during firing are very complex and not completely understood. The oxides forming the glass frit melt, enabling silver grains to sinter and form a continuous conductor so that the layer can present low sheet resistance. Neither the silver melting point nor the silicon–silver eutectic temperature is reached, sintering consisting of the intimate contact of solid silver crystallites. At the same time, the reactive molten glass etches some silicon and silver grains are allowed to form intimate contact with the substrate. The amount of etched silicon is on the order of 100 nm. When a layer of TiO_2 or SiN is present, the glass frit is able to etch through it. In fact, the quality of the contact improves because of a better homogeneity.

   The picture of the contact after cooling down shows two zones [74]. In the inner one, crystallites of silver are plugged into silicon forming crystalline interfaces and presumably very good electrical contact in a sort of "point contact". These grains are embedded in a compact amorphous glass. The outer zone is more porous and contains silver grains and glass frit: this porosity explains why the resistivity of silver paste is much higher than that of pure silver.

   Besides, the contact resistance of printed contacts is much higher than that of an evaporated contact to *n*-Si of the same doping. It seems that, although enough silver grains make good contact with silicon, not all them are connected to the grains in the outer layer; many remain isolated by the glass.

   When the paste, in the case of the back metallization, contains aluminum as well as silver, the Al-Si eutectic formed and recrystallized ensures a good contact. With dielectric layers the contact appears to be localized as well, and some beneficial role is attributed to the metal atoms in the frit [75].

6. *Limitations and trends in screen printing of contacts*: As explained in former sections, the high contact resistance and the etching action of the glass frit require the front emitters to be highly doped and not very thin if screen printing is used. Only improved paste formulation and processing can overcome this limitation.

   Narrow but thick fingers with good sheet conductance are also needed. Well-defined lines must be much wider than the pitch of the woven fabric; 60-μm lines seem achievable, with 100-μm ones being standard (see Figure 7.10). Incrementing the amount of transferred paste implies increasing the thickness of the emulsion or the

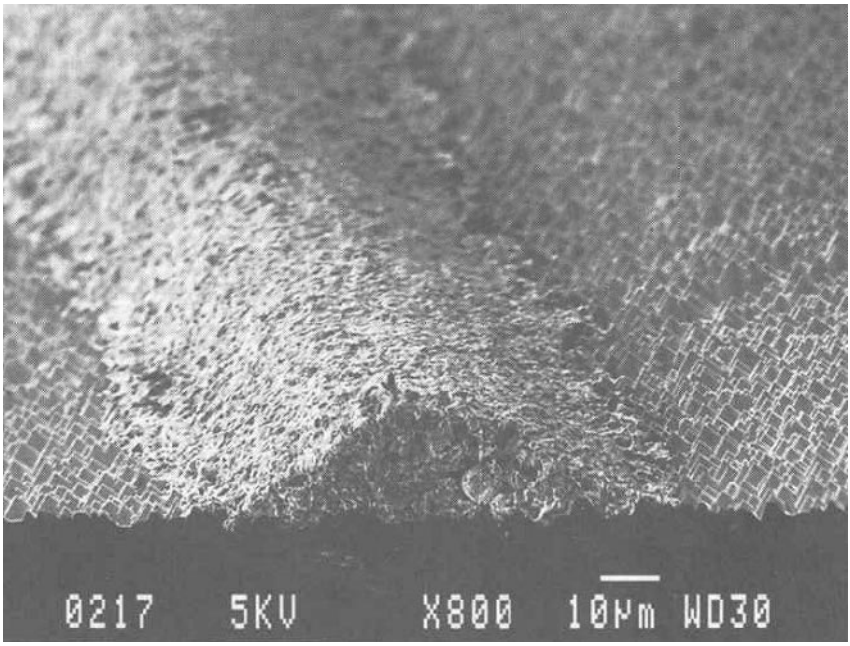

Figure 7.10 Screen-printed contact finger; texture pyramids are also visible. (Reprinted from *Solar Energy Materials and Solar Cells*, **41/42**, Nijs J, Demesmaeker E, Szulfcik J, Poortmans J, Frisson L, De Clerq K, Ghannam M, Mertens R, Van Overstraeten R, "Recent improvements in the screen-printing technology and comparison with the buried contact technology by 2D-simulation", 101–107, (1997), with permission from Elsevier Science)

pitch-to-diameter ratio of the wires, which are both limited. Besides, screens become deformed with usage and a continuous deterioration of printed patterns is observed.

Metal stencils [76] can outperform screens: they produce finer lines with better aspect ratio, endure more printing operations without degradation and need less cleaning and maintenance.

In screen printing, the wafer is subjected to considerable pressure. This can pose a problem with very thin or irregular wafers, such as those obtained by sheet growth of silicon, which can break down. Metallization alternatives have been developed, some of which are used in industries. They will be presented in Section 7.7.

7.4.3 Throughput and Yield

Because of the rapidly growing demand, photovoltaic factories are quickly expanding their production volumes so that there is a strong driving force to increase the throughput of processes and equipment. Automation is being extensively applied to the fabrication of solar cells and in-line, continuous processing tends to displace batch steps: in the process outlined above, only chemical etches, tube diffusion and edge isolation are batch steps. Automation and large-scale production lead to reduced costs [77].

Most processes described above have been borrowed from the electronic industry: diffusion, plasma etching, and so on are standard in microelectronics, while screen printing

was extensively used by thick-film technology in hybrid circuits. The character of the industries being different, their requirements for equipment differ, and it is to be expected that substantial improvements of photovoltaics will take place, now that the business volume makes it attractive for equipment manufacturers to get involved in.

A modern fabrication line is capable of processing around 1000 wafers h^{-1}, that is, an operation in a cell takes 2 to 3 s. Of course, the slowest operation along the flow line will limit the overall throughput. In order to get an estimate of how this translates into yearly production, let us consider 10×10 cm^2 cells with 15% efficiency (1.5 Wp power per cell). If the line operates without interruption and all wafers are successfully processed, during one year it will produce

$$1.5 \text{ Wp/cell} \times 1000 \text{ cells/h} \times 24 \text{ h/day} \times 365 \text{ days/year} \cong 13 \text{ MWp/year}$$

This number has to be decreased by (1) the downtime of the equipment due to maintenance, repair, and so on and (2) the yield, that is, the percentage of defective or broken wafers. Allowing for both would give a throughput in the range of 5 to 10 MWp/year per production line with available, commercial equipment.

Yield is a most important parameter for cell production: it can be defined as the ratio of successful finished cells to starting wafers. Since PV technology is material-intensive, yield has a strong influence on cost. Breakage and poor electrical performance are the causes of low yield, which is, generally speaking, benefited by automation. In this respect, in-line quality control acquires a great relevance to quickly detect and amend problems affecting yield.

For a given time per operation per cell, the throughput increases if the power of the cell increases. This is achieved by increasing the cell's area and the efficiency, which also helps in decreasing the cost. The standard wafer size is shifting from 10×10 cm^2 to 12.5×12.5 cm^2 and 15×15 cm^2. Series resistance and the uniformity of the obtained layers (emitter, AR coating), that may compromise the electrical performance, become important issues. Besides, larger cells are more difficult to handle without breaking and the yield may be affected.

There is a lot of room for efficiency improvement of industrial solar cells and the processes to realize it are proved in the laboratory. The question is how to implement them in an industrial environment so that they are cost-effective.

7.5 VARIATIONS TO THE BASIC PROCESS

This section introduces some variations to the basic process described above that aims at improving the efficiency, the throughput or the cost. While some modifications are already in production, most of these improvements are still being developed at the laboratory.

7.5.1 Thin Wafers

Wafering and sheet-growth techniques improve and produce thinner substrates, with wafer thickness below 200 μm being envisaged for the near term [78]. When processing these thin cells, several relevant issues appear.

The probability of fracture of the wafer during handling increases, especially in conjunction with a larger size. Adequate handling tools must be designed. Some steps appear to be critical: for instance, in chemical baths convection can exert significant torque on the wafers. This issue is fostering the study of the mechanical properties of silicon [79, 80] and even the development of new crystallization procedures.

The behavior during heat treatments is modified due to a decreased thermal mass. On the other hand, wafers can more easily become bent. Processes need to be specifically optimized for thin cells [81].

Thin cells largely depend on surface passivation and optical confinement. If attained to reasonable degrees, efficiency improvement comes as a bonus for thin cells, but otherwise the performance is degraded. New optimal structures must be developed.

7.5.2 Back Surface Passivation

The enhancement of material quality and the decrease of wafer thickness will make it necessary to passivate the back surface. Several approaches are feasible to be incorporated to the basic screen-printing process [55, 82]:

- *Aluminum back surface field*: With the benefit of gettering action, a highly doped *p*-type region at the back can easily be formed by screen-printing aluminum paste on the entire surface followed by high-temperature alloying. Several manufacturers implement aluminum BSF in their production lines. It can be integrated in the process flow (1) before metallization, possibly at the same time as phosphorus diffusion, and (2) by printing the aluminum paste after the front contact print so that the alloy forms during paste firing, though in this case lower temperatures are possible leading to worse properties.

  In either case, a back, silver-based contact is still needed for solderability. Bending of the wafers is an issue for thin cells.
- *Boron back surface field*: Like phosphorus, boron can be diffused from solid sources, so that it can easily be integrated into the basic process. Though it would be very attractive to diffuse both phosphorus and boron during the same thermal step, it appears that the obtained profiles are far from optimum and that a two-step diffusion seems necessary.
- *Silicon nitride passivation*: The surface and bulk passivation properties of silicon nitride are explained below. This replaces AR coating deposition and does not alter the basic process, though the parasitic junction must not be allowed to form in this case. This structure, as well as boron BSF, is compatible with the bifacial operation of the solar cell.

7.5.3 Improvements to the Front Emitter

Quantitative improvements in both recombination currents and spectral response will be derived from front surface passivation only when better paste formulations and finer line prints allow more resistive emitters – thinner and/or less doped – to be used [83]. In that case, tube oxidation and silicon nitride deposition appear as good candidates for industrial use.

Selective emitters are being developed at the laboratory level for screen-printed solar cells. A number of techniques have been proposed [84] that are compatible with the screen-printing process; none of them is at present implemented in production lines:

- Two separate diffusions for metallized and unmetallized regions, the heavy diffusion being restricted to the regions to be metallized by a screen-printed mask.
- A homogeneous and thick emitter is diffused by conventional means; a screen-printed mask is applied to protect the regions to be metallized from the plasma etch that follows. In this way, in the unprotected regions the emitter is thinner and less doped.
- Self-aligned selective emitter by diffusion from a patterned solid dopant source: under the dopant source a highly doped emitter is formed, while a much lighter diffusion from the gas phase takes place at the uncovered regions.
- First a high sheet resistance emitter is formed to which self-doping pastes containing phosphorus as well as silver are applied. Firing is performed above the silver–silicon eutectic temperature, thus leading to the formation of an alloyed layer heavily doped with phosphorus [85].

Except the last one, all the techniques require some kind of pattern aligning to print the front contact fingers on the heavily doped regions. Automatic screen printers feature enough accuracy to perform this task.

Obviously, the unmetallized part of these emitters is sensitive to surface passivation, which must thus be implemented by oxidation or nitride deposition.

7.5.4 Rapid Thermal Processes

In conventional furnaces of the closed-tube or conveyor-belt types, not only are the wafers heated to the process temperature but also the equipment itself: chambers, substrates or boats and so on. This brings about (1) long heating–cooling times, due to the large thermal masses involved, (2) a high potential for contamination, since a lot of parts, some of them metallic, are held at a high temperature and (3) high-energy consumption.

On the other hand, the microelectronic industry has developed in the last years, so-called *rapid thermal processes* (RTP), whereby only the wafers, and not their environment, are heated up to high temperature. Selective heating is accomplished by intense UV illumination of the semiconductor. The interest of RTP for solar cell fabrication comes from very short thermal cycles down to a few minutes including heating and cooling, so that throughput can be boosted. Besides, the absence of hot parts in the equipment diminishes potential contamination and energy consumption.

At the laboratory scale rapid thermal diffusion of very thin emitters (which is beneficial from the electrical point of view) has been demonstrated. Rapid thermal firing of screen-printed contacts and aluminum alloying have also been successfully implemented, along with other promising techniques such as rapid thermal nitridation and oxidation of the surfaces for passivation purposes [86, 87]. It can be said that every thermal step in the solar cell process can be made by RTP.

A possible drawback of the technique is a degradation of substrate lifetime as compared to conventional processing of some materials, due to the formation and quenching-in

of defects because of the very fast heating and cooling cycles and possibly also due to precluded gettering action [88].

A hurdle to industrial deployment of RTP is the lack of suitable equipment, since Microelectronics uses one-wafer reactors while Photovoltaics would need large capacity batch reactors or, better, in-line continuous equipment. It seems possible to furnish conveyor-belt furnaces with UV lamps to obtain these industrial RTP reactors, but some problems such as temperature uniformity must be solved [89].

7.6 MULTICRYSTALLINE CELLS

It has already been pointed out that the peculiarities of mc cells may prevent, in some cases, the use of standard processing technologies. Some of the proposed alternatives are not yet so cost-effective as to be incorporated in an industrial production line, but others are finding their way. Two main differences with single-crystalline silicon can be highlighted:

- Mc-material quality is poorer because of crystalline defects (such as grain boundaries, dislocations, etc) and metallic impurities (dissolved or precipitated), giving lower bulk lifetimes and hence lower cell efficiencies. To address this problem, two main strategies are followed: implementation of gettering steps and defect passivation with hydrogen.
- Texturing is more difficult because of different exposed crystallographic planes, so that standard alkaline solutions are not appropriate. To improve light-trapping and absorption, other techniques have to be implemented.

7.6.1 Gettering in mc Solar Cells

As already explained, gettering processes are also used in monocrystalline Si processing, but in the case of mc-Si they are even more important to improve material quality. P and Al gettering steps are routinely integrated in mc solar cell processing. Gettering conditions (temperature, process duration etc) differ from those of single crystal, because of the interaction among metal impurities, crystalline defects and other impurities present in mc-materials (mainly O and C).

It has been realized that gettering efficiency is strongly material dependent [90, 91]. This is explained by the fact that different techniques to grow mc-Si ingots produce wafers with different number and distribution of defects. Differences are even found in regions of the same ingot [92].

Additionally, a single mc wafer may exhibit nonuniform properties, both areal and in-depth, so that response to a gettering process can be inhomogeneous, affecting the final electrical performance of the solar cell [93, 94].

7.6.2 Passivation with Hydrogen

Silicon nitride is widely used as masking film in microelectronics [95]. For solar cells, it presents the advantage of performing as an effective antireflection coating. Films can

be deposited by several techniques, but the most commonly used process is chemical vapor deposition (CVD), involving the reaction of silane gas and ammonia. Plasma-Enhanced Chemical Vapor Deposition (PECVD) is preferred to other CVD technologies (atmospheric pressure CVD or low pressure CVD) because it is a low temperature process ($T < 500^{\circ}C$), and this means reducing complexity and preventing lifetime degradation.

But the most outstanding property of PECVD for mc-material is that it produces hydrogenation, and its benefits for silicon are well known [96, 97]. Atomic H interacts with impurities and defects in the bulk of Si, neutralizing their recombination properties to a certain extent, a phenomenon that is usually expressed as "bulk passivation". In the case of PECVD, amorphous silicon nitride films are produced with up to 40 atomic % of hydrogen (i.e. although these films are usually referred to as SiN_x they are really a-SiN_x:H). A subsequent thermal step is needed to activate hydrogenation, and in an industrial process the metal firing step fulfills this objective [98].

Additionally, surface passivation due to SiN_x deposition by PECVD has also been reported [99]. Achievable surface recombination velocity on a phosphorus-doped emitter is similar to that of a high-quality oxide passivated one, and a value as low as 4 $cm\,s^{-1}$ has been obtained on a polished 1.5 Ω·cm FZ *p*-type silicon wafer [100].

These three different properties (AR coating, bulk passivation and surface passivation) cannot be varied independently, an optimization of processing parameters (temperature, plasma excitation power and frequency, gas flow rate) is necessary, and a compromise should be reached [101, 102]. Furthermore, there are different PECVD techniques giving different results.

The state of the art of the industrial PECVD equipments today is the "direct" PECVD, schematized in Figure 7.11(a). The processing gasses are excited by means of an electromagnetic field, and the wafers are located within the plasma. Bulk is effectively passivated, but surface damage is sustained due to direct exposure of wafers to plasma, precluding the achievement of good surface passivation. Furthermore, surface passivation degrades with exposition to UV light.

There is a high frequency direct PECVD (13.56 MHz) and a low frequency one (in the range of 10–500 kHz), the former being better in terms of surface passivation and UV stability. On the other hand, it is more difficult to obtain uniform layers.

A different approach is the "remote" PECVD, where wafers are located outside the region in which the plasma is formed. Surface damage is avoided in this way, so that

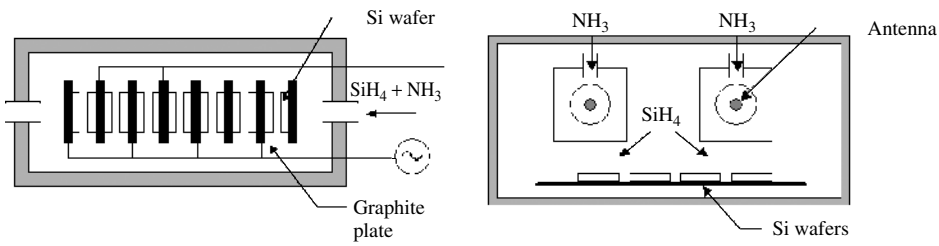

Figure 7.11 Industrial PECVD reactors: (a) direct-plasma reactor; and (b) remote-plasma system

better surface passivation is achieved. On the other hand, bulk passivation is reduced. This technique has been developed at the laboratory level in the last decade, and is currently being introduced into the industry. Figure 7.11(b) shows a sketch of an industrial remote PECVD. It implements a continuous feed of wafers, an advantage that should be compared to the batch-type direct PECVD.

7.6.3 Optical Confinement

Anisotropic texture with alkaline solutions (NaOH or KOH), standard in single crystal solar cells, is also applied to multicrystalline wafers, but with much poorer results, which is one of the reasons for their reduced performance. Reflectance of the textured wafers is relatively high because for randomly oriented grains the etch rate is not the same as that of (100) crystals. Another drawback is the existence of steps between grains, which may cause interruption in the screen-printed metal contacts.

That is why new alternatives are being considered. Their evaluation should take into account not only gains in reflectivity, but also surface damage and compatibility with metallization. In any case, the potential of some of these have been proved, and they are now being developed for industrial applications. Others need more research. The surface features produced by some of these are comparable in size or smaller than the wavelength, and geometrical optics is no longer applicable. They act as diffraction gratings, as scattering media or, in the limit of very small feature size, as graded index layers.

7.6.3.1 Chemical texturing

Several chemical techniques have been proposed. Some of them result in an inverted pyramid structure, but need photolithography patterning, which is a serious drawback for compatibility with the industry [103]. The result of nearly 20% for a mc-Si solar cell relies on an oxide-forced acidic texturing scheme [104]. A simpler approach is based on isotropic etching with an acidic solution containing nitric acid, hydrofluoric acid and some additives. The resulting etch pits of 1–10 μm in diameter are uniformly distributed, giving a homogeneous reflectance over the surface of the wafer and the absence of steps between grains (see Figure 7.12). An increase of short-circuit current of about 1 $mA \cdot cm^{-2}$ is reported for solar cells processed on isotropic textured wafers when compared to cells processed on anisotropic textured wafers [105]. Some technical difficulties, such as depletion of the solution and exothermic effects, can be encountered to come to an industrially compatible processing step. An automatic wet-bench, with temperature control of the etching solution and automatic replenishment of chemicals, has been designed recently.

Reduction in reflection, by forming porous silicon, is also being developed [106]. A detailed analysis taking into account the sum of reflectance and absorption within the porous Si layer shows an optimum of about 5 to 6% total optical loss. Besides its potential, the compatibility of the porous Si formation with screen-printed contacts still needs to be addressed.

7.6.3.2 Mechanical texturing

V-grooves about 50-μm deep can be formed in Si wafers by mechanical abrasion using conventional dicing saws and beveled blades, followed by an alkaline etching to reduce

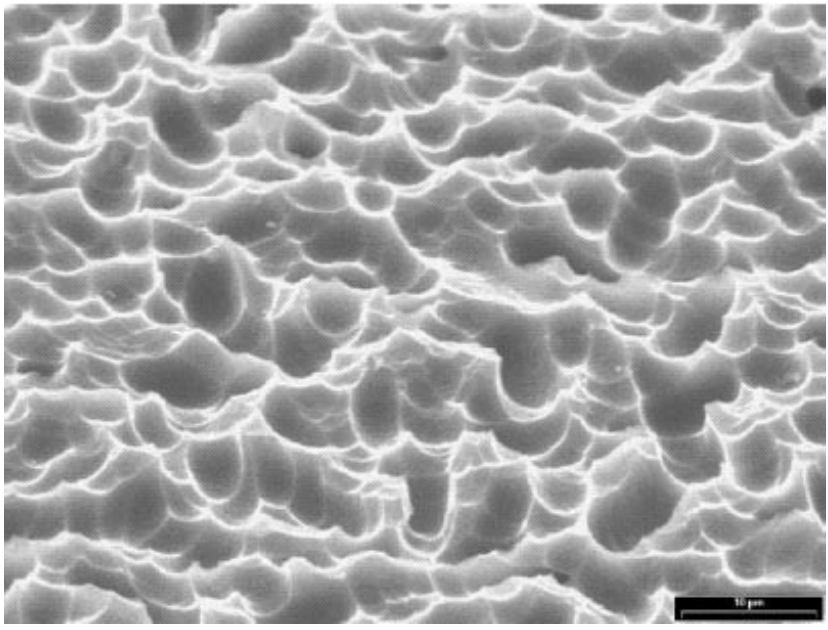

Figure 7.12 Mc-Si surface after acid etching. (Reprinted from *Solar Energy Materials and Solar Cells*, **74**, Szulfcik J, Duerinckx F, Horzel J, Van Kerschaver E, Dekkers H, De Wolf S, Choulat P, Allebe C and Nijs J, "High-efficiency low-cost integral screen-printing multicrystalline silicon solar cells", 155–164, (2002), with permission from Elsevier Science)

surface damage. With this technique, efficiency gains of 5% (relative) after encapsulation have been reached [107]. Contact fingers should be screen printed parallel to the grooves, on plateaus left untextured to ensure easy printing, so that some kind of alignment is maintained. Other contacting alternatives can be implemented, such as roller printing [108] or buried contact [109]. Currently, automated systems are being developed to check industrial feasibility.

Another approach is scribing grooves by laser [110]. Upright pyramids of 7-μm height can be created by two orthogonal sets of parallel grooves, followed by a chemical etch to remove the silicon residues. Combined with a single layer ARC, laser texturing can reduce weighted reflectivity to 4%, half of that given by anisotropic etching and the same AR coating. Adjustments have been made to obtain smoother and smaller grooves, in order to adapt the technique to a screen-printed process.

7.6.3.3 Reactive ion etching (RIE)

Reactive ion etching (RIE) texturization of silicon in chlorine plasma is a dry isotropic etching process that creates a surface with a high density of steep etching pits, with typical dimensions below 1 μm (see Figure 7.13) [111]. Increases of up to 1.4 $mA \cdot cm^{-2}$ in short-circuit current compared to anisotropic texture have been reported with a maskless technique [112]. RIE can also be performed in conjunction with a masking layer to produce more regular features [113]. The main obstacle in industrial implementation is too

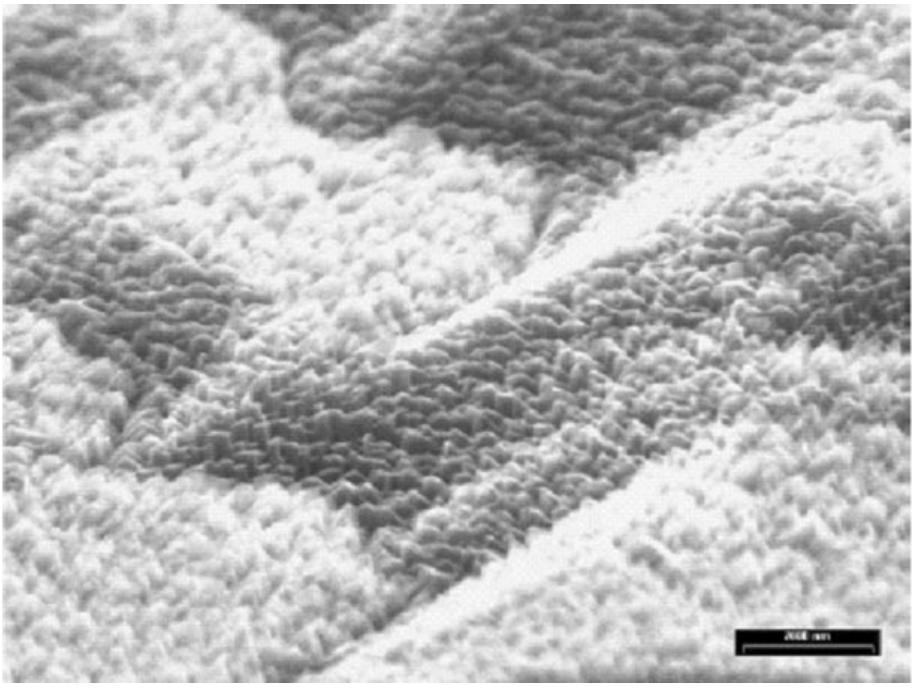

Figure 7.13 Mc-Si surface after RIE. (Reprinted from *Solar Energy Materials and Solar Cells*, **74**, Szulfcik J, Duerinckx F, Horzel J, Van Kerschaver E, Dekkers H, De Wolf S, Choulat P, Allebe C and Nijs J, "High-efficiency low-cost integral screen-printing multicrystalline silicon solar cells", 155–164, (2002), with permission from Elsevier Science)

low process throughput. Alternatives to the use of toxic and corrosive Cl_2 are also being investigated [114].

7.6.3.4 AR coating and encapsulation

It has to be taken into account that cell reflection properties differ from those of texturing because it is usually complemented by AR coating (typically, by atmospheric pressure CVD deposition of TiO_2 or TiO_2/SnO_2 or by PECVD of SiN_x), and cell encapsulation, so that the relative difference between several texturing methods normally reduces, as can be noticed in Table 7.4.

Table 7.4 Comparison of weighted AM1.5 reflectivities for mc-Si wafers with several surface treatments [115]

Reflectivity [%]	Alkaline textured	Acidic textured	Maskless RIE
Bare	34.4	27.6	11.0
With SiN AR coating	9.0	8.0	3.9
SiN & encapsulated	12.9	9.2	7.6

7.7 OTHER INDUSTRIAL APPROACHES

Other commercially available technologies will be described in this section. They all look for a decrease in the \$ W^{-1} figure of merit, following different approaches:

- using ribbons, presented in Chapter 6, as substrates;
- implementing techniques that do not need high-temperature processes: HIT, based on a-Si/*x*-Si heterojunction emitter;
- substituting screen-printing metallization by a more efficient technique: LGBG, based on the buried contact concept;

These only cover a small fraction of the PV market today, but they all have big expansion plans for the next few years.

7.7.1 Silicon Ribbons

Ribbon technologies offer a cost advantage over crystalline silicon, thanks to the elimination of the slicing process. They cover at the moment around 5% of the PV market, Edge-defined-Film-fed Growth (EFG) being the most mature of them, while string ribbon (STR) and dendritic web (WEB) are also into industrial production.

A specific solar cell process is needed for ribbon substrates, to account for the high density of defects (dislocations, grain boundaries, impurities, etc). Al paste is usually printed to create a deep BSF and to benefit from gettering, and silicon nitride is deposited by PECVD for bulk defect passivation and anti-reflection coating.

For EFG solar cells, the uneven surface of the sheets precludes the use of screen-printing metallization, and back and front contact formation is done by pad-printing and direct writing (extrusion) of silver pastes and inks. Efficiencies exceeding 14% on an average have been produced in the manufacturing line, achieving more than 14.7% in some cases [116]. Further reduction of production costs is expected by the growth of large-diameter EFG cylinders, which reduce thermoelastic stresses and can result in thinner and more uniform wafers. Thin curved wafers will require new technology for solar cell processing.

In the case of STR, 14.7% efficiencies have been reported for a process including screen-printed contacts fired with RTP [117], and 50 and 100 W modules are commercially available [118]. Regarding dendritic web, an $n^+ np^+$ structure (phosphorus front diffusion and rear Al alloyed emitter) is implemented on a high-resistivity antimony-doped substrate. Because of the low substrate thickness (100 μm), it can benefit from the location of the *p-n* junction at the back, performing an effective front surface field, enabling a high diffusion length and immunity to light-induced degradation. Using only production-worthy, high-throughput processes, dendritic web cells have been fabricated with efficiencies of up to 14.2% [119].

7.7.2 Heterojunction with Intrinsic Thin Layer

A new structure called HIT has been developed recently, which makes use of the cheaper amorphous silicon (a-Si) technology, depositing a-Si layers on crystalline silicon by

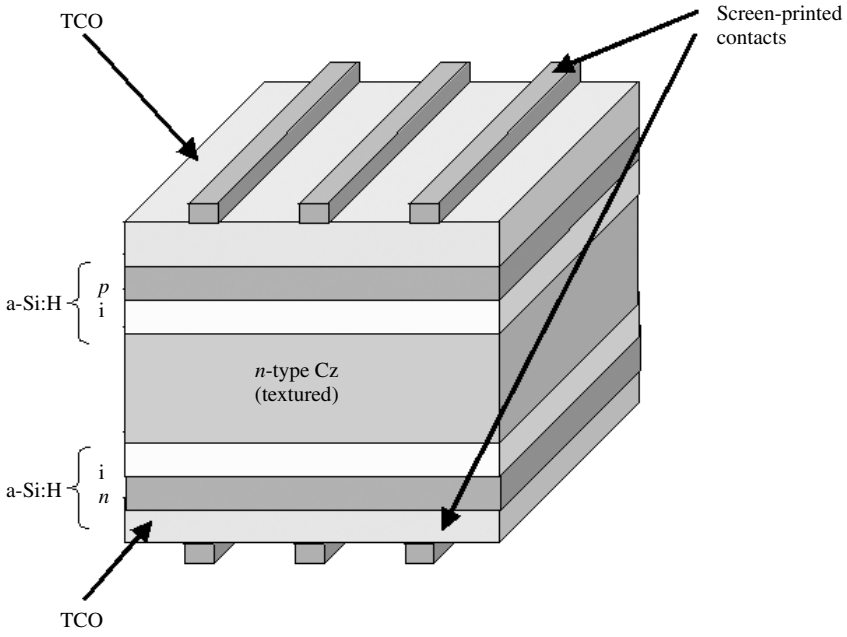

Figure 7.14 Structure of the HIT cell

PECVD [120]. It provides an excellent surface passivation with very low temperature processes (below 200°C), avoiding lifetime degradation of the bulk material. Figure 7.14 shows the structure of the HIT cell. A textured *n*-type Cz-Si substrate is used. The emitter and BSF are made of *p*-type and *n*-type a-Si layers, respectively. Very thin intrinsic a-Si layers are inserted between a-Si and the crystalline substrate, to improve the characteristics of the a-Si/c-Si interface. Thickness of these amorphous layers is on the order of 10 to 20 nm. On both doped layers, transparent conductive oxide (TCO) layers are formed, by sputtering, and metal fingers are screen printed. Back metallization is also comblike to reduce thermal and mechanical stresses, making the cell symmetrical and enabling it to perform as a bifacial cell.

In 1994, 20% efficiency was achieved with a similar HIT structure on a 1 cm^2 cell. Mass production of HIT cells started in 1997, with conversion efficiencies of 17.3% on 100 cm^2 substrates. 180 W modules are fabricated, and special modules exist for roof-tile and bifacial applications.

7.7.3 Buried Contact Technology

The buried contact solar cell process was developed at the University of New South Wales [50]. It is based on forming grooves in the silicon surface, where the metal is deposited by electroless plating, so that high aspect ratios and low metal shading losses are achieved. Several techniques have been proposed for groove formation, laser scribing being the most attractive for large-scale production. A metallized groove, typically 40-μm deep and 20-μm wide, is presented in Figure 7.15. Additionally, other high-efficiency

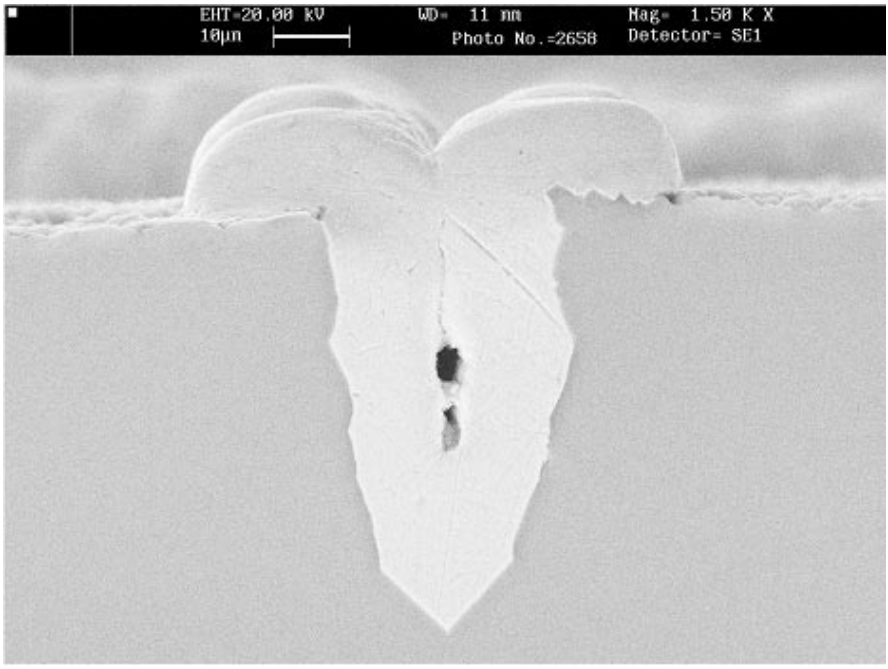

Figure 7.15 Cross-section of a buried contact. (Reprinted with permission from BP Solar)

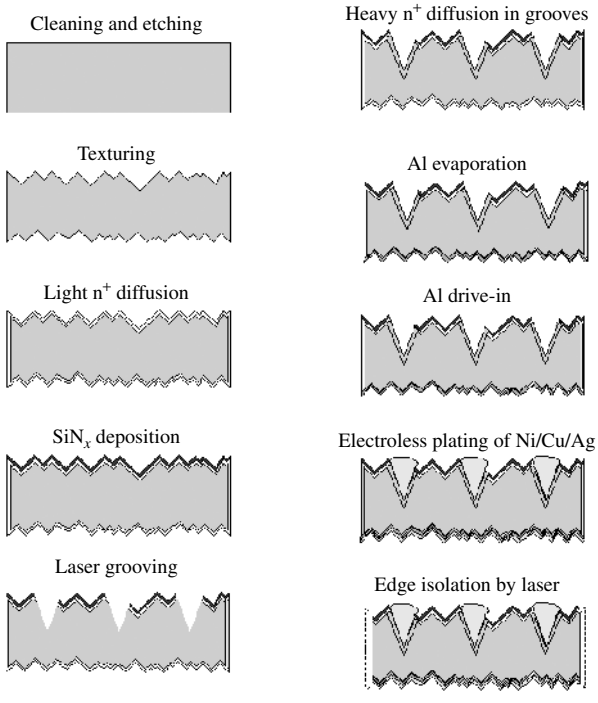

Figure 7.16 Laser-grooved buried-grid solar cell process

features are implemented, such as a selective emitter (highly doped under the metal fingers and low-doped and surface-passivated in the active area) and a Back Surface Field by Al evaporation and alloying, which also produces gettering effect.

The buried contact solar cell has been licensed to many manufacturers, but for the moment only one of them has implemented it at the industrial level, commercializing it as the LGBG solar cell. The LGBG process is sketched in Figure 7.16. Three high-temperature steps are needed, and a number of wet steps must be performed. A key element is the silicon nitride layer, which serves as a masking layer for heavy phosphorus diffusion and plating, and also performs as an antireflection coating and surface passivator. Efficiencies of 17% are routinely achieved with Cz-Si [121], and improvements are being researched and implemented to further increase cell efficiency [122].

The buried contact approach relies on compensating the increase in process complexity as compared to screen-printed technology with an increase in cell efficiency. A midway is proposed with a simplified buried contact solar cell process, with only one high-temperature step, TiO_2 antireflection coating and screen-printed Al BSF [123].

7.8 CRYSTALLINE SILICON PHOTOVOLTAIC MODULES

The power of a single solar cell being small, several of them must be electrically associated to make a practical generator. The module is the building unit for generators that can be purchased in the market, that is, it is the real PV product. Performance and lifetime of PV systems depend on the protection that module construction offers to the active photovoltaic devices.

The basic module fabrication procedure used by most manufacturers was developed three decades ago and is described below briefly. Modules for special applications (building integration, marine operation, etc) require slight modifications of the process and the materials.

7.8.1 Cell Matrix

In a module, the cells are usually arranged in series. After cell finishing, tinned copper ribbons (tabs) are soldered to the bus bars at the front (Figure 7.17a). It has to be noted that tabs must overlap a long distance along bus bar length since the conductance of the printed bus bars is too low. Conductive epoxies can replace conventional solder alloys and illumination used instead of iron heating.

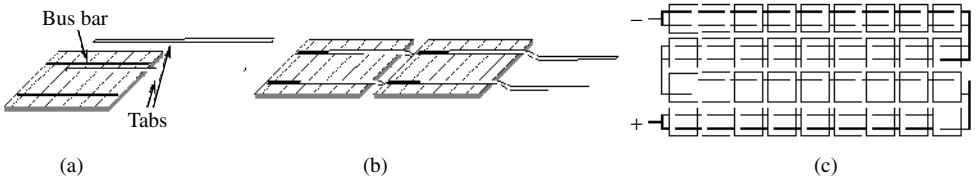

Figure 7.17 (a) Cell interconnection with tabs; (b) two cells in series; and (c) layout of 36 series-connected cells

Two tabs per cell are employed thus providing redundancy that allows current to flow in case electrical continuity is broken because of some failure [124]. Besides, the effective length of grid fingers is one-fourth the cell side and series resistance is alleviated. Tabs provide a nonrigid link between cells that allow thermal expansions to be accommodated.

Series interconnection of strings by soldering the tabs to the rear side of another cell follows (Figure 7.17b). The strings are interconnected with auxiliary tabs to form the cell matrix. This can consist of a single series string or several strings (Figure 7.17c). If the strings are not internally paralleled, their terminals are brought outside the module to permit flexible circuit configuration.

A common module configuration uses 36 series-connected cells, which, under operating conditions, would produce around 15 V at maximum power, appropriate for 12 V battery charging [125]. As building-integrated, grid-connected applications grow, modules with different electrical configurations enter the market.

A few years ago these operations were performed manually, but current factories use sophisticated equipment that performs most of the operations automatically. Both throughput and yield benefit from automation since the connected cells are very fragile and difficult to handle.

7.8.2 The Layers of the Module

The array of cells must be properly encapsulated for reliable outdoor operation for more than 20 years, paying attention to factors like rigidity to withstand mechanical loads, protection from weather agents and humidity, protection from impacts, electrical isolation for the safety of people and so on.

The different layers that the module is made up of are then stacked. A common structure is sketched in Figure 7.18.

A 2- to 3-mm thick soda lime glass is used as a superstrate that provides mechanical rigidity and protection to the module while allowing light through. It must have low iron content or otherwise the light transmission will be low. Modern modules use glass with cerium that absorbs UV radiation to enhance reliability [126]. Tempered glass must be employed to increase the resistance to impacts.

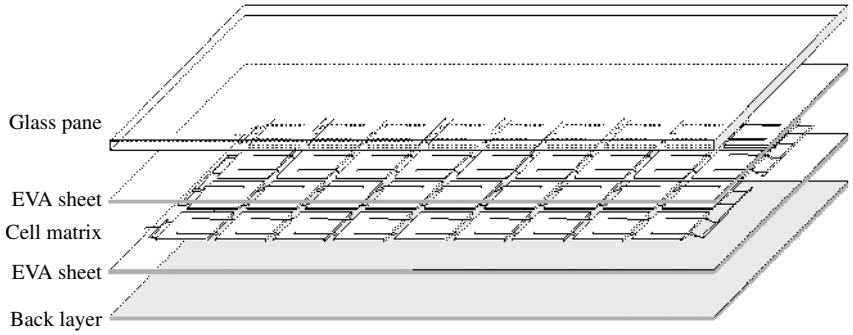

Figure 7.18 Stack of materials to be laminated

The cell matrix is sandwiched between two layers of the encapsulant or pottant material. The most popular encapsulant is the copolymer ethylene-vinyl-acetate (EVA), a plastic composed of long molecules with a backbone of carbon atoms with single covalent bonding. EVA is a thermoplastic, that is, shape changes made under heating are reversible. It is sold in rolls of extruded film around 0.5-mm thick. Along with the polymer, the film contains (1) curing agents and (2) stabilizers whose role will be described later.

The outer layer at the nonilluminated module side is usually a composite plastic sheet acting as a barrier for humidity and corroding species. Some manufacturers use another glass, which increases protection.

7.8.3 Lamination and Curing

These steps are carried out in a laminator, a table that can be heated and furnished with a cover that closes the edges tightly. The cover has an internal chamber and a diaphragm that separates this from the chamber containing the module. Both chambers can be independently evacuated: this configuration allows the module to be kept in a vacuum while mechanical pressure is exerted on it.

In the lamination stage, both chambers are evacuated while temperature is raised above the EVA melting point at around 120°C. Vacuum is important to extract air – to prevent voids from forming – and moisture and other gases. The EVA flows and embeds the cells. After a few minutes, with the module chamber still in vacuum, the upper chamber is filled with air so that the diaphragm presses the laminate. The temperature is increased to 150°C and the curing stage begins: the curing agents induce cross-linking of the EVA chains, that is, chemical bonds are formed transversely among the long molecules that before curing are only weakly linked to one another. The plastic then acquires elastomeric, rubberlike properties and indeed the curing step is analogous to the vulcanization of rubber. This stage takes up to 60 min for standard cure EVA [127]. After cooling down, the laminates are unloaded from the laminator.

Lamination used to be a bottleneck in the module fabrication process. To improve throughput several solutions have been followed by the industry: (1) commercial fast-curing EVA formulations allow drastic reductions of curing time to less than 10 min [128], (2) performing the curing step in a separate oven decreases the residence time in the laminator and (3) a large lamination area – up to several square meters – enables simultaneous process of several modules or very large ones.

Another polymeric material, poly vinyl butyral (PVB), was used in early times of module fabrication. It is processed in a similar way to EVA and can present some advantages over EVA [129] but it requires low temperature storing. For modules using two glass panes, resin fill-in is an alternative to EVA with reliability advantages. A sealed cavity is formed between the glass panes with the cells in-between and the liquid resin is poured into it. Care must be taken to ensure that no bubbles form [125]. Resins do not require heating to cure. Silicone resins are expensive but very stable and some modules for building integration use them. Yet curing can be inhibited by the module sealant so that they are difficult to handle. Acrylic resins with UV curing are being investigated.

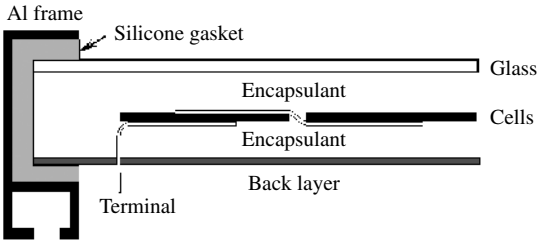

Figure 7.19 Cross-section of a standard module

7.8.4 Postlamination Steps

These include (1) trimming the edges of the laminate to remove spread-out encapsulant, (2) sealing them with silicone rubber to close this potential path of moisture penetration in the module, (3) sticking the plastic junction box at the back of the laminate and performing the connections and (4) when required, installing the anodized aluminum frame (Figure 7.19). The frame must be electrically insulated from the active cell circuit so that high-voltage differences can be sustained between the electrical terminals and the frame without current flow.

Besides, among other final tests, the $I-V$ curve of all modules under standard conditions is measured in a solar simulator to check if they fulfill specifications. Flash simulators are commonly utilized to save energy, with the electronic equipment able to record a complete $I-V$ curve in a fraction of a second. They must have a spectral content matched to the AM1.5 standard, or else, they must be calibrated with a calibrated cell of the same technology.

7.8.5 Special Modules

7.8.5.1 BIPV products

Building integration of PV modules (BIPV) has emerged as one of the most important – by volume – applications of Photovoltaics. Modules perform two tasks: as constructive materials as well as power generators. Modules can be incorporated to a building in a number of ways and special products are being developed so that the typical framed module is no longer the only PV product. Very large modules with special fixing for roof or façade integration, roof tiles with cells and semitransparent modules allowing light through are available. Visual appearance is enhanced by module shape, encapsulation and cell color [130]. Besides, these products must comply with building normative such as fire resistance.

7.8.5.2 Bifacial modules

Several cell structures have been presented that can operate with bifacial illumination. By encapsulation between two glass panes, bifacial modules offering increased power output per unit cell area can be produced without technology changes. In spite of their potential, their presence in the market is very small at the moment.

7.8.5.3 Modules with back contact cells

Several cell structures have been proposed that bring both contacts to the back face, which is usually accomplished by implementing phosphorus diffusions at both faces that are internally connected through processing. They fit the scheme in Figure 7.1(d) [131]. Back contact cells are interconnected without tabs by soldering them to a layer with the connection paths printed, similar to PCB practice in electronic circuits. These experimental designs offer simplified module fabrication and enhanced visual appeal.

7.9 ELECTRICAL AND OPTICAL PERFORMANCE OF MODULES

7.9.1 Electrical and Thermal Characteristics

The voltage of the module is, in principle, the number of series-connected cells times the voltage of the single cell, and the module current the number of paralleled cells times the single cell current. Whatever the combination, the module power equals the power of a single cell times the number of them. Mass-produced modules offered in the catalogues of manufacturers show power ratings that typically range from 50 to 200 Wp, delivered at current levels between 3 and 8 A and at voltages between 20 and 40 V. Lower and higher values are possible for special applications.

The manufacturer usually provides values of representative points (short-circuit, open-circuit and maximum power) of the module $I-V$ curve measured at standard cell conditions (STC), that is, 1 $kW \cdot m^{-2}$ irradiance (=0.1 $W \cdot cm^{-2}$), AM1.5 spectral distribution and 25°C cell temperature. The maximum power of the module under STC is called the peak power and given in watts-peak (Wp). While efficiency has the greatest importance for a solar cell, for a module it has the less relevant meaning since part of the area is not occupied by the expensive solar cells.

The conditions in real operation are not the standard ones; instead, they vary strongly and influence the electrical performance of the cell, causing an efficiency loss with respect to the STC nominal value. This loss can be divided into four main categories [132]:

1. *Angular distribution of light*: Because of the movement of the sun and the diffuse components of the radiation, light does not fall perpendicular to the module, as is the case when measurements are done and the nominal efficiency is determined.
2. *Spectral content of light*: For the same power content, different spectra produce different cell photocurrents according to the spectral response. And the solar spectrum varies with the sun's position, weather and pollution and so on, and never exactly matches the AM1.5 standard.
3. *Irradiance level*: For a constant cell temperature, the efficiency of the module decreases with diminished irradiance levels. For irradiances near one sun, this is primarily due to the logarithmic dependence of open-circuit voltage on photocurrent; at very low illumination the efficiency loss is faster and less predictable.
4. *Cell temperature*: The ambient temperature changes and, because of the thermal insulation provided by the encapsulation, light makes cells in the module heat over it;

higher temperature means reduced performance. This is usually the most important performance loss.

But, prediction of the module response under different conditions is required to correctly assess the yearly production of a PV system in the field. The physical mechanisms of influence of temperature and irradiance on cell performance are well known, so that, in principle, prediction of module output could be rooted in physical models. This is however unpractical and would be a different approach if followed by PV system engineers.

Instead, very simple methods are used for translating the $I-V$ performance to different operating conditions and standardized procedures have been developed for PV modules of industrial technologies [133]. These methods are applicable within a limited range of temperature and irradiance conditions that are not very far from those met when testing the module and which require a small number of easily measurable parameters. The module datasheets from the manufacturers used to include some of these, allowing simplest estimates to be made, such as:

1. The steady-state power balance determines cell temperature: the input is the absorbed luminous power, which is partially converted into useful electrical output and the rest is dissipated into the surroundings. Convection is the main mechanism for heat dissipation in terrestrial, flat plate applications, and radiation is the second nonnegligible mechanism of heat dissipation. A common simplifying assumption is made that the cell-ambient temperature drop increases linearly with irradiance. The coefficient depends on module installation, wind speed, ambient humidity and so on, though a single value is used to characterize a module type. This information is contained in the Nominal Operating Cell Temperature (*NOCT*), which is defined as the cell temperature when the ambient temperature is 20°C, irradiance is 0.8 kW·m^{-2} and wind speed is 1 m·s^{-1}. *NOCT* values around 45°C are typical. For different irradiance values G, this will be obtained by

$$T_{\text{cell}} = T_{\text{ambient}} + G \times \frac{NOCT - 20^{\circ}\text{C}}{0.8\ \text{kW}\cdot\text{m}^{-2}}$$

2. The module short-circuit current is assumed strictly proportional to irradiance. It slightly increases with cell temperature (this stems from a decrease in band gap and an improvement of minority-carrier lifetimes). The coefficient α gives the relative current increment per degree centigrade. By combining both assumptions, the short-circuit current for arbitrary irradiance and cell temperature is calculated as

$$I_{\text{SC}}(T_{\text{cell}}, G) = I_{\text{SC}}(\text{STC}) \times \frac{G}{1\ \text{kW}\cdot\text{m}^{-2}} \times [1 + \alpha(T_{\text{cell}} - 25^{\circ}\text{C})]$$

   For crystalline Si, α is around 0.4% per degree centrigrade.

3. The open-circuit voltage strongly depends on temperature (the main influence is that of the intrinsic concentration), decreasing linearly with it. Knowledge of the coefficient, called β, allows the open-circuit voltage to be predicted by

$$V_{\text{OC}}(T_{\text{cell}}, G) = V_{\text{OC}}(\text{STC}) - \beta(T_{\text{cell}} - 25^{\circ}\text{C})$$

   The irradiance dependence is buried in T_{cell}. For crystalline Si, β is around 2 mV/°C per series-connected cell.

4. A lot of factors affect the variation of the maximum power (or, equivalently, the efficiency) with irradiance and temperature. The parameter γ is defined as the relative decrease in module efficiency per degree centigrade of cell temperature increase

$$\eta(T_{\text{cell}}, G) = \eta(\text{STC}) \times [1 - \gamma(T_{\text{cell}} - 25^{\circ}\text{C})]$$

Usual γ values are near 0.5% per degree centrigrade.

7.9.2 Fabrication Spread and Mismatch Losses

So-called mismatch losses arise when cells with different $I-V$ characteristics are interconnected because of the fewer degrees of freedom left to bias the devices, so that the array output is less than the sum of the powers that the individual cells could deliver. The differences come from the unavoidable fabrication spread or from nonuniform irradiance or working temperature within the array.

To minimize mismatch losses, finished cells are measured and sorted in the factory. For series connection, the important parameter is the current at the maximum power point (mpp). It is the common practice to measure the current before encapsulation at a fixed voltage close to the mpp and to classify the cells accordingly, though other classification criteria are possible [134]. Within each class all devices present similar currents within the specified tolerance that ensures that, when connected in series to form the module, the mismatch loss will be below the desired limit [135]. Depending on the class being processed, the power rating of the resulting module will vary and this explains why manufacturers offer different module families though they are built in exactly the same way.

7.9.3 Local Shading and Hot Spot Formation

Because of local shading or failure, one or several solar cells can present a much smaller short-circuit current than the rest of devices in the series string. If the defected cells are forced to pass a current higher than their generation capabilities, they become reverse-biased, even enter the breakdown regime, and sink power instead of sourcing it.

Figure 7.20 illustrates this behavior for an 18-cell string with one cell shaded so that its short-circuit current is half that of the remaining devices. String short-circuit is marked with a horizontal line, showing that in this condition the shaded cell is strongly reverse-biased and dissipates the power produced by the unshaded cells. This effect of course severely degrades the efficiency of the module, but more important is the fact that it can get damaged.

Avalanche breakdown is characterized by a nonuniform distribution of current across the junction, breakdown occurring preferentially at localized regions, possibly correlated to damage during processing. Intense local heating can produce very high temperatures (a hot spot). If a temperature of around 150°C is reached, the lamination material becomes degraded and the module irreversibly deteriorated [136, 137]. Because of the localized nature of the process solar cells show large scattering in their reverse characteristics so that the module behavior under partial shading is not accurately predictable.

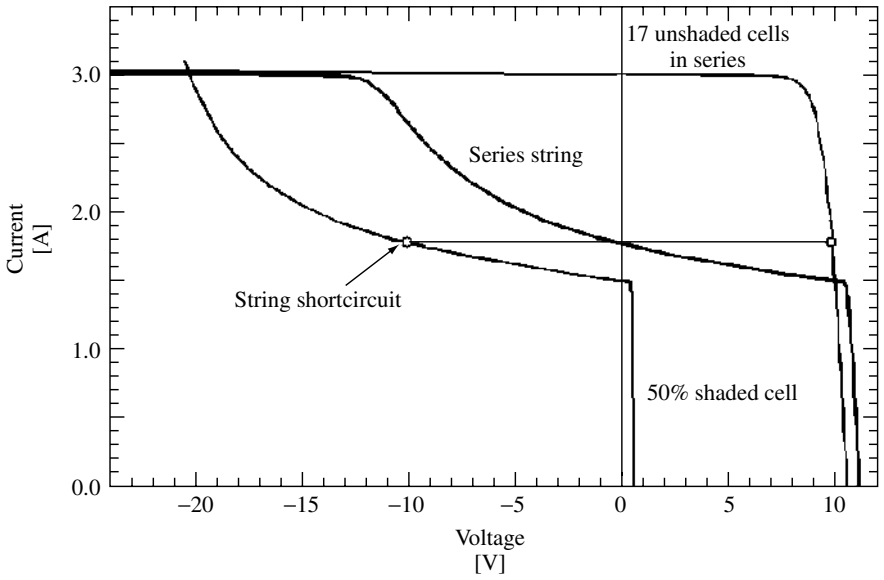

Figure 7.20 Computer simulation of the $I-V$ curves of a 50% shaded cell, showing the typical "soft" reverse breakdown, and of 17 identical cells, unshaded, in series. When series-connected with the shaded cell, the curve labeled "series string" is obtained

In order to devise the means of preventing hot spot failure from occurring, the worst case is considered. This occurs when the N-cell series string is short-circuited and a shaded solar cell is reverse-biased with the voltage of the remaining $N-1$ good devices, as shown in Figure 7.20. The minimum N that will lead to hot spot formation (i.e. the maximum N for safe operation) depends on rather uncontrollable factors, as explained. For Si solar cells of standard technology, it is around 15 to 20.

Since larger series strings are generally used, the approach followed is to put a diode (bypass diode) in parallel, but in opposite polarity, with a group cells. The number of cells in the group is chosen so that hot spots cannot be formed. When one or several cells are shaded, they are reverse-biased only to the point where the diode across the group starts forward conduction. The diode carries away the necessary current to keep the group near short-circuit.

Figure 7.21 illustrates the operation of the bypass diodes. When the current forced through the shaded substring is such that the reverse bias equals the diode threshold voltage, the bypass diode sinks all necessary current to keep the string at this biasing point thus preventing the power dissipated in the shaded cell to increase. It is also apparent that the bypass diode leads to a significant increase of output power allowing the module to keep delivering the power generated by the unaffected groups.

It is clear then that the smaller the number of cells per bypass diode, the lower the efficiency loss for a shading condition, but this means a higher cost and more complex fabrication. It has been proposed to integrate a bypass diode in each cell so that these effects will be minimized at the expense of more complicated cell processing [138].

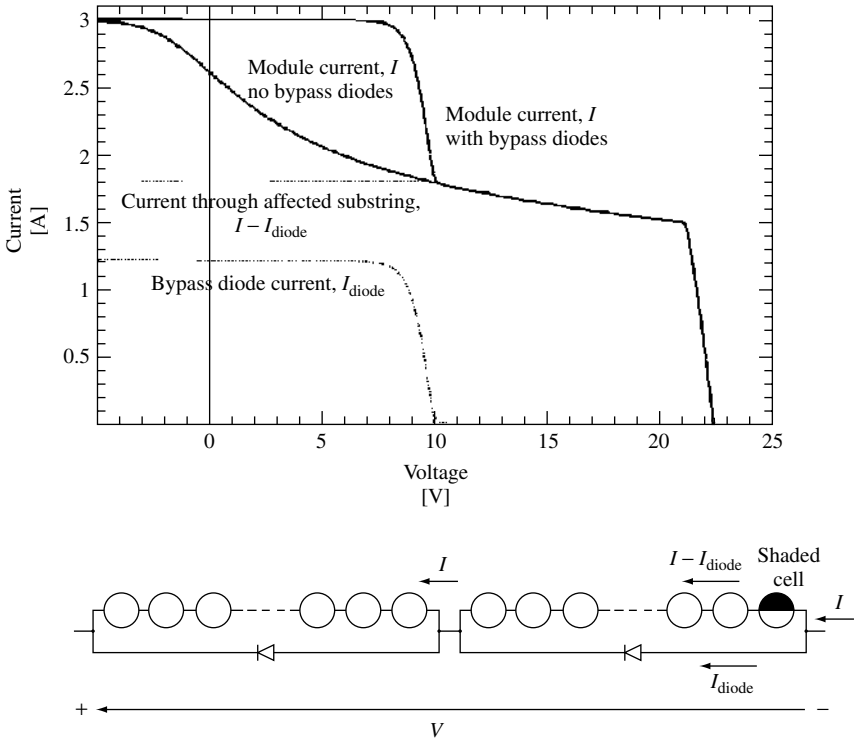

Figure 7.21 Computer simulation of the $I-V$ curves of a 36-cell series string without and with two bypass diodes, connected as shown in the bottom of the figure, when one cell is 50% shaded. The currents through the shaded substring and its bypass diode are also shown

The practice is to take electrical terminals outside the encapsulation not only for the extremes of the series string, but also for intermediate points as well, so that bypass diodes are connected in the junction box 12 or 18 cells each (Figure 7.22). Endurance to shading is a standard test for module qualification.

The influence of local shading on the module output depends on the details of the $I-V$ curve of the cells as well. Under certain circumstances of partial shading, it is beneficial that the cells show some shunt resistance. However, tight control of leakage currents by processing is not easy.

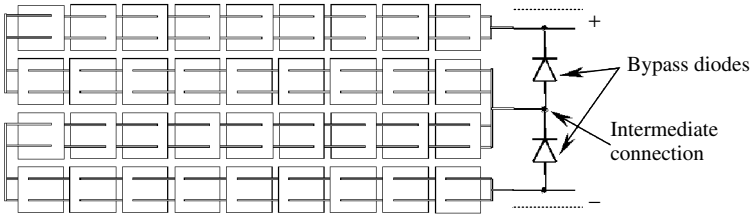

Figure 7.22 Two bypass diodes in a 36-cell module. The connections are done in the junction box

7.9.4 Optical Properties

The encapsulation affects the optical properties of the cells in several ways. The optical properties of the cells must be optimized attending to cost and performance after encapsulation.

Some effects of encapsulation are [139] as follows:

- The refraction index of glass and EVA is similar, around 1.5, between those of air and Si. Encapsulation acts, then, as a thick AR. For well textured Si solar cells, this antireflection action is enough and sometimes no thin ARC is used.
- The design of the ARC coating must account for the fact that the cell is illuminated from a medium with this index. The optimum ARC refractive index is larger than in air.
- Glass and EVA absorb some light in the short-wavelength range.
- Typically, 4% reflection occurs at the air–glass interface [Figure 7.23 (1)]. ARC coatings and texturing can be applied to decrease this loss.
- The light reflected by the metal fingers and the cell surface, if the reflected rays are tilted with respect to the normal to the glass surface, can be partly recovered by total internal reflection at the glass–glass interface [Figure 7.23 (2)]. This effect could be enhanced by texturing the cell surface with tilted pyramids, instead of the upright pyramids obtained by alkaline etching of (1 0 0) surfaces [140].
- Though the trapping capabilities of the cell, due to the lower difference in refractive index, appear to worsen with encapsulation, the escaped rays are trapped in the glass so that the absorption enhancement in the ideal case is not affected.
- For cells without a back metal mirror, the transmitted light can be recovered by putting a reflector, detached from the cell, at the back of the module [Figure 7.23 (3)]. The back plastic layer, if white, serves this purpose.
- The same white layer, since it reflects diffusively, allows some of the light incident between the cells to be collected [Figure 7.23 (4)].

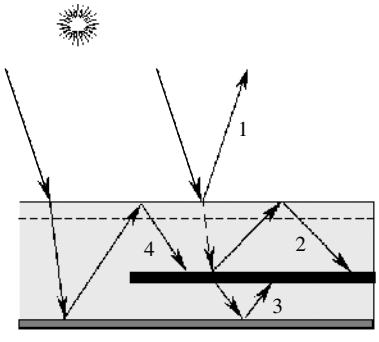

Figure 7.23 Optical effects of encapsulation: (1) glass reflection; (2) trapping of cell reflectance; (3) trapping of cell transmittance; (4) collection of peripheral light

7.10 FIELD PERFORMANCE OF MODULES

7.10.1 Lifetime

Long lifetime is claimed as one of the main virtues of PV and some manufacturers currently offer warranty for more than 20 years, with 30-year lifetime being the objective for short-term development. This should mean that for this period of time the module will keep working, that is, producing electrical power with an efficiency similar to the starting efficiency and without deterioration that compromises the safety or the visual appearance. Two factors determine lifetime: reliability, that refers to premature failure of the product, and durability, that attends to slow degradation that eventually decreases production to unacceptable levels. Cost effectiveness, energy payback balance and public acceptance of photovoltaic energy strongly rely on the reliability and the long lifetime of modules.

PV systems worldwide have been working for more than 20 years, and this allows us to gather information concerning degradation mechanisms. Modules in the field are subjected to static and dynamic mechanical loads, thermal cycling, radiation exposure, ambient humidity, hail impact, dirt accumulation, partial shading and so on. Common failure modes [124, 141] are related to the action of weather agents in combination with deficiencies in fabrication.

Location-dependent steady degradation of module output is also observed, with short-circuit current and fill factor being the most affected parameters. In many cases, this has been proved to correlate with degradation of EVA encapsulation [127]. EVA, like most polymers, is known to undergo photothermal degradation: UV radiation breaks molecular chains. Diffusion of chemical species is also relatively easy through it, so that moisture and corroding agents can enter while absorbers and stabilizers can out-diffuse.

Yellowing or browning of EVA reduces its optical transmission affecting module current. For this reason, EVA incorporates UV absorbers in its formulation. Cerium-containing glasses alleviate this problem. Degradation also decreases the strength of the encapsulant, leading to loss of adhesion to the cells and even detachment of the layer (delamination). This is promoted by the shear stress that accompanies different expansion coefficients upon diurnal thermal cycles. Delamination brings about optical and thermal degradation. Besides, the degraded encapsulant can be penetrated more easily by moisture and chemicals. Among these, sodium from the glass and phosphorus from the cell emitter are known to precipitate at the cell surface, corroding solder joints and increasing series resistance [141]. Encapsulant formulations are being continuously improved to address these problems.

7.10.2 Qualification

Several organisms, such as the International Electrotechnical Commission (IEC), the Institute of Electrical and Electronic Engineers (IEEE) and so on, have designed tests aimed at guaranteeing the quality of PV products [142]. Test procedures have been defined that, if successfully passed by a product, should guarantee the reliability of the PV module.

Manufacturers voluntarily submit their products for qualification tests in an accredited laboratory. These include verification of the module performance claimed in the datasheets as well as reliability tests. The certifications obtained are intended as a quality assurance for the customer.

Qualification tests consist in verifying the module integrity by visual inspection, measurement of the electrical performance at STC and of the electrical isolation before and after treatments that simulate, in an accelerated manner, real operation conditions. For instance, the IEC Standard 61 215 [143] specifies the following:

- Ultraviolet exposure using xenon lamps.
- Thermal cycling (-40°C to 50°C, 50 cycles) in climatization chamber.
- Humidity freeze cycling (thermal cycling with 85% relative humidity).
- Damp heat (1000 h at 85°C and 90% relative humidity).
- Twist test for testing resistance to torques.
- Pressure is applied to the module to test resistance to static mechanical loads.
- Hail impact test, where the module is stricken by 25 mm diameter ice balls at 23 m seg^{-1}.
- Outdoor exposure.
- Hot spot tests, where the module is selectively shaded.

Different test combinations are applied to a sample of a few modules. The modules will qualify if no major failures are found and the visual inspection reveals no damage, the electrical power is within 90% of specifications, and isolation is maintained.

7.11 CONCLUSIONS

This chapter has reviewed current state of crystalline silicon solar cells and modules. The main lines defining the structure of the described situation can be summarized as follows:

- *Changing scale*: The current booming of the markets enables and fosters technological and processing improvements.
- *Laboratory-industry gap*: There is a mature technology at the laboratory that has led to impressive performance levels, on the one hand, and a reliable, fast, 30-year-old industrial process producing modest efficiency, on the other hand. Closing this gap is the key to a lower \$ Wp^{-1} figure of merit.
- *Novel silicon materials*: Market growth and the threat of silicon shortage stimulates new materials and very thin substrates that demand new technological solutions.
- *Technology diversification*: These two challenges are to be faced by solar cell production technology in the coming years. Intensive preindustrial research is being conducted and solutions are being developed along several different lines.
- *Quality*: Product reliability and durability and environmental and aesthetical friendliness are as important as cost for the growth of PV industry and this also influences technology.
- *Long-term scenario*: Alternatives to crystalline silicon technology are being researched thoroughly and presumably some of them will succeed in reducing photovoltaic costs to competitive ones. Nevertheless, for these so-called "leapfrogs" to take place, a mature PV market should consolidate, for which silicon technology is essential at least for the next decade.

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