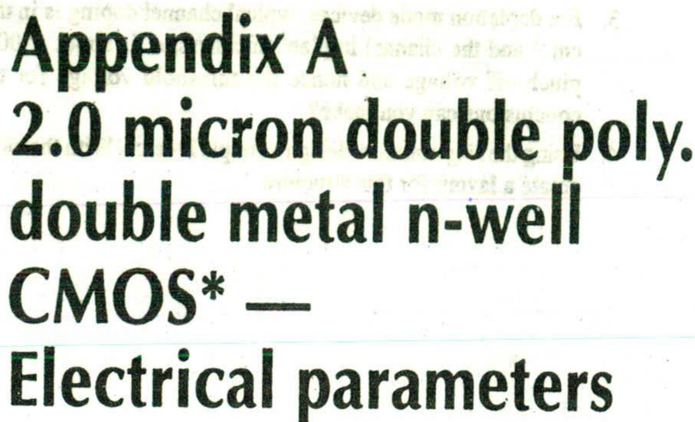

Appendix A 2.0 micron double poly. double metal n-well CMOS* — Electrical parameters

Process specs: 2.0 micron double poly. double metal n-well CMOS*

Oxide thickness (angstroms)	Minimum	Typical	Maximum
Poly. 1 gate oxide	370	400	430
Poly. 2 oxide	470	500	530
Field oxide (poly. 1 & 2 to sub.)	5500	6000	6500
Metal 1 to poly. 1 & 2	8000	8500	9000
Metal 1 to sub.	13500	14500	15500
Metal 1 to n^+/p^+ diff.	8500	9000	9500
Metal 2 to metal 1	6000	6500	7500
Poly. 1 to poly. 2	650	750	850
Conductors			
Poly. 1	3700	4000	4300
Poly. 2	3700	4000	4300
Metal 1	5500	6000	6500
Metal 2	10500	11500	12500

* In all cases, the serious user is advised to contact Orbit for their latest process details.

Device specs: 2.0 micron double poly. metal n-well CMOS

P-channel poly. 1	Minimum	Typical	Maximum
Threshold (volts)	−1.0	−0.75	−0.5
Gamma (volts **.5)	0.45	0.55	0.65
K' = μCox/2 (μA/V**2) VDS = 0.1V, VGS = 2 − 3V	6.0	7.5	8.5
Punchthrough for min. length channel (volts)	−16	−14	−10
Subthreshold slope (volts** −3/decade)	90	100	110
Delta length = effective-drawn (microns)	−0.7	−0.4	−0.1

Poly. 2 etch delta from mask C.D. to wafer is 1.1 μm.
For drawn C.D. of 2 μm, and biased to 3 μm, the final wafer dimension is 2.0 μm.
Recommended minimum poly. 2 gate width is 2.5 μm but interconnect can be 2.0 μm.

P-channel poly. 2	Minimum	Typical	Maximum
Threshold (volts)	−1.5	−1.15	−0.8
Gamma (volts **.5)	0.5	0.6	0.8
K' = μCox/2 (μA/V**2)	5.0	6.0	7.0
Punchthrough for min. length channel (volts) 2.5 μm	−16	−14	−10
Subthreshold slope (volts** − 3/decade)			
Delta length = effective − drawn (microns)	−0.8	−0.5	−0.2

N-channel poly. 1	Minimum	Typical	Maximum
Threshold (volts)	0.5	0.75	1.0
Gamma (volts **.5)	0.15	0.25	0.35
K' = μCox/2 (μA/V**2) VDS = 0.1V, VGS = 2 − 3V	20	23	26
Subthreshold slope (volts** − 3/decade)	90	100	110
Punchthrough for min. length channel (volts)	10	14	16
Delta length = effective-drawn (microns)	−0.7	−0.3	−0.0

Poly. 2 etch delta from mask C.D. to wafer is 1.1 μm.
For drawn C.D. of 2 μm, and biased to 3 μm, the final wafer dimension is 2.0 μm.
Recommended minimum poly. 2 gate width is 2.5μm but interconnect can be 2.0 μm.

N-channel poly. 2	Minimum	Typical	Maximum
Threshold (volts)	0.7	1.10	1.40
Gamma (volts**.5)	0.215	0.30	0.40

	Minimum	Typical	Maximum
K' = μCox/2 (μA/V**2)	18	20	22
Subthreshold slope (volts** – 3/decade)			
Punchthrough for min. length channel (volts) 2.5 μm	10	14	16
Delta length = effective – drawn (microns)	−0.8	−0.4	−0.1
CCD channel potential (volts)			
Poly. 1 VG = 0	3.0	5.0	8.0
Poly. 2 VG = 0	3.0	5.0	8.0

NPN transistor in the n-well

Beta = 80 to 200 at $I_B = 1\mu A$

BVEBO	= 10V
BVCEO	≥ 10V
BVCES	> 10V
BVCBO	≥ 60V
P-base Xj	= 0.45 to 0.50 micron
N+ emitter Xj	= 0.3 micron
Rcollector	= 1.0 +_0.2 kohm/sq
P- base resistance	1.2 + _0.2 kohm/sq
Early voltage	> 30 volts

Sheet resistance (ohms per square)

	Minimum	Typical	Maximum
P+ Active	40	57	80
N+ Active	20	28	40
N-well	2000	2500	3000
Poly. 1	15	21	30
Poly. 2	18	25	30
Metal 1	.050	.070	.090
Metal 2	.030	.040	.050

Contact Resistance (ohms)	Minimum	Maximum
	(single contact 2 by 2μm)	
Metal 1 to p^+ Active	35	75
Metal 1 to n^+ Active	20	50
Metal 1 to poly. 1	20	50
Metal 1 to poly. 2	20	50
Metal 1 to metal 2	0.4	0.7

Field inversion and breakdown voltages (volts)

	Minimum	Typical	Maximum
N-channel poly. 1 field inversion	10	14	
N-channel poly. 2 field inversion	10	14	
N-channel metal 1 field inversion	10	14	
P-channel poly. 1 field inversion		–14	–10
P-channel poly. 2 field inversion		–14	–10
P-channel metal 1 field inversion		–14	–10
N-diffusion to substrate junction breakdown		14	16
P-diffusion to substrate junction breakdown		15	18
N-well to P-subjunction breakdown		50	90

Interlayer capacitances (Plate: 10** – 5 pF micron ** – 2)

	Capacitance		Equiv. thickness	
	Min.	Max.	Min. (angstroms)	Max. (angstroms)
Gate oxide plate poly. 1	78	90	370	430
Gate oxide plate poly. 2	64	70	470	530
Poly. 1 to poly. 2 over active	43	55	650	850
Poly. 1 to poly. 2 over field	43	55	650	850
Metal 1 to active plate	3.6	4.0	8500	9500
Metal 1 to subs plate	2.2	2.5	13500	15500
Metal 1 to poly. plate	3.7	4.4	8000	9000
Metal 2 to active plate	1.9	2.4	14500	17500
Metal 2 to subs plate	1.5	1.65	19500	22000
Metal 2 to poly. plate	1.9	2.4	14500	17500
Metal 2 to metal 1 plate	4.6	5.6	6000	7500

Appendix B
1.2 micron single poly. double metal n-well and p-well CMOS*— design rules and process and device specifications

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* In all cases, the serious user is advised to contact Orbit for the latest design rules and process details.

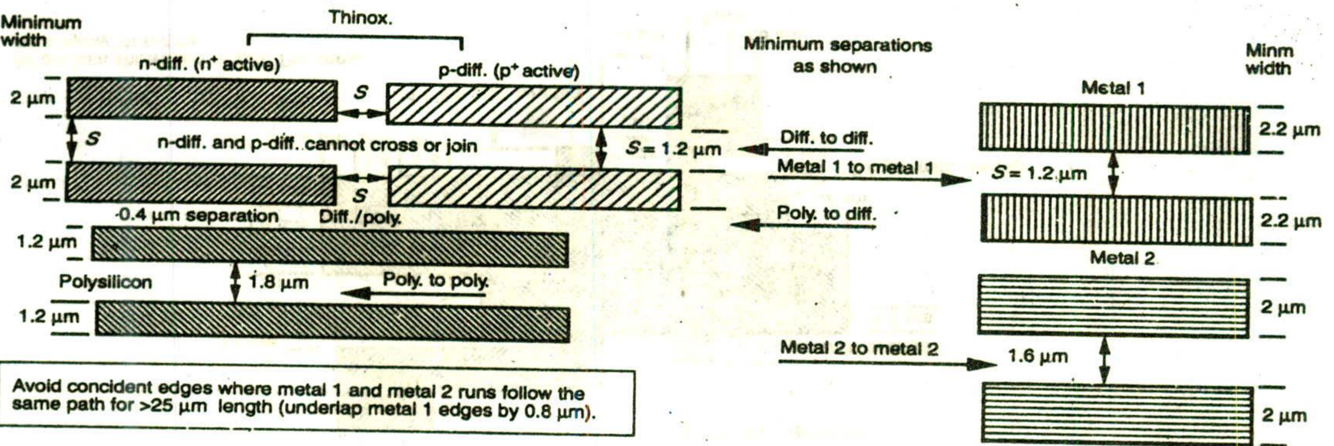


Figure B–1(a) Design rules for wires (interconnects) (Orbit 1.2 µm CMOS)

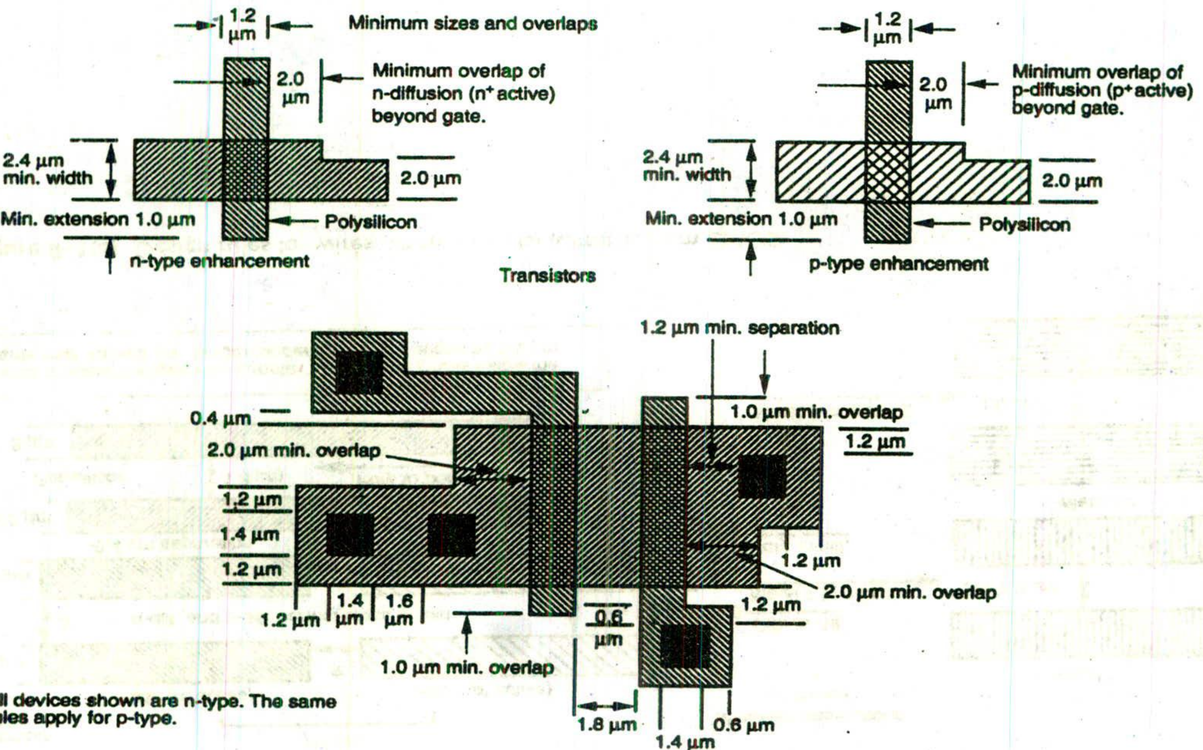


Figure B–1(b) Transistor-related design rules (Orbit 1.2 µm CMOS) minimum sizes and overlaps

1) Metal to polysilicon

0.6 µm
0.8 µm 1.4 µm
1.4 µm
2.2 µm min. width
1.2 µm 2.6 µm 3 µm
1.4 µm
3 µm 2.6 µm
Metal 1/polysilicon

2 µm
Metal 1/ p⁺active
2.2 µm min. width
1.4 µm 3 µm 3.8 µm

(2) Metal 1 to active

Metal 1 /n⁺active
2 µm
1.4 µm 3 µm 3.8 µm
2.2 µm min. width

S
2.2 µm min. width
S
S = 1.6 µm min. separation

(3) Multiple contact cuts

2 µm
0.8 µm 1.0 µm
2.2 µm
1.4 µm
0.8 µm 1.0 µm
1.4 µm
0.8 µm 0.8 µm
1.0 µm 1.0 µm

(4) Via metal 1/metal 2

5) Vias from metal 2 to metal 1 and thence to other layers

1 µm min. space from via to polysilicon or active edge
1 µm 0.6 µm 1 µm Via outside active to active edge
2 µm min. width
1.4 µm 1.4 µm 1.4 µm 1.6 µm 1.4 µm
3 µm min. width
3.4 µm 3.0 µm
0.8 µm 1 µm for poly.
1.4 µm 1.8 µm for active
0.8 µm
2.2 µm min. width
1.4 µm
0.6 µm 1 µm
1.2 µm min. width
1.6 µm
Via to via min.
1 µm min. space from via inside poly. or 1.8 µm min. for via inside active to edge

Note: Vias must not be placed over contacts.

Figure B–1(c) Rules for contacts and vias (Orbit 1.2 µm CMOS)

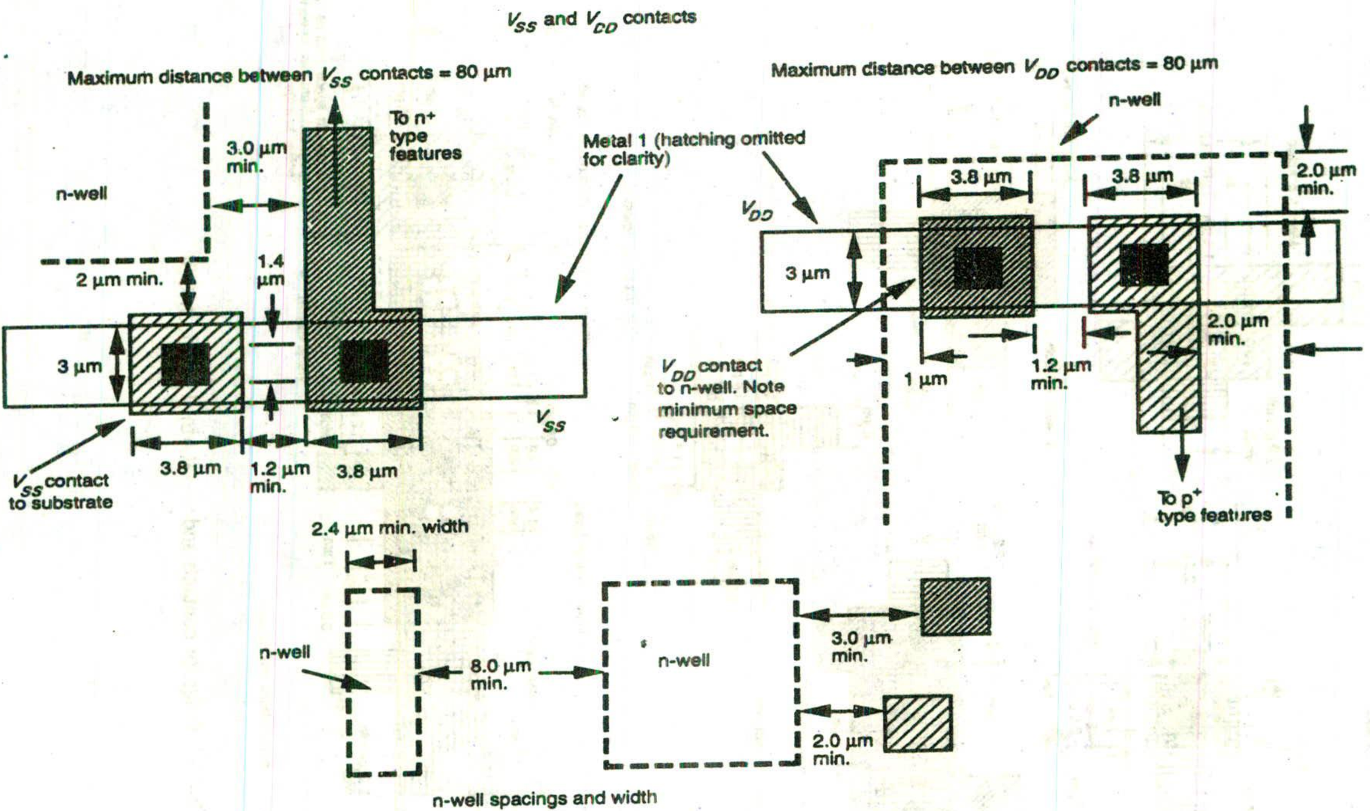
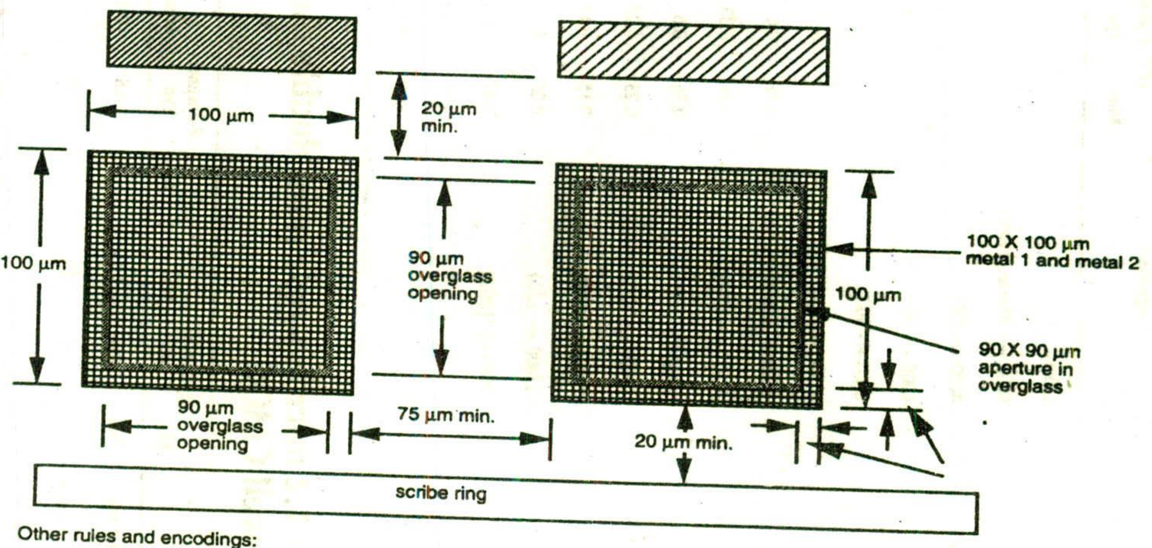


Figure B–1(d) Rules for n-well (Orbit 1.2 μm CMOS process)



Other rules and encodings:

Via overlap of pad 2 μm.
Pad to active separation 20 μm min.
Color encoding for overglass mask . . . gray.

Figure B–1(e) Rules for pad and overglass geometry (Orbit 1.2 μm CMOS)

	Thickness/separation (angstroms)	Capacitance (10^-4 pf/um^2) Min.	Typ.	Max.
Gate oxide	225 +/- 25			
Field oxide	6000 +/- 300 (as grown)			
Poly.	4000 +/- 250			
Intermediate oxide	6000 +/- 600			
Metal 1	6000 +/- 500			
Metal 2	11500 +/- 750			
Metal 1 to polysilicon	6000 +/- 10000	0.56	0.6	0.68
Metal 1 to substrate	11000 +/- 1000	0.31	0.33	0.35
Metal 1 to diffusion	6000 +/- 1000	0.56	0.6	0.68
Metal 2 to poly. 1	13000 +/- 1500	0.25	0.28	0.31
Metal 2 to substrate	20000 +/- 2000	0.15	0.17	0.18
Metal 2 to diffusion	13000 +/- 1500	0.25	0.28	0.31
Metal 2 to metal 1	7000 +/- 10000	0.42	0.50	0.56
N+ to P– JCN		3.1	3.87	4.7
P+ to N – JCN		3.0	3.74	4.4

Device specs: 1.2 micron single poly. double metal n-well and p-well CMOS

	N-channel Min.	Typ.	Max.	P-channel Min.	Typ.	Max.	
VTE (VBS = 0) 30 x 1.2 μm	0.6	0.8	1.0	–1.0	–0.8	–0.6	(volts)
BVDSS (VBS = 0) 30 x 1.2 μm		10	13	–13	–10		(volts)
IDS @ VGS = 5V, VDS = 5V, L = 1.2μm	0.18	0.2	0.22	– 0.11	– 0.093	– 0.083	(mA/micron
K Prime (linear) 30 x 30 μm	30	33	36	7.5	9.5	11.5	(μA/V**2)
Leff @ Ldrawn = 1.2 μm	0.8	0.9	1.0	1.0	1.1	1.2	(microns)
Oxide encroachment/side	0.48	0.52	0.56	0.48	0.52	0.56	(microns)

BE (short channel) 1.2 μm = delta VT (VBS = 0,2)	0.4	0.6	0.8	0.2	0.35	0.5	(volts)
BE (long channel) 30 μm = delta VT (VBS = 0,2)	0.5	0.7	0.9	0.3	0.45	0.6	(volts)
VTF polysilicon		10	13	–13	–10		(volts)
Diffusion resistance	25	35	45	50	70	100	(ohm/sq)
Poly. resistance	15	20	30	15	22	30	(ohm/sq)
Substrate resistance		1.3	1.6	1.8			(kohms/sq)
Substrate Cs	1E16	1.5E16	2E16	6E15	7E15	8E15	(/cm)
Diffusion junction	0.25	0.3	0.35	0.25	0.3	0.45	(microns)
Well junction	3.5	4.0	4.5	3.5	4.0	4.5	(microns)
Oxide spacer		0.2			0.2		(microns)
Contact resistance (1.4 x 1.4 μm)		75			150		(ohms)
Junction breakdown voltage		15			15		(volts)
N-well to P-substrate breakdown			45				(volts)
Metal 1 sheet resistance		35	45	55			(mohm/sq)
Metal 2 sheet resistance		20	25	30			(mohm/sq)

The UCB-Mosfet model in TECAP is an exact copy of the model in U. C. Berkeley's 2g.5 and 2g.6 versions of SPICE, except for the parameter WD.

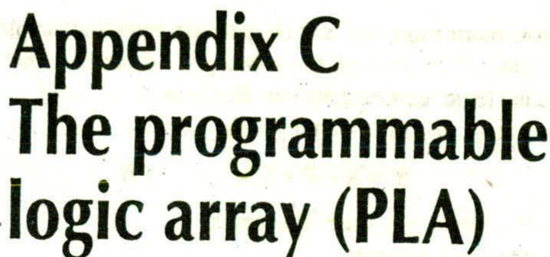
The TECAP model takes oxide encroachment and any biasing between drawn and mask into account through the parameter WD†. The effective channel width Weff is W-2*WD, where W is the drawn channel width. When doing SPICE simulations, use Weff as the device channel width. It is important to take WD into account for devices whose drawn channel widths are small. The other parameters that SPICE needs are L, AS, and AD, which are the drawn channel length, the area of the source and the area of the drain respectively. Do not enter in the effective channel length L. SPICE figures out the effective channel length for you by internally subtracting twice the lateral diffusion from the drawn channel length that you enter.

Because of the different biasing of the drawn active layer for each rule set, there is a different value of WD† associated with each rule set and it may be found in the beginning of each of the rule set descriptions.

† Parameter WD (channel width reduction) = 0.4 μm for Orbit 1.2 μm technology and WD = 0.25 μm for Orbit 2 μm technology.

Corner simulations may be done by using the following fast and slow models:

Fast model — change values Weff, L, and Tox to Weff + 0.25 microns, L – 0.15 microns, and Tox = 21.0 nanometers respectively.
Slow model — change values of Weff, L, and Tox to Weff – 0.25 microns, L + 0.15 microns, and Tox = 24.0 nanometers respectively.



Appendix C The programmable logic array (PLA)

An elegant solution to the mapping of irregular combinational logic functions into regular structures is provided by the PLA. The PLA provides the designer with a systematic and regular way of implementing multiple output functions of n variables in sum of products (SOP) form. The general arrangement of a PLA is given as Figure C–1 and it may be seen to consist of a programmable two-level *And/Or* structure.

Clearly, the structure is regular and may be expanded in any of its dimensions — the number of input variables v, the number of product (*And*) terms p, and the number of output functions (*Or* terms) z. It will also be noted that if there are v input variables, for complete generality each of the product forming *And* gates must have v inputs, and if there are p product terms, each output *Or* gate must have p inputs.

In practice, a range of 'off-the-shelf' PLAs is available to the TTL-based system designer. Typically, PLAs with 14 variable inputs, 96 product terms, and eight output functions are readily obtained, and much larger PLAs (e.g. with more than 200 product terms) are also available. Such elements are programmed by the manufacturer or field programmed by the user to meet requirements.

In VLSI design, however, custom PLAs can be readily designed and must be 'programmed' during the design process. Thus for the VLSI designer, PLAs are tailored to specific tasks with little wastage of functions or space. However, the PLA structure is regular and readily expanded, contracted, or modified during design. This contrasts sharply with the attributes of random logic.

In VLSI design our objective is to map circuits onto silicon to meet particular specifications. The way in which a PLA maps onto the chip may be indicated by a 'floor plan' which gives the notional areas and relative disposition of the particular circuits and subsystems. A floor plan layout for a PLA is given in Figure C–2(a).

For MOS fabrication, *And* and *Or* gates are neither as simple nor as suitable as the *Nor* gate. Thus, we look to De Morgan's theorem to manipulate *And-Or* combinational logic requirements into *Nor* form.

For an *n* input *Nor* gate, we may write

$$X' = A + B + C + \ldots\ldots + N$$

where *X* is the output and *A* to *N* the inputs.

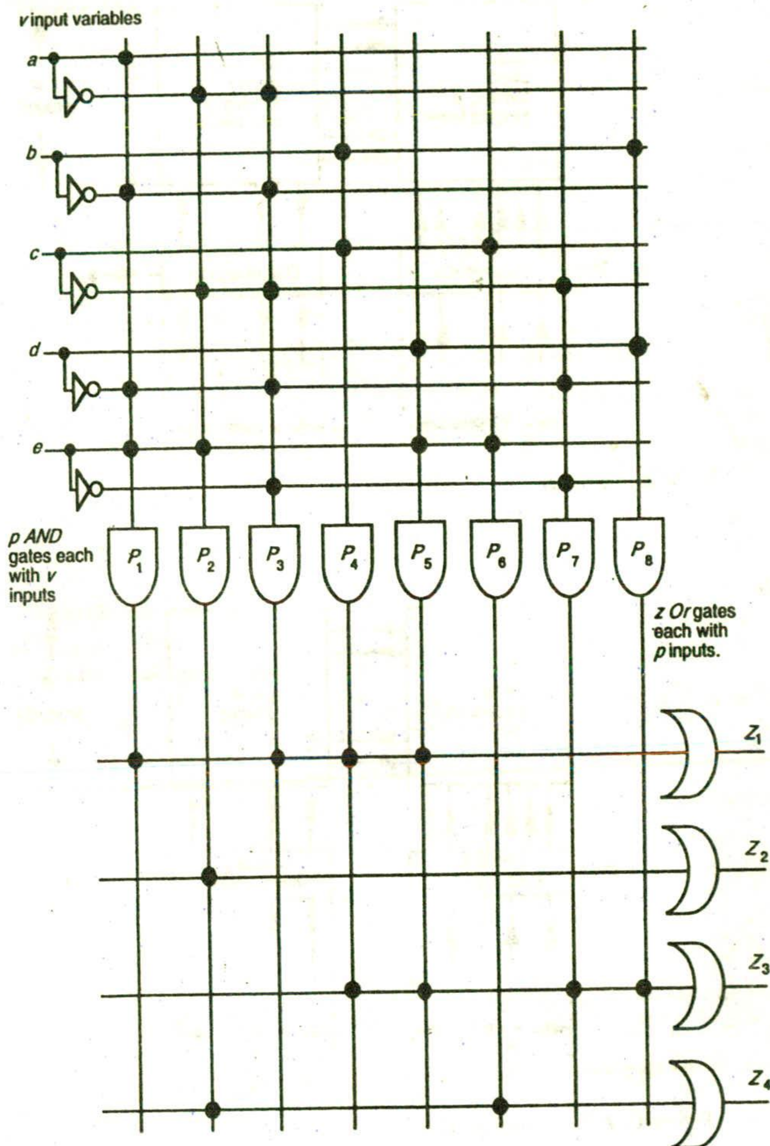
By De Morgan's theorem

$$X = A'.B'.C' \ldots\ldots N'$$

In other words, the *Nor* gate is an *And* gate to inverted input levels.

Obviously, the output *Or* functions of the PLA can be realized with *Nor* gates each followed by an inverter. Thus, the requirements and floor plan of the PLA may be adapted to *Nor* gate form as in Figure C–2(b). A MOS *Nor* gate-based PLA realization for the multiple output functions used as an example in Figure C–1 is presented in circuit form as Figure C–3.

It will be noted that Figure C–3 is a PLA, tailored to meet the particular needs and drawn in mixed circuit and logic symbol notation. Although not in mask layout form, it can be clearly seen how the factors *v*, *p*, and *z* affect the PLA dimensions. A PLA circuit is readily turned into a stick diagram and then to mask layout form. A similar 4 × 8 × 4 programmed PLA is given in stick diagram form as Figure C–4 and the regular nature of the topology is clearly apparent. The reader is left to determine the functions implemented by this PLA.



Note: 5 × 8 × 4 PLA shown symbolically and programmed for:

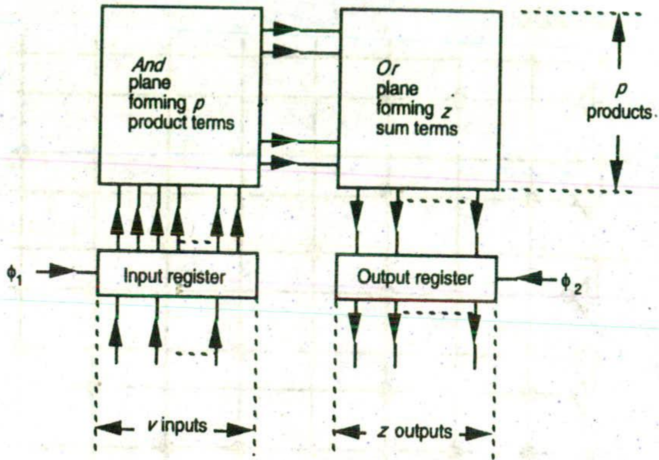
$Z_1 = p_1 + p_3 + p_4 + p_5 \therefore Z_1 = a\bar{b}\bar{d}e + \bar{a}\bar{b}\bar{c}\bar{d}\bar{e} + bc + de$

$Z_2 = p_2 \qquad \therefore Z_2 = \bar{a}\bar{c}e$

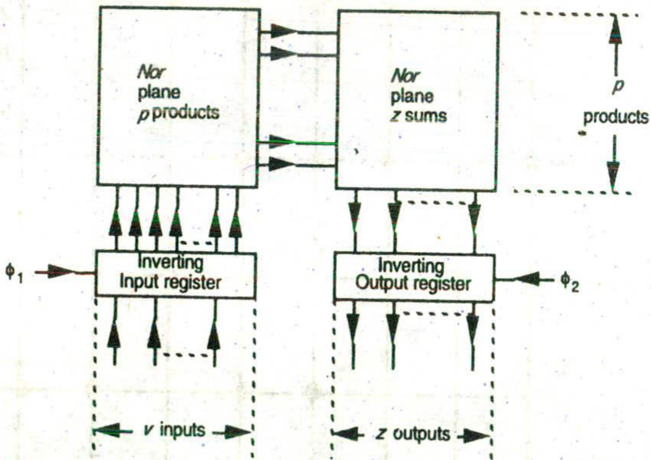
$Z_3 = p_4 + p_5 + p_7 + p_8 \therefore Z_3 = bc + de + \bar{c}\bar{d}\bar{e} + bd$

$Z_4 = p_2 + p_6 \qquad \therefore Z_4 = \bar{a}\bar{c}e + ce$

Figure C–1 $v \times p \times z$ PLA



(a) *And/Or* based



(b) *Nor* based

Figure C–2 PLA floor plans

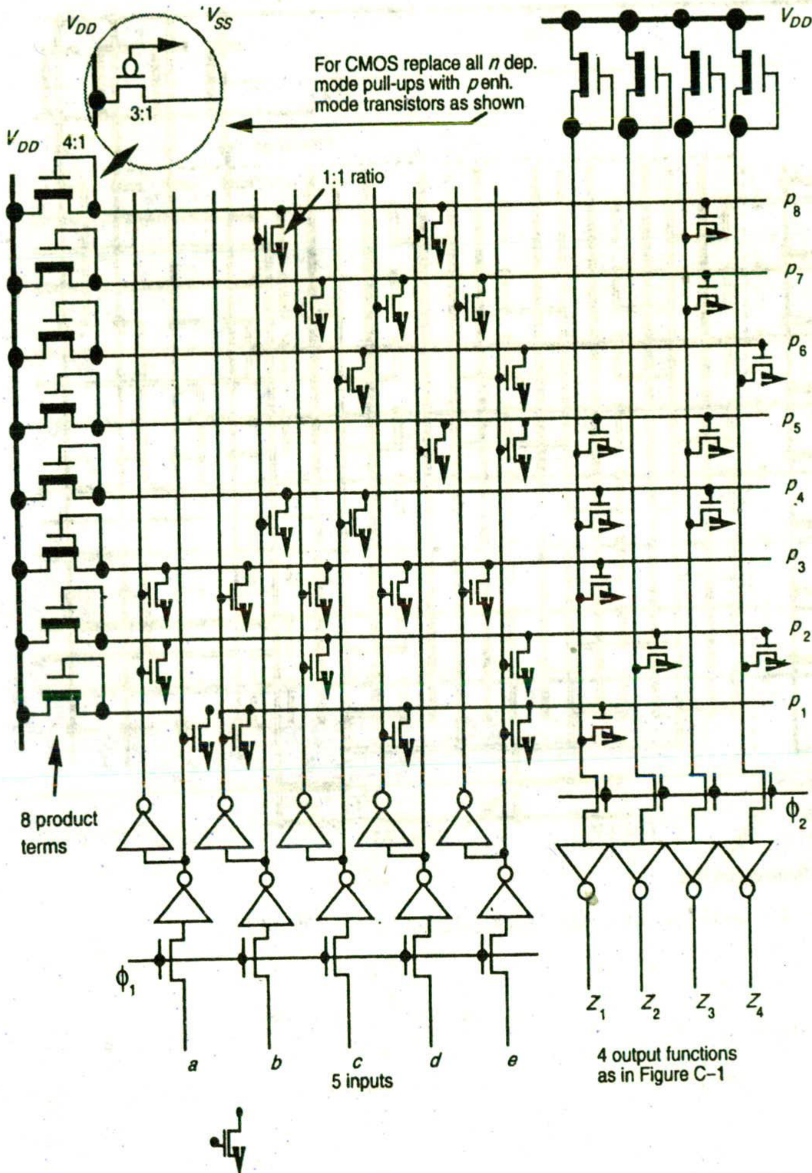


Figure C–3 PLA arrangement for multiple output function

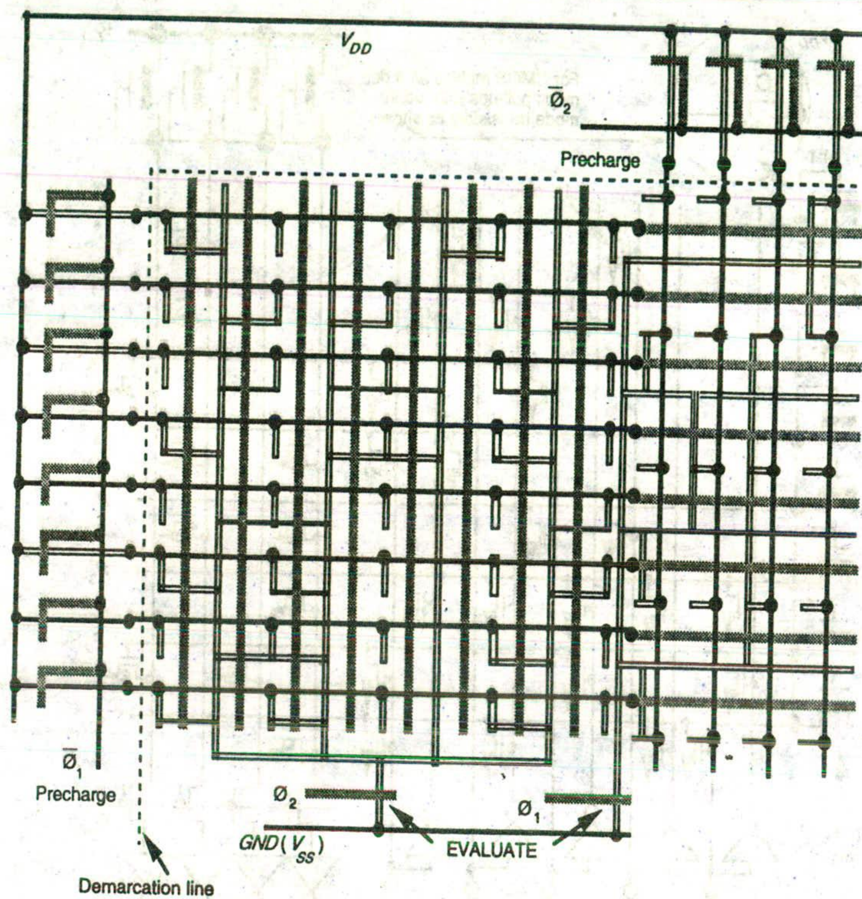


Figure C–4 CMOS (dynamic logic) stick diagram for a 4 × 8 × 4 PLA

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COLOR	STICK ENCODING	LAYERS	MASK LAYOUT ENCODING	CIF LAYER
GREEN		n-diffusion (n+ active) Thinox*	*Thinox = n-diff. + transistor channels	ND
ED		Polysilicon		NP
E		Metal 1		NM
ACK		Contact cut		NC
	NOT APPLICABLE	Overglass		NG
		Implant		NI
MOS ONLY BROWN		Buried contact		NB

FEATURE	FEATURE (STICK)	FEATURE (SYMBOL)	FEATURE (MASK)
n-type enhancement mode transistor	D L: W G S; L: W S D G	L: W S D G	(L: W = 1:1) S D G
Transistor length to width ratio L: W should be shown.			
n-type depletion mode transistor nMOS only	L: W; L: W	L: W S G D	(L: W = 1:1)
Source, drain and gate labelling will not normally be shown.			

Color plate 1(a) Encodings for a simple single metal nMOS process. (See Figure 3–1(a) for nMOS monochrome encoding details.)

COLOR	STICK ENCODING	LAYERS	MASK LAYOUT ENCODING	CIF LAYER
GREEN	Encoding as in Color plate 1(a)	n-diffusion (n^+ active) Thinox*	* Thinox = n-diff. + p-diff. + transistor channels Encoding as in Color plate 1(a)	CAA or CNA
RED		Polysilicon		CPF
BLUE		Metal 1		CMF
BLACK		Contact cut		CC
GRAY		Overglass		COG
YELLOW (STICK)	green outline here for clarity	p-diffusion (p^+ active)	p^+ mask	CAA or CPA
YELLOW	Not shown on diagram	p^+ mask	either or	CPP
DARK BLUE OR PURPLE		Metal 2		CMS
BLACK		VIA		CVA
BROWN	Demarcation line p-well edge is shown as a demarcation line in stick diagrams	p-well		CPW
BLACK	X	V_{DD} or V_{SS} contact*	V_{DD} V_{SS}	CC

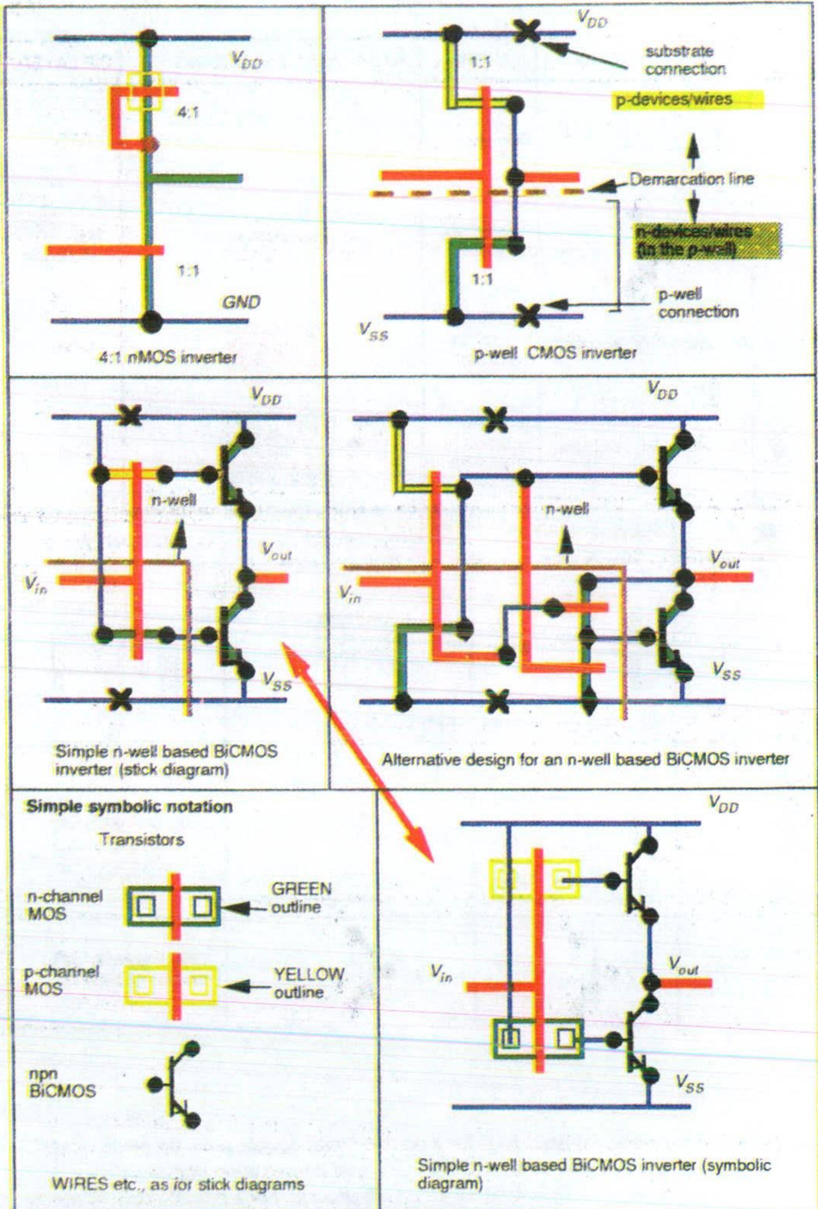
FEATURE	FEATURE (STICK)	FEATURE (SYMBOL)	FEATURE (MASK)
n-type enhancement mode transistor *(as in Color plate 1(a))*	Demarcation line L:W		
Transistor length to width ratio L:W may be shown.			
p-type enhancement mode transistor	L:W S G D Demarcation line	S G D	S D G p^+ mask
Note: p-type transistors are placed above and n-type below the demarcation line			

Color plate 1(b) Color encodings for a double metal CMOS p-well process. The same well encoding and demarcation line is used for an n-well process. For a p-well process, the n features are in the well. For an n-well process, the p features are in the well. (See Figure 3–1(b) for CMOS monochrome encoding details.)

COLOR	STICK ENCODING	LAYERS	MASK LAYOUT ENCODING	CIF LAYER
ORANGE		Polysilicon 2		CPS
		Bipolar npn transistor	See Color plate 6 also Figure 3.13(f)	Not applicable
PINK	Not separately encoded	p-base of bipolar npn transistor		CBA
PALE GREEN	Not separately encoded	Buried collector of bipolar npn transistor	n-well	CCA

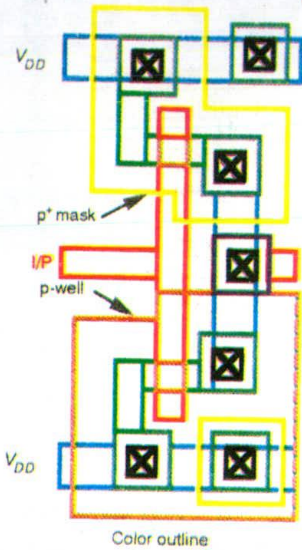
FEATURE	FEATURE (STICK)	FEATURE (SYMBOL)	FEATURE (MASK)
n-type enhancement poly. 2 transistor.	Demarcation line; L: W; S; D; G	S; D; G	S; D; G
Transistor length to width ratio L: W may be shown.			
p-type enhancement poly. 2 transistor	L: W; Demarcation line		
Note: p-type transistors are placed above and n-type below the demarcation line			
npn bipolar transistor			See Figure 3.13(f) and Color plate 6

Color plate 1(c) Additional encodings for a double metal double poly. BiCMOS n-well process. The same well encoding and demarcation line as in Figure 3–1(b) is used for an n-well process. For a p-well process, the n features are in the well. (See Color plate 9 for additional BiCMOS color encoding details and see Figure 3–1(c) for monochrome encoding details.)

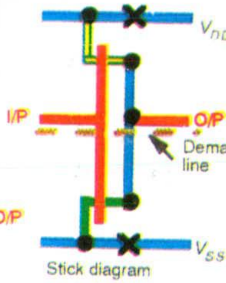


Color plate 1(d) Color stick diagram examples. (See Figure 3-1(d) Monochrome stick diagrams and simple symbolic encoding.)

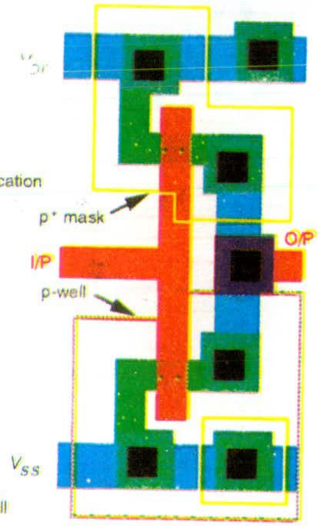
CMOS inverter I/P & O/P on polysilicon



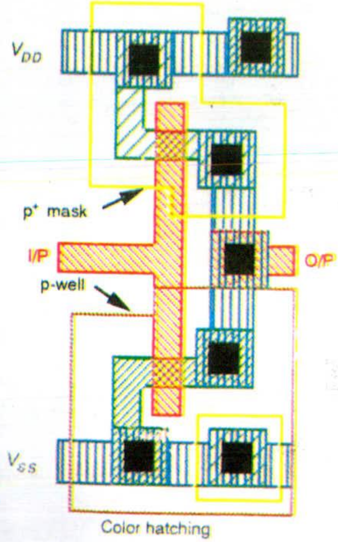
Color outline



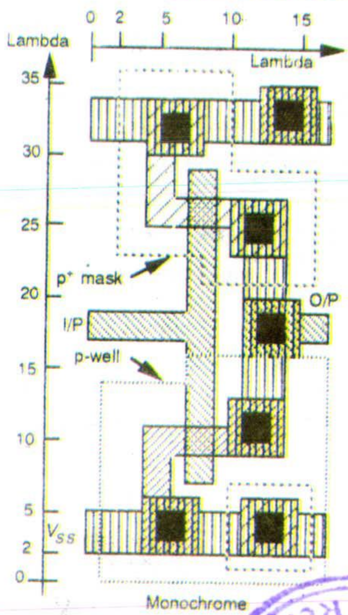
Stick diagram



Color fill



Color hatching



Monochrome

Color plate 2 Example layout encodings

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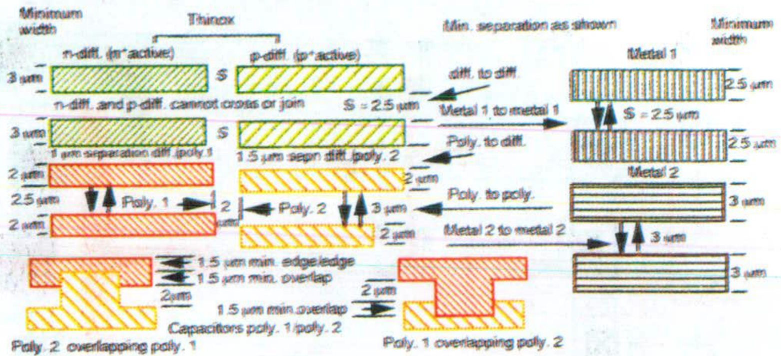
Date
Cell: 01675841692

Design rules for wires (interconnects) (ORBIT 2 µm CMOS)

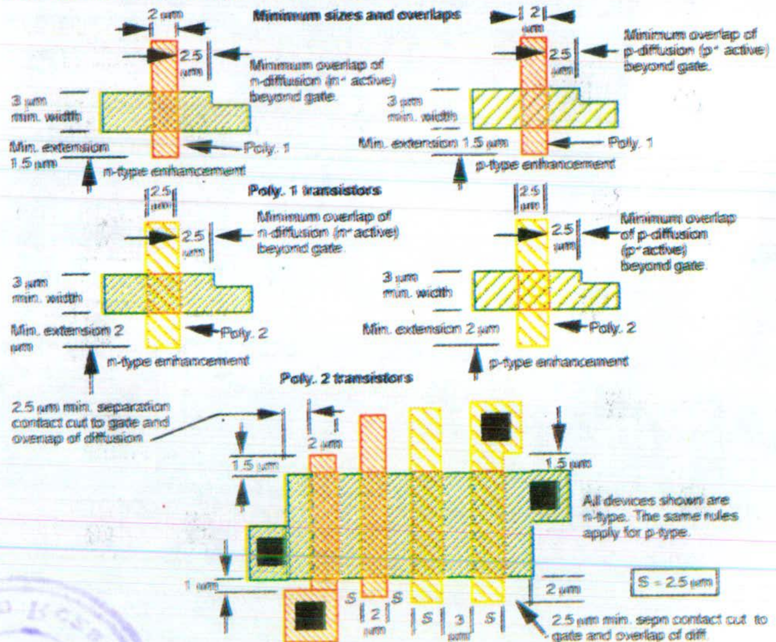


Otherwise poly. 2 must not be coincident with poly. 1

Note: Where no separation is specified, wires may overlap or cross (e.g. metal may cross any layer). For p-well CMOS, n-diff. wires can only exist inside and p-diff. wires outside p-well. For n-well CMOS, p-diff. wires can only exist inside and n-diff. wires outside n-well.

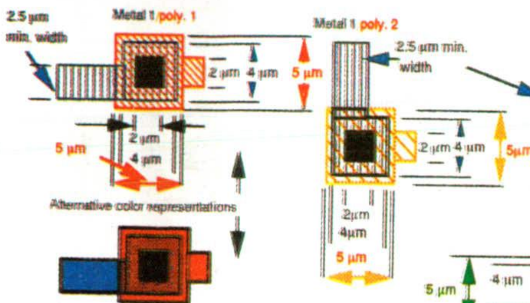
Avoid coincident edges where metal 1 and metal 2 runs follow the same path for > 25 µm length (underlap metal 1 edges by 0.8 µm).

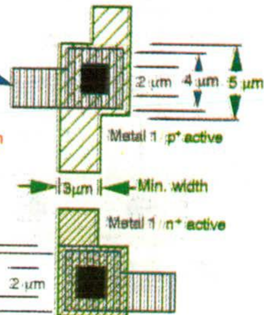
Transistor related design rules (ORBIT 2 µm CMOS)

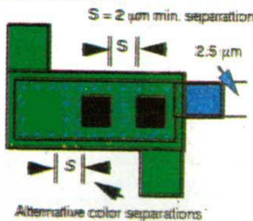


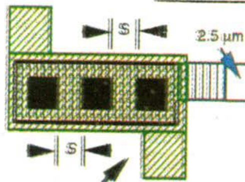
Color plate 3 ORBIT™ 2 µm design rules (a) (b)

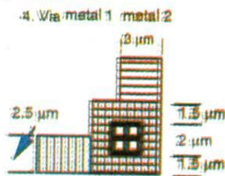
Rules for contacts and vias (ORBIT 2 µm CMOS)

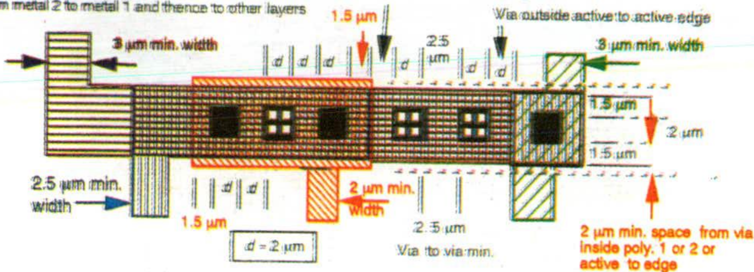








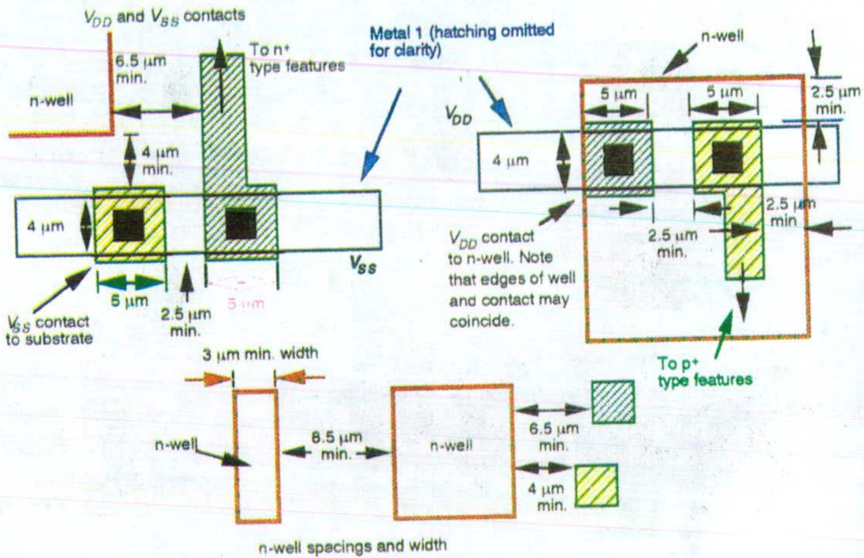




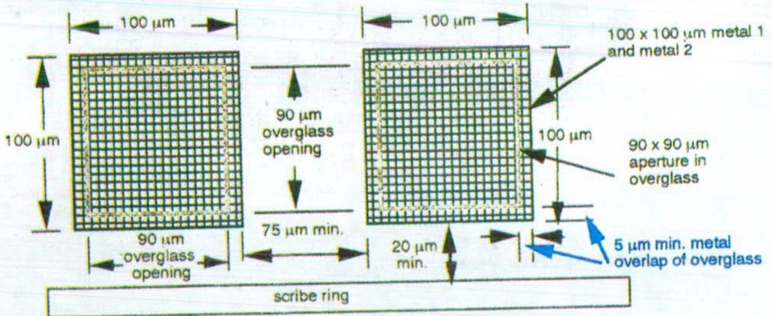
Note that vias must not be placed over contacts.

Color plate 4 ORBIT™ 2 µm design rules (c)

ules for n-well and V_{DD} and V_{SS} contacts (ORBIT 2 µm CMOS process)



Rules for pad and overglass geometry (ORBIT 2 µm CMOS)



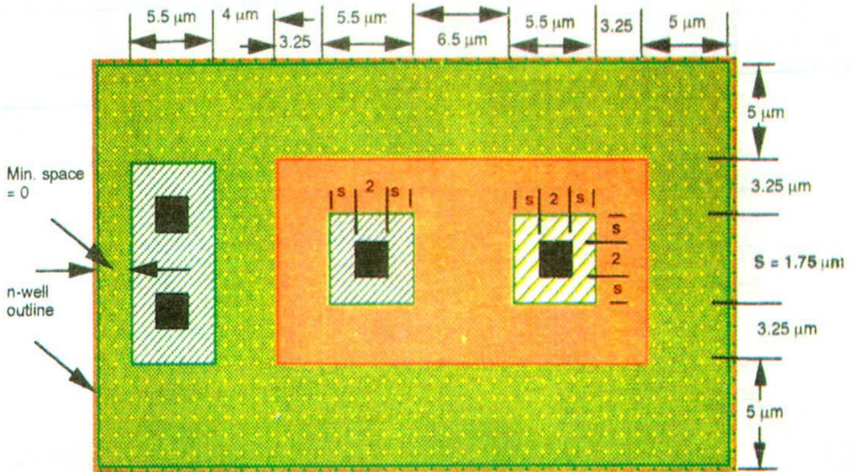
Other rules and encodings

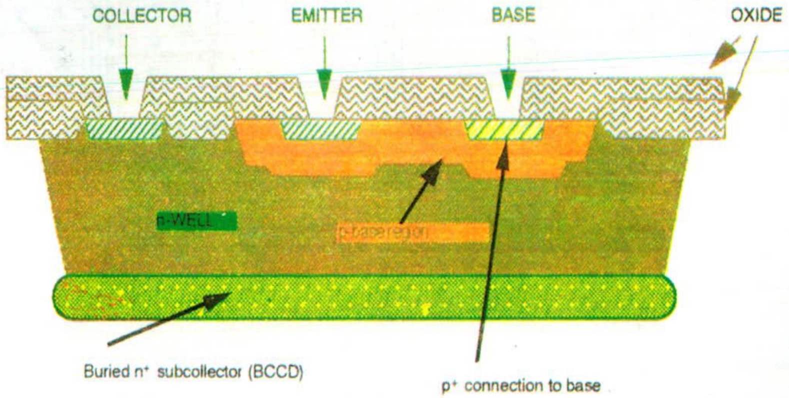
Via overlap of pad 2 µm
Pad to active separation 20 µm minimum
Color encoding for overglass mask . . . gray.

Color plate 5 ORBIT™ 2 µm design rules (d) (e)

Special rules for BiCMOS transistors (ORBIT 2 μm CMOS)

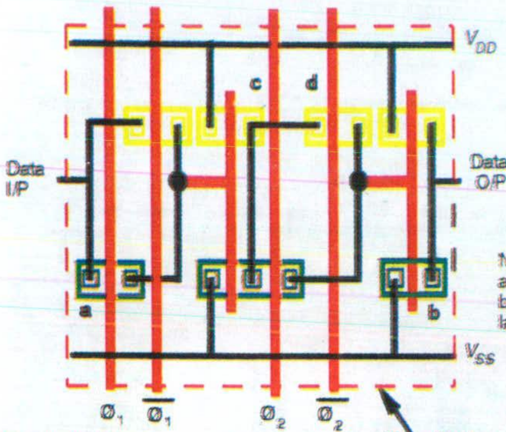
Note: For clarity, layers have not been drawn transparent. Note that BCCD underlies the entire area and the p-base underlies all within its boundary.





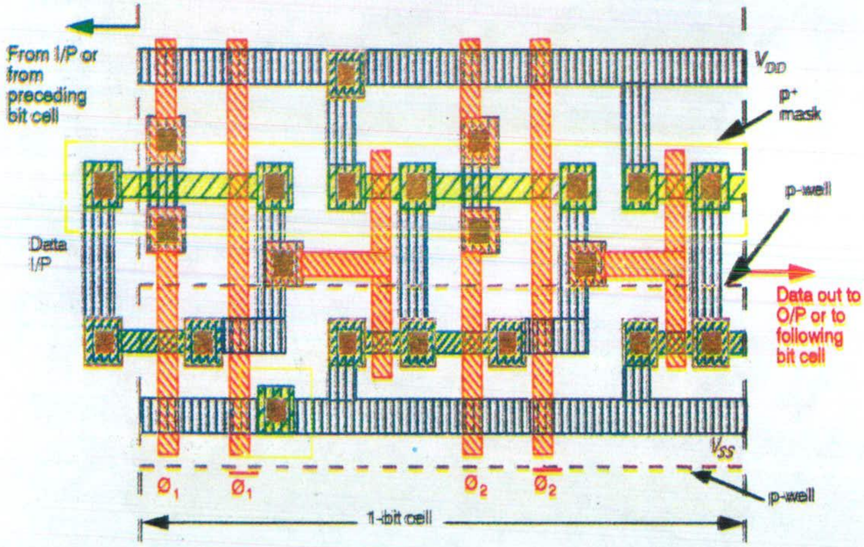
Cross-section through npn transistor (ORBIT 2 μm BiCMOS)

Color plate 6 ORBIT™ 2 μm design rules (f)



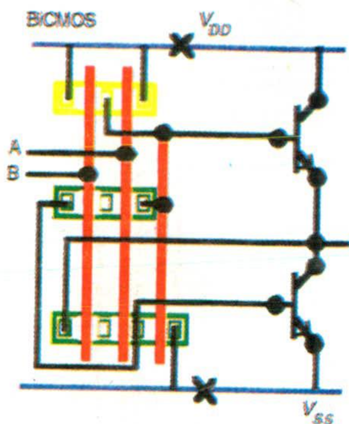
Note that the transistors a and b also c and d have been merged in the mask layout.

(a) Symbolic diagram



(b) Derived mask layout

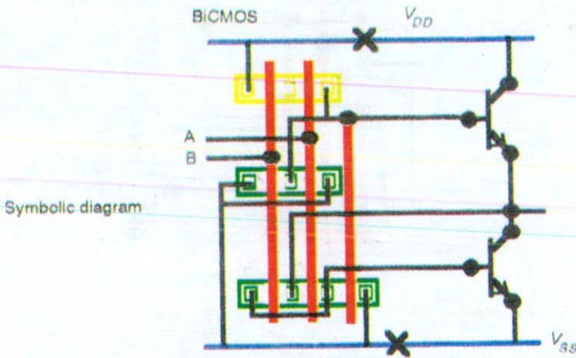
Color plate 7 1-bit CMOS shift register cell

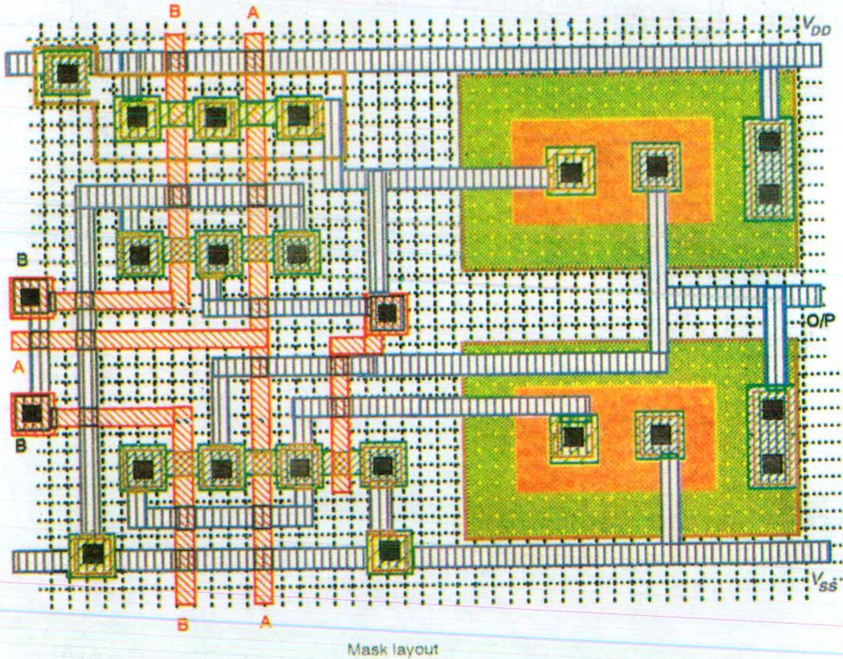


Symbolic diagram

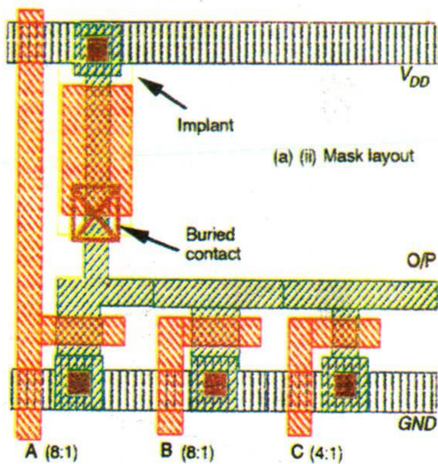
Mask layout

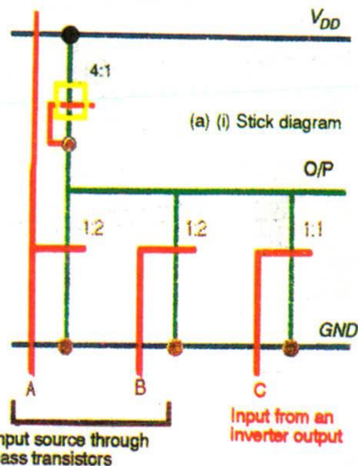
Color plate 8(a) A BiCMOS 2 input *nand* gate

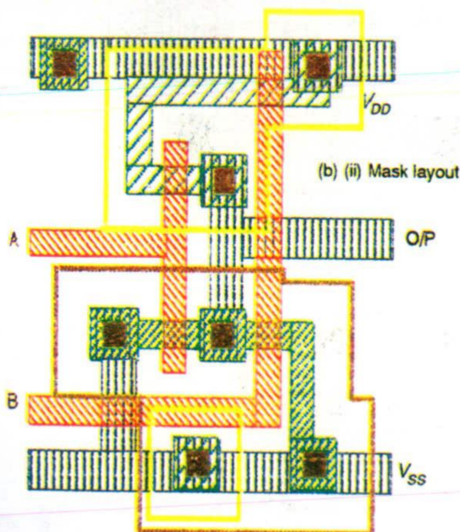


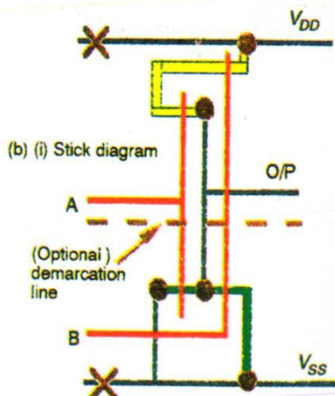


Color plate 8(b) A BiCMOS 2 input *nor* gate









Color plate 9 (a) Three input nMOS *nor* gate; (b) two input CMOS (p-well) *nor* gate

(a) Standard cell layouts

(i)

Standard cells $7\lambda \times 11\lambda$

(ii)

I_0

I_1

I_2

I_3

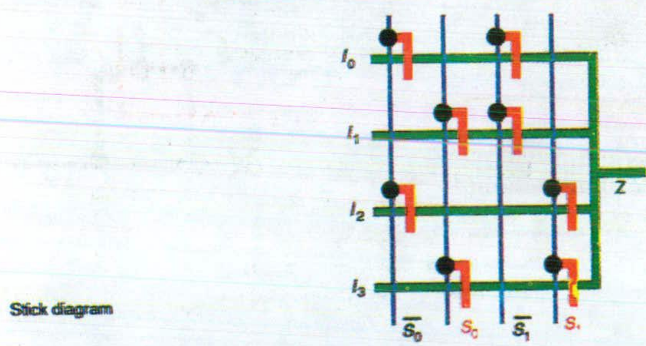
Cell outlines shown for clarity

O/P

Z

(b) Mask layout

$\overline{S_0}$ S_0 $\overline{S_1}$ S_1



Color plate 10 n-type pass transistor based 4-way MUX

V_{DD}

I_0

I_1

Mask layout

I_2

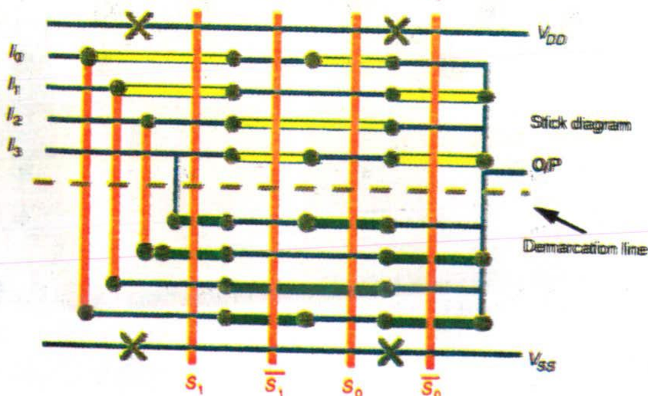
I_3

O/P

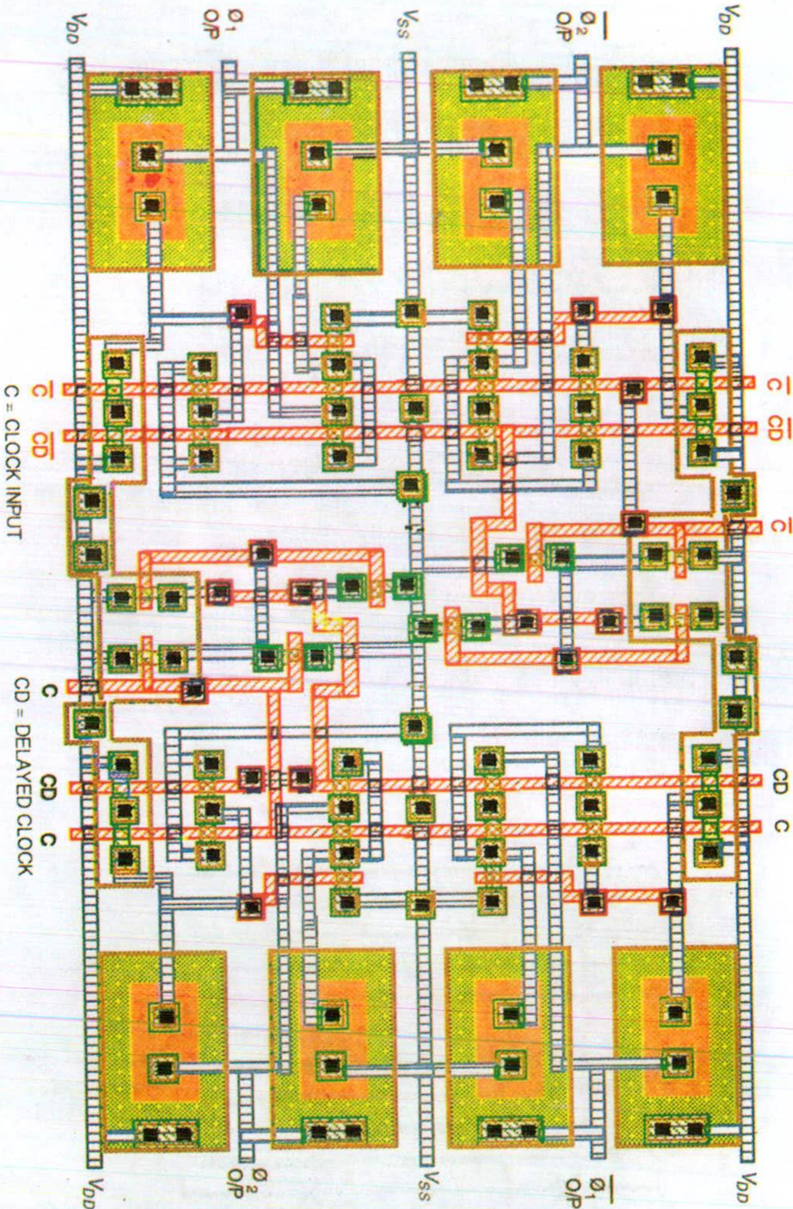
Note that the n and p switch networks are identical—each comprising 6 minimum size contact/transistor structures plus 1 long double transistor switch.

V_{SS}

S_1 $\overline{S_1}$ S_0 $\overline{S_0}$



Color plate 11 CMOS transmission gate based 4-way MUX



Color plate 12 Mask layout for two-phase (and complements) clock generator (see Figure 5–34)