Chapter 15
Operational Amplifier Frequency Response and Compensation

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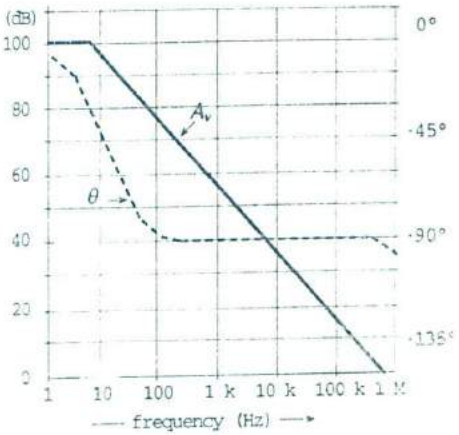


Objectives

You will be able to:

1. Show how feedback can produce instability in op-amp circuits.
2. Sketch and explain typical gain/frequency and phase/frequency response graphs for uncompensated and compensated operational amplifiers.
3. Define: loop gain, loop phase shift, phase margin.
4. Discuss compensation methods for stabilizing op-amp circuits, and calculate component values for compensating circuits.
5. Explain how the bandwidth of an op-amp circuits is affected by closed-loop gain.
6. Define: Gain-bandwidth product, slew rate, full-power bandwidth.
7. Determine the bandwidths of various op-amp circuits using: frequency response graphs, gain-bandwidth product, and slew rate.
8. Explain how stray and load capacitance can affect op-amp circuit stability, sketch appropriate compensating circuits,and calculate suitable component values.
9. List precautions that should be observed to ensure op-amp circuit stability.

Introduction

Signals applied to operational amplifiers experience phase shifts as they pass from input to output. These phase shifts are greatest at high frequencies, and at some particular frequency the total loop phase shift (from the inverting input terminal to the output and back to the input via the feedback network) can add up to 360°. When this occurs, the amplifier circuit can go into a state of unwanted oscillation. The conditions that produce oscillation are that the loop voltage gain be greater than or equal to unity when the loop phase shift approaches 360°. Measures taken to combat instability include the use of capacitors and resistors to reduce the total phase shift. Most operational amplifiers have compensating components included in the circuitry to ensure stability.

15-1 Operational Amplifier Circuit Stability

Loop Gain and Loop Phase Shift

Consider the inverting amplifier circuit and waveforms in Fig. 15-1(a). The signal voltage voltage (v_s) is amplified by a factor R_2/R_1, and phase shifted through -180°. The circuit is redrawn in Fig. 15-1(b) to illustrate the fact that the output voltage (v_o) is divided by the feedback network to produce the feedback voltage (v).

For an *ac* voltage (v) at the op-amp inverting input terminal [in Fig. 15-1(b)], the amplified output is $v_o = A_v v$, as shown. The output is divided by the feedback factor [$B = R_1/(R_1 + R_2)$], and fed back to the input. An additional -180° of phase shift can occur within the op-amp at high frequencies, and this causes v to be in-phase with v_o, as illustrated. Thus, the feed back voltage can be exactly equal to and in phase with the voltage (v) at the inverting input. In this case, the circuit is supplying its own *ac* input voltage, and a state of continuous oscillation exists.

Because of the feedback network, high-frequency oscillations can occur in many operational amplifier circuits, and when this happens the circuit is termed *unstable*. Measures taken to combat circuit instability are referred to as *frequency compensation*.

Two conditions normally have to be fulfilled for a circuit to oscillate; the *loop gain* must be equal to or greater than 1, and the *loop phase shift* should equal 360°. The loop gain is the voltage gain around the loop from the inverting input terminal to the amplifier output, and back to the input via the feedback network. The loop phase shift is the total phase shift around the loop from the inverting input terminal to the amplifier output, and back to the input via the feedback network.

The gain from the inverting input terminal to the output is the op-amp open-loop gain (A_v). For the feedback network, the gain from the amplifier output back to the input is actually an attenuation. So,

$$\text{loop gain} = (\text{amplifier gain}) \times (\text{feedback network attenuation})$$
$$= A_v B$$

Assuming that the feedback network is purely resistive, it adds nothing to the loop phase shift. The loop phase shift is essentially the amplifier phase shift. The phase shift from the inverting input terminal to the output is normally -180°. (The output goes negative when the input goes positive, and vice versa.) At high frequencies there is additional phase shift caused by circuit capacitances, and the total can approach -360°. When this occurs, the circuit is virtually certain to oscillate. Most currently-available operational amplifiers have internal *compensating components* to prevent oscillations. In some cases, compensating components must be connected externally to stabilize a circuit.

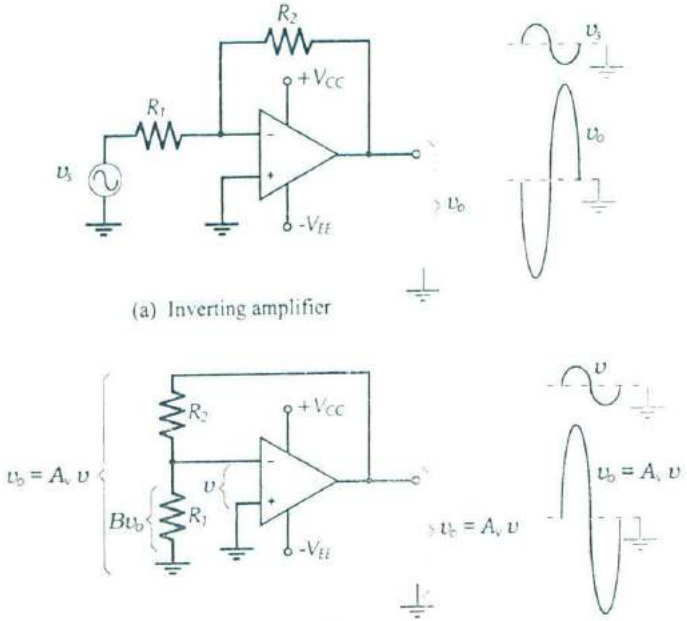


Figure 15-1
Because an inverting amplifier consists of an operational amplifier and a feedback network, the circuit can supply its own ac input (v derived from v_o), and a state of continuous oscillations can occur.

Uncompensated Gain and Phase Response

A straight-line approximation of the gain/frequency response graph for a typical operational amplifier *without any compensating components* is shown in Fig. 15-2. Note that the overall open-loop voltage gain (A_v) initially falls off (from its 100 dB level) at 6 dB/octave (-20 dB/decade) from f_{p1} (*pole frequency #1*). From f_{p2}, the rate of decline is 12 dB/octave (-40 dB/decade), and from f_{p3}, the fall-off rate of A_v is 18 dB/octave (-60 dB/decade).

The phase/frequency response graph in Fig. 15-2 shows that the phase shift (θ) is approximately -45° at f_{p1}, -135° at f_{p2}, and -225° at f_{p3}. This open-loop phase shift is in addition to the -180° phase shift that normally occurs from the op-amp inverting input terminal to the output. Thus, the total loop phase shift (θ_L) at f_{p1} is (-45° -180°) = -225°; at f_{p2}, θ_L = (-135° -180°) = -315°; and at f_{p3}, θ_L = (-225° -180°) = -405°.

As already discussed, oscillations occur when the loop gain is equals or exceeds 1 and the loop phase shift is 360°. In fact, the phase shift does not have to be exactly 360° for oscillation to occur. A phase shift of 330° at $A_v B = 1$ makes the circuit unstable. To avoid oscillations, the total loop phase shift must not be greater than 315° when $A_v B = 1$. The difference between 360° and the actual loop phase shift at $A_v B = 1$ is referred to as the *phase margin* (ϕ_m). Thus, for circuit stability, the phase margin should be a minimum of,

$$\phi_m = 360° - 315° = 45°$$

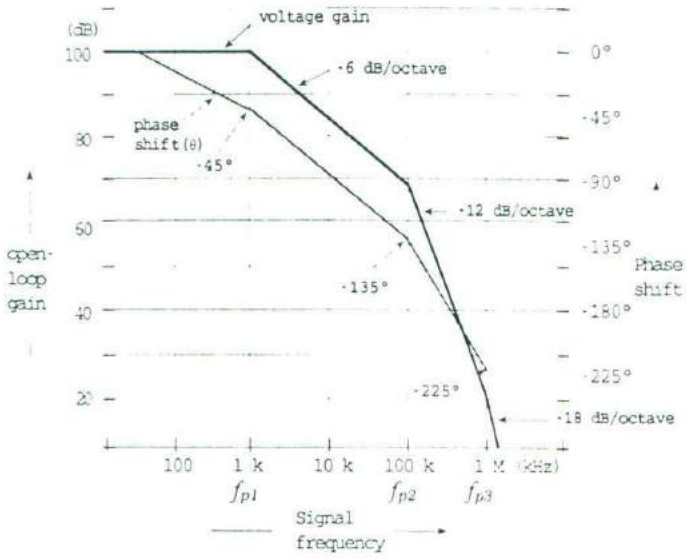


Figure 15-2
The three stages of an op-amp (internal) circuit each has its own gain/frequency response with a 6 dB/octave fall-off, and its own phase shift/ frequency response with a maximum phase shift of 90°. These responses combine to give the overall op-amp A_v/f and θ/f responses.

Compensated Op-amp Gain and Phase Response

The open-loop gain/frequency and phase/frequency responses for two internally compensated operational amplifiers are shown in Figs. 15-3 and 15-4. The *741* frequency response graphs in Fig. 15-3 shows that the gain starts at 100 dB and falls by 20 dB/decade over most of its frequency range. The phase shift remains -90° or less for most of the frequency range. The open-loop gain falls off to 1 (0 dB) at a frequency of approximately 800 kHz. The *741* is known as a general purpose operational amplifier for use in relatively low frequency applications.

The *AD843* frequency response in Fig. 15-4 shows an open-loop gain of 90 dB at low frequencies, falling off at 20 dB per decade to 34 MHz at A_v =1. Instead of the open-loop phase shift, the phase margin is plotted versus frequency. The phase margin is close to 90° over much of the frequency range, starts to become smaller around 3.4 MHz, and falls to approximately 40° at f = 34 MHz.

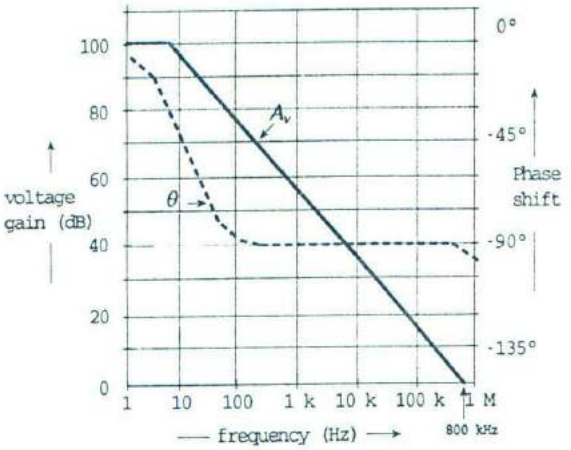


Figure 15-3
Approximate gain/frequency and phase/frequency responses for a 741 op-amp.

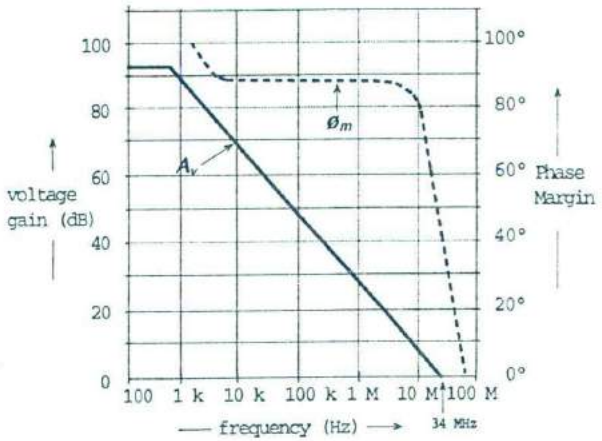


Figure 15-4
Approximate gain/frequency and phase-margin/frequency response for an AD843 op-amp.

Amplifier Stability and Gain

From Eq. 13-3, the overall voltage gain of an amplifier with negative feedback is,

$$A_{CL} \approx \frac{1}{B}$$

and the loop gain is, $$A_v B \approx \frac{A_v}{A_{CL}}$$

So, the loop gain ($A_v B$) equals 1 when

$$A_{CL} \approx A_v$$

This is one of the conditions required for circuit oscillation. To determine if oscillation will occur in a given circuit, it is necessary to first find the frequency at which $A_{CL} \approx A_v$, then determine the op-amp phase margin at that frequency.

Example 15-1

The inverting amplifier in Fig. 15-5 is to be investigated for stability. Determine the frequency at which the loop gain equals 1 and estimate the phase margin if the operational amplifier is: (a) one with the gain/frequency characteristics in Fig. 15-2, (b) a *741*, (c) an *AD843*.

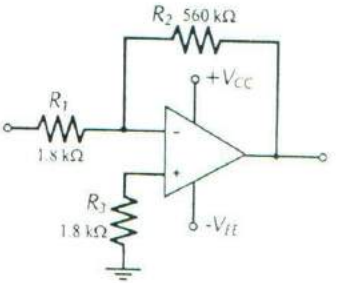


Figure 15-5
Inverting amplifier circuit for Example 15-1.

Solution

(a) Refer to the A_v/f and θ/f graphs reproduced in Fig. 15-6 (from Fig. 15-2).

$$A_{CL} = \frac{R_2}{R_1} = \frac{560\ \text{k}\Omega}{1.8\ \text{k}\Omega}$$
$$= 311$$

or,
$$A_{CL} = 20 \log 311$$
$$\approx 50\ \text{dB}$$

Draw a horizontal line on the frequency response graph at $A_v = A_{CL} = 50$ dB. (Fig. 15-6). Draw a vertical line where the horizontal line intersects the A_v/f graph. The frequency at this point is identified as f_2.

$$f_2 \approx 150\ \text{kHz (logarithmic scale)}$$

From the θ/f graph, the op-amp phase shift at f_2 is,

$$\theta \approx -165^\circ$$

The loop phase shift is,

$$\phi_l = \theta - 180^\circ = -165^\circ - 180^\circ$$
$$= -345^\circ$$

and,
$$\phi_m = 360^\circ - \phi_l = 360^\circ - 345^\circ$$
$$= 15^\circ$$

Because the phase margin is less than 45°, the circuit is likely to be unstable.

(b) For a *741*

A horizontal line at 50 dB on the frequency response in Fig. 15-3 gives,

$$f_2 \approx 1.5\ \text{kHz and } \theta \approx -90^\circ$$
$$\phi_l = -90^\circ - 180^\circ$$
$$= -270^\circ$$

and,
$$\phi_m = 360^\circ - 270^\circ$$
$$= 90^\circ \quad \text{(stable circuit)}$$

(c) For an *AD843*

A horizontal line at 50 dB on the frequency response in Fig. 15-4 gives,

$$f_2 \approx 90\ \text{kHz}$$

and,
$$\phi_m \approx 90^\circ \quad \text{(stable circuit)}$$

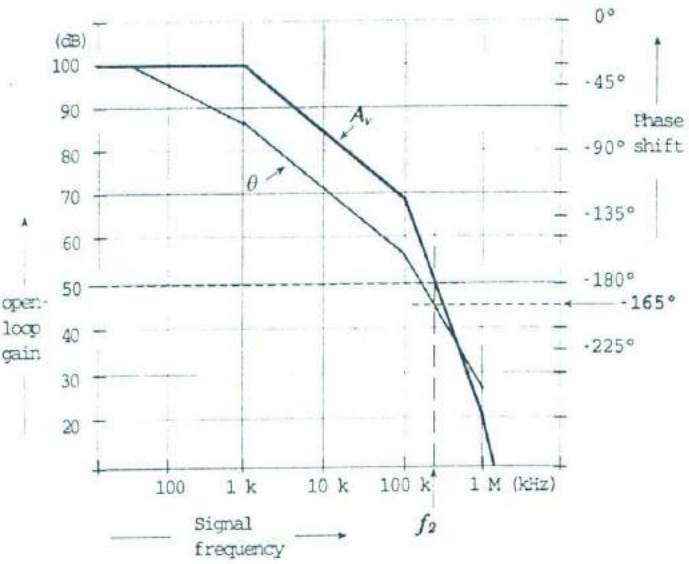


Figure 15-6
A_v/f and θ/f characteristics for the op-amp in Ex. 15-1(a).

A circuit with the frequency response in Fig. 15-6 and with A_{CL} = 50 dB was shown to be unstable. If the amplifier had A_{CL} = 70 dB, reconsideration shows that it is stable. That is, an amplifier with a high closed-loop gain is more likely to be stable than one with the lower gain. Low gain amplifiers are more difficult to stabilize than high gain circuits. The voltage follower (with a closed-loop gain of 1) can be one of the most difficult circuits to stabilize.

Some internally compensated op-amps are specified as being stable to closed-loop gains as low as 5. In this case, external compensating components must be used with lower gain circuits.

Practise Problems

15-1.1 Investigate the stability of an inverting amplifier with a closed-loop gain of 60 dB if the operational amplifier is; (a) one with the gain/frequency characteristics in Fig. 15-2, (b) a *741*, (c) a *AD843*.

15-2 Frequency Compensation Methods

Phase-Lag and Phase-Lead Compensation

Lag compensation and *lead compensation* are two methods often employed to stabilize op-amp circuits. The phase-lag network in Fig. 15-7(a) introduces additional phase lag at some low frequency where the op-amp phase shift is still so small that additional phase lag has no effect. It can be shown that at frequencies where $X_{C1} >> R_2$, the voltage v_2 lags v_1 by as much as 90°. At higher frequencies where $X_{C1} << R_2$ no significant phase lag occurs, and

the lag network merely introduces some attenuation. The effect of this attenuation is that the A_v/f graph is moved to the left, as illustrated in Fig. 15-7(b). Thus, the frequency (f_{x1}) at which $A_vB = 1$ [for a given closed-loop gain (A_{CL})] is moved to a lower frequency (f_{x2}), as shown. Because f_{x2} is less than f_{x1}, the phase shift at f_{x2} is less than that at f_{x1}, and the circuit is likely to be stable.

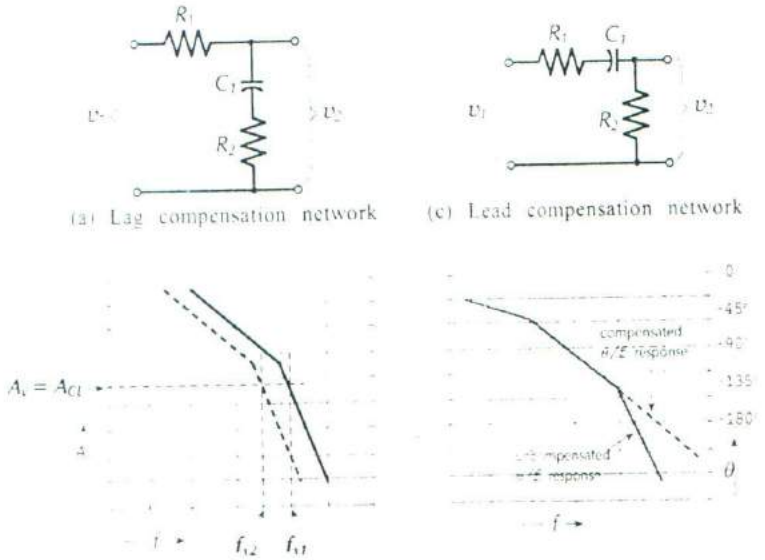


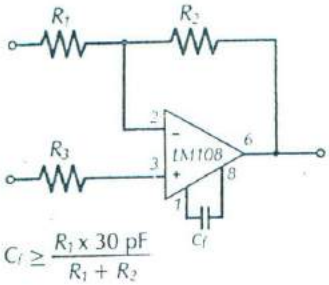
Figure 15-7
A phase-lag network reduces an amplifier open-loop gain, so that the phase shift where $A_vB = 1$ is too small for instability. A phase-lead network cancels phase lag.

The network in Fig 15-7(c) introduces a phase lead. In this network, when $X_{C1} >> R_1$, the voltage v_2 leads v_1. This phase lead cancels some of the unwanted phase lag in the operational amplifier θ/f graph, [see Fig. 15-7(d)], thus rendering the circuit more stable. Phase-lag and phase-lead networks are both used internally to compensate op-amp circuits. Both types of circuit can also be used externally.

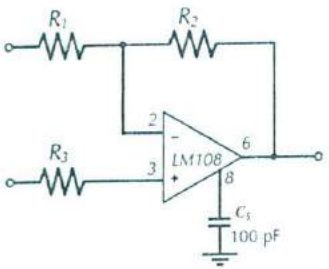
Manufacturer's Recommended Compensation

Most currently-available operational amplifiers contain internal compensating components, and do not require additional external components. Some have internal compensating resistors, and need only a capacitor connected externally to complete a compensating network. For those that require compensation, *IC* manufacturers list recommended component values and connection methods on the op-amp data sheet. An example of this is illustrated in Fig. 15-8 for the *LM108*.

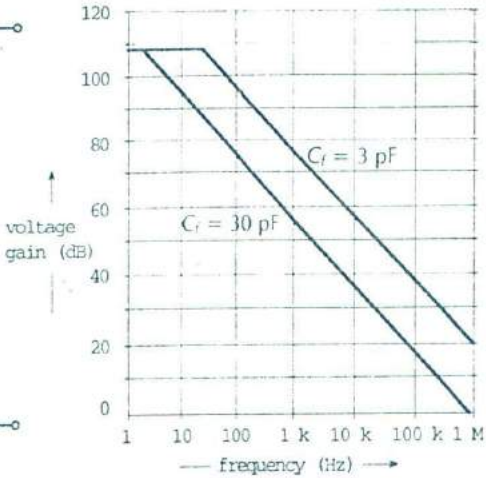
When selecting standard value compensating capacitors the next larger values should be used. This is termed *over-compensation* and it results in better amplifier stability, but it also produces a smaller circuit bandwidth.



(a) Phase lag compensation



(b) Alternate phase lag compensation



(c) Approximate gain/frequency response

Figure 15-8
Manufacturer's recommended compensation methods and gain/frequency response for the LM108 op-amp. (reproduced with permission of National Semiconductor Corp.)

Example 15-2

The inverting amplifier in Fig. 15-9 is required to amplify a 200 mV input by a factor of 4.5. Determine suitable component values.

Solution

Because the *LM108* has a very low input bias current (see Appendix 1-14), it should be treated as a *BIFET* op-amp.

Select $R_2 = 1\ M\Omega$

$$R_1 = \frac{R_2}{A_{CL}} = \frac{1\ M\Omega}{4.5}$$

$= 222\ k\Omega$ (use 220 kΩ standard value)

$R_3 = R_1 \| R_2 = 220\ k\Omega \| 1\ M\Omega$

$= 180\ k\Omega$ (standard value)

From Fig. 15-8, $$C_f = \frac{R_1 \times 30\ pF}{R_1 + R_2} = \frac{220\ k\Omega \times 30\ pF}{220\ k\Omega + 1\ M\Omega}$$

$= 5.4\ pF$ (use 10 pF standard value for over-compensation)

Connect C_f between terminals 1 and 8, as shown in Fig. 15-9.

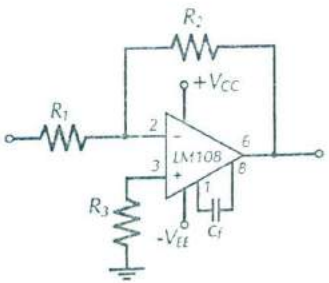


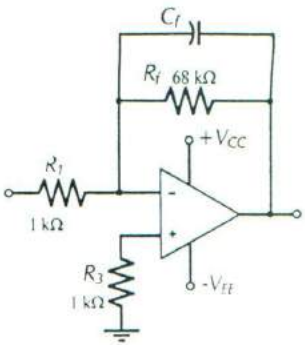
Figure 15-9
Op-amp circuit for Ex. 15-2.

Miller-Effect Compensation

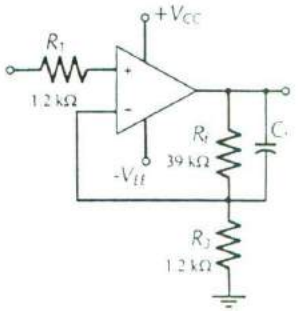
Miller effect (discussed in Section 8-3) involves connecting a capacitor between the output and input terminals of an inverting amplifier. Miller-effect compensation of an op-amp circuit is very simple, and it is often the only external method available for stabilizing a circuit where the op-amp is internally compensated. A capacitor (C_f) is connected across the feedback resistor, as shown in Fig. 15-10(a) and (b). The capacitor value is calculated to have an impedance equal the feedback resistor value at the desired signal cutoff frequency (f_2).

$$X_{Cf} = R_f \text{ at } f_2 \qquad \textbf{(15-1)}$$

This reduces the closed-loop by 3 dB at the selected frequency. So long as the op-amp is stable at this frequency, the circuit will not oscillate. The op-amp used should have an upper cutoff frequency much higher than f_2.



(a) Inverting amplifier with Miller-effect compensation



(b) Noninverting amplifier with Miller-effect compensation

Figure 15-10
Miller-effect frequency compensation for amplifier circuits.

Example 15-3

Calculate a suitable Miller-effect capacitor to stabilize the circuit in Fig. 15-10(a) at f_2 = 35 kHz.

Solution

From Eq. 15-1, $$C_f = \frac{1}{2\pi f_2 R} = \frac{1}{2\pi \times 35\text{ kHz} \times 68\text{ k}\Omega}$$

$$\approx 67\text{ pF (use 68 pF standard value)}$$

Practise Problems

15-2.1 The components of the lag and lead compensation network in Fig. 15-7 are: R_1 = 6.8 kΩ, R_2 = 390 Ω, and C_1 = 500 pF. Calculate the approximately phase lag and phase lead at a frequency of 50 kHz.

15-2.2 Calculate a suitable Miller-effect capacitor to stabilize the circuit in Fig. 15-10(b) at f_2 = 50 kHz.

15-3 Op-amp Circuit Bandwidth and Slew Rate

Low Cutoff Frequency

Operational amplifiers are direct-coupled internally, so where they are employed in direct-coupled applications, the circuit lower cutoff frequency (f_1) is zero. In capacitor-coupled circuits, the lower cutoff frequency is determined by the selection of coupling capacitors. The circuit high cutoff frequency (f_2) is, of course, dependent on the frequency response of the operational amplifier.

High Cutoff Frequency

In Section 13-7 it is shown that for a negative feedback amplifier,

the high cutoff frequency occurs when the amplifier open-loop gain approximately equals the circuit closed-loop gain:

Eq. 13-26. $A_v \approx A_{CL}$

So, the circuit high cutoff frequency (f_2) can be found simply by drawing a horizontal line at $A_v \approx A_{CL}$ on the op-amp open-loop gain/ frequency response graph. Because the op-amp low cutoff frequency is zero (as explained above), The circuit bandwidth is,

$$BW = f_2 - f_1$$
$$= f_2$$

Consequently, the op-amp high cutoff frequency is often referred to as the circuit bandwidth.

The frequency response graphs published on manufacturer's data sheets are typical for each particular type of operational amplifier. Like all typical device characteristics, the precise frequency response differs from one op-amp to another. All frequencies derived from the response graphs should be taken as typical quantities. The process of determining circuit cutoff frequency from the op-amp frequency response graph is demonstrated in Example 15-4.

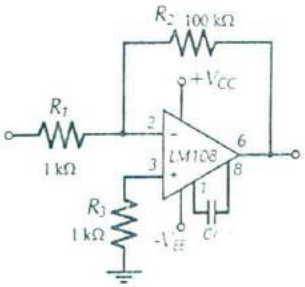


Figure 15-11
Amplifier circuit for Example 15-4.

Example 15-4

Determine the typical upper cutoff frequency for the inverting amplifier in Fig. 15-11 when the compensating capacitor (C_f) value is; (a) 30 pF, (b) 3 pF. The A_v/f graph for the *LM108* is shown in Fig. 15-12.

Solution

$$A_{CL} = \frac{R_2}{R_1} = \frac{100\ \text{k}\Omega}{1\ \text{k}\Omega}$$

$$= 100 = 40\ \text{dB}$$

f_2 occurs at $A_v = A_{CL} = 40$ dB

(a) For $C_f = 30$ pF:
Draw a horizontal line on the A_v/f graph at $A_v = 40$ dB. Where the line cuts the A_v/f characteristic for $C_f = 30$ pF read,

$$f_2 \approx 8\ \text{kHz}$$

(b) For $C_f = 3$ pF:
Where the $A_v = 40$ dB line cuts the A_v/f characteristic for $C_f = 3$ pF read,

$$f_2 \approx 80\ \text{kHz}$$

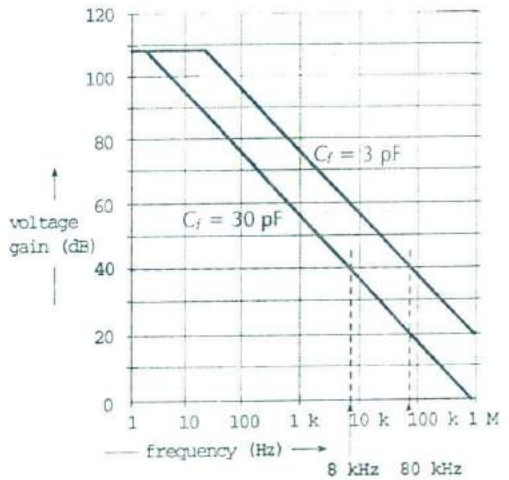


Figure 15-12
Straight line approximation of LM108 gain/frequency response.

Gain-Bandwidth Product

The *gain-bandwidth produce* (*GBW*), or *unity-gain bandwidth*, of an operational amplifier is the open-loop gain at a given frequency multiplied by the frequency. Referring to the A_v/f response for the *741* reproduced in Fig. 15-13, it is seen that at $A_{v(a)} = 10^4$, the frequency is $f_{(a)} \approx 80$ Hz. Thus,

$$GBW = A_{v(a)} \times f_{(a)} = 10^4 \times 80 \text{ Hz}$$
$$= 8 \times 10^5$$

Similarly, at $A_{v(b)} = 10$, $f_{(b)} \approx 80$ kHz, again giving $GBW = 8 \times 10^5$. Also, at $A_{v(c)} = 1$, $f_{(c)} \approx 800$ kHz, once more giving $GBW = 8 \times 10^5$. This last determination explains the term *unity-gain bandwidth*, because the *GBW* is simply equal to the frequency at which $A_v = 1$.

Because the high cutoff frequency for an op-amp circuit occurs when the closed-loop gain equals the open-loop gain, the circuit upper cutoff frequency can be calculated by dividing the gain-bandwidth product by the closed-loop gain:

$$f_2 = \frac{GBW}{A_{CL}} \qquad \textbf{(15-2)}$$

It is important to note that Eq. 15-2 applies only to operational amplifiers that have a gain/frequency response that falls off to the unity-gain frequency at 20 dB/decade. Where the A_v/f response falls off at some other rate, Eq. 15-2 cannot be used.

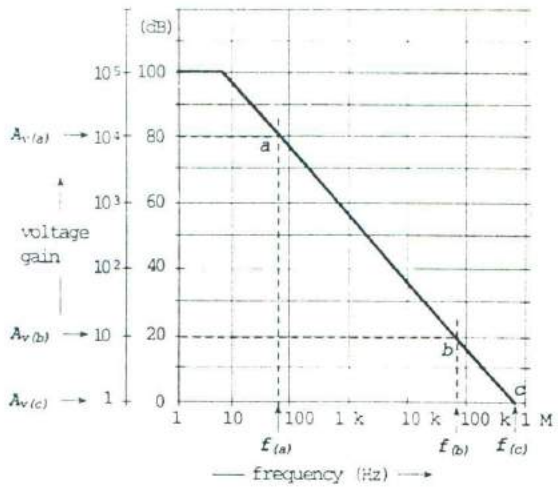


Figure 15-13
The gain-bandwidth product (GBW) for an operational amplifier can be used to determine the cutoff frequency for any given closed-loop gain.

Example 15-5

Using the gain-bandwidth product, determine the cutoff frequencies for the circuit in Ex. 15-4 (reproduced in Fig. 15-14), when the compensating capacitor is (a) $C_f = 30$ pF, (b) $C_f = 3$ pF.

Solution

(a) For C_f = 30 pF:

Referring to the *LM108* A_v/f graph for C_f = 30 pF in Fig. 15-12,

$$GBW = f \text{ at } A_v = 1$$
$$\approx 800 \text{ kHz}$$

Eq. 15-2,
$$f_2 = \frac{GBW}{A_{CL}} = \frac{800 \text{ kHz}}{100}$$
$$= 8 \text{ kHz}$$

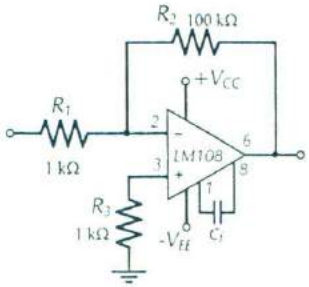


Figure 15-14
Amplifier circuit for Example 15-5.

(b) For C_f = 3 pF:

Referring to the *LM108* A_v/f graph for C_f = 3 pF in Fig. 15-12,

at A_v = 20 dB = 10, $f \approx$ 800 kHz

$$GBW = f \times A_v = 800 \text{ kHz} \times 10$$
$$= 8 \text{ MHz}$$

Eq. 15-2,
$$f_2 = \frac{GBW}{A_{CL}} = \frac{8 \text{ MHz}}{100}$$
$$= 80 \text{ kHz}$$

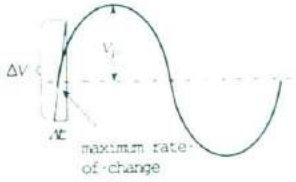
Full-Power BW and Slew Rate

The A_v/f response graphs, upper cutoff frequencies, and *GBW* specified on op-amp data sheets normally refer to the operational amplifier performance as a small-signal amplifier. In this case, the measurements are usually made *for output amplitudes not exceeding 100 mV peak-to-peak.* Where an amplifier circuit has to produce a large output voltage, the op-amp *full-power bandwidth* (f_p) must be used. The *AD843* operational amplifier, for example, is specified as having a typical unity gain bandwidth of 34 MHz for an output amplitude of 90 mV p-to-p, and a typical full power bandwidth of 3.9 MHz when the output amplitude is 20 V p-to-p.

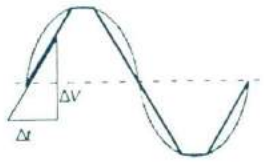
The op-amp slew rate (*SR*) (see Section 14-9) can be used to calculate the full-power bandwidth for a given output amplitude. For a sinusoidal voltage waveform, the fastest rate-of-change of voltage occurs at the point where the waveform crosses from its negative half-cycle to its positive half-cycle, and vice versa. This is illustrated in Fig. 15-15(a). It can be shown that the voltage rate-of-change at this point is,

$$\Delta V/\Delta t = 2\pi f V_p \text{ (volts/second)}$$

The maximum rate-of-change of the waveform is limited by the maximum slew rate of the op-amp used. Where the waveform amplitude or frequency is higher than the limits imposed by the slew rate, distortion will occur as illustrated in Fig. 15-15(b).



(a) Sine wave maximum rate-of-change



(b) Sine wave distortion caused by the slew rate

Figure 15-15
The op-amp slew-rate limits the upper cutoff frequency of an op-amp circuit, and limits the output amplitude at a given frequency.

The *SR* can be equated to the sine wave rate-of-change,

$$SR = 2\pi f_p V_p \qquad (15\text{-}3)$$

where f_p is the slew-rate limited frequency, or full-power bandwidth, and V_p is the peak level of the circuit output voltage. Equation 15-3 can be used to determine the full-power bandwidth of an op-amp circuit for a given output voltage amplitude. Sometimes Eq. 15-3 gives an f_p value greater than that determined from the A_v/f graph or the *GBW* product. In these cases, the circuit bandwidth is still dictated by the A_v/f graph or the *GBW* product.

Example 15-6

(a) Calculate the full-power bandwidth for an *AD843* op-amp circuit (Fig. 15-16), given a 1 V peak input and op-amp slew rate of 250 V/μs.

(b) Determine the maximum peak output voltage obtainable from a *741* op-amp circuit with a 100 kHz signal frequency. (*SR* = 0.5 V/μs for a 741.)

Solution

(a) For the *AD843:*

$$V_{o(p)} = \frac{R_2 + R_3}{R_3} \times V_{i(p)} = \frac{39\ \text{k}\Omega + 4.7\ \text{k}\Omega}{4.7\ \text{k}\Omega} \times 1\ \text{V}$$

$$= 9.3\ \text{V}$$

From Eq. 15-3,

$$f_p = \frac{SR}{2\pi V_p} = \frac{250\ \text{V}/\mu\text{s}}{2\pi \times 9.3\ \text{V}}$$

$$\approx 4.2\ \text{MHz}$$

(b) For a *741:*

From Eq. 15-3,

$$V_p = \frac{SR}{2\pi f_p} = \frac{0.5\ \text{V}/\mu\text{s}}{2\pi \times 100\ \text{kHz}}$$

$$= 0.79\ \text{V}$$

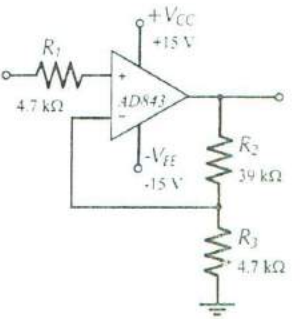


Figure 15-16
Amplifier circuit for Example 15-6.

Practise Problems

15-3.1 Determine the typical upper cutoff frequency for an inverting amplifier with a closed-loop gain of 15 using a *741* op-amp. The A_v/f graph for the *741* is shown in Fig. 15-13.

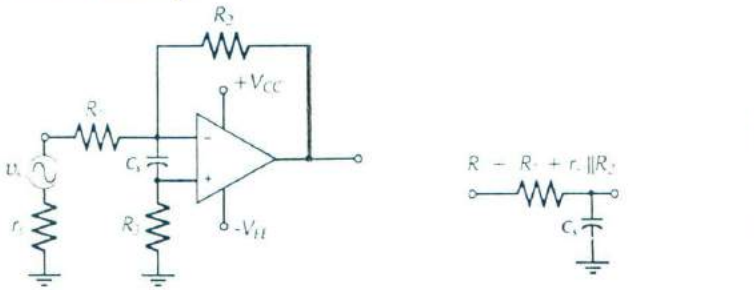
15-3.2 Using the gain-bandwidth product, calculate the cutoff frequencies for an inverting amplifier with a closed-loop gain of 30 when the op-amp used is (a) *741*, (b) an *AD843*.

15-3.3 Calculate the full-power bandwidth for an *LF353* op-amp circuit, with a 14 V peak-to-peak output voltage.

15-4 Stray Capacitance Effects

Stray capacitance (C_s) at the input terminals of an operational amplifier effectively introduces an additional phase-lag network in

the feedback loop, (see Fig. 15-17), thus making the op-amp circuit unstable. Stray capacitance problems can be avoided by good circuit construction techniques that keep the stray to a minimum. The effects of stray capacitance also depend upon the resistor values used in the feedback network. High resistance values make it easier for small stray capacitances to produce phase lag. With low-resistances, small stray capacitances normally have little effect on the circuit stability.



(a) Stray capacitance (C_s) at amplifier input (b) C_s and its series resistance

Figure 15-17
Stray capacitance can cause instability in an op-amp circuit by introducing additional phase-lag in the feedback network.

Analysis of an *RC* phase lag circuit shows that the capacitor voltage lags the input voltage by 45° when the capacitor impedance (X_c) equal the series resistance (R). Also, when $X_c = 10\ R$, the phase lag is approximately 10°, and it is this 10° of additional phase lag that might make the circuit oscillate if its phase margin is already close to the minimum for stability. If the phase margin is known to be large at the frequency where $A_v B = A_{CL}$ (the frequency at which the circuit is likely to oscillate), the stray capacitance might be unimportant. Where the phase margin is small, for circuit stability the op-amp input stray capacitance should normally be much less than,

$$C_s = \frac{1}{2\pi f(10R)} \qquad (15\text{-}4)$$

where R is the equivalent resistance in series with the stray capacitance. In Fig. 15-17, $R = R_3 + (R_1 + r_s)\|R_2$.

From Eq. 15-4 it is seen that (as already mentioned) the larger resistor values the smaller the stray capacitance that can produce circuit instability. If the signal source is disconnected from the circuit, R becomes equal to $(R_2 + R_3)$, which is much larger than $[R_3 + (r_s + R_1)\|R_2]$. In this situation, extremely small stray capacitance values can make the circuit unstable.

Miller-effect compensation can be used to compensate for stray capacitance at an op-amp input, as shown in Fig. 15-18. To eliminate the phase shift introduced by the stray capacitance the division of the output voltage produced by C_S and C_2 in series should be equal to the division produced by R_1 and R_2. Therefore,

$$\frac{X_{CS}}{X_{C2}} = \frac{R_1}{R_2}$$

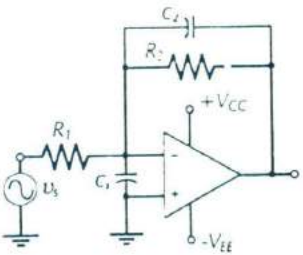


Figure 15-18
Use of Miller-effect compensation for stray capacitance at the input terminals of an op-amp.

This gives, $$C_2 R_2 = C_S R_1 \qquad (15\text{-}5)$$

Note that Eq. 15-5 does not allow for r_s or R_3 in Fig. 15-17. Where r_s is not very much smaller than R_1, it must be added to R_1. Also, resistor R_3 could be bypassed with another capacitor to reduce the total series resistance.

Example 15-7

Calculate the op-amp input terminal stray capacitance that might cause instability in the circuit of Fig. 15-19 if the amplifier cutoff frequency is 800 kHz. Also, determine a suitable Miller-effect compensating capacitor value.

Solution

Stray capacitance:

Eq. 15-4, $$C_s = \frac{1}{2\pi f \times 10[(r_s + R_1)\|R_2]}$$

$$= \frac{1}{2\pi \times 800\ \text{kHz} \times 10\ [(600\ \Omega + 1\ \text{k}\Omega)\|10\ \text{k}\Omega]}$$

$$= 14.4\ \text{pF}$$

Compensation:

Eq. 15-5, $$C_2 = \frac{C_s(r_s + R_1)}{R_2} = \frac{14.4\ \text{pF} \times (600\ \Omega + 1\ \text{k}\Omega)}{10\ \text{k}\Omega}$$

$$= 2.3\ \text{pF}$$

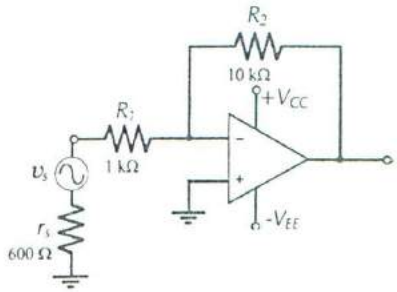


Figure 15-19
Op-amp amplifier circuit for Example 15-7.

Practise Problems

15-4.1 Determine the op-amp input stray capacitance that might cause instability in an inverting amplifier with $R_1 = 1.8\ \text{k}\Omega$, $R_2 = 560\ \text{k}\Omega$, and $f_2 = 600$ kHz; (a) when the signal source is open-circuited, (b) when $r_s = 600\ \Omega$, and R_1 and R_2 are reduced by a factor of 10.

15-4.2 Determine a suitable Miller-effect compensating capacitor value for the circuit in part (b) of Problem 15-4.1.

15-5 Load Capacitance Effects

Capacitance connected at the output of an operational amplifier is termed *load capacitance* (C_L). Figure 15-20 shows that C_L is in series with the op-amp output resistance (r_o), so C_L and r_o constitute a phase-lag circuit in the feedback network. As in the case of stray capacitance, another 10° of phase lag introduced by C_L and r_o could cause circuit instability where the phase margin is already small. The equation for calculating the load capacitance that might cause instability is similar to that for stray capacitance;

$$C_L = \frac{1}{2\pi f(10 r_o)} \qquad (15\text{-}6)$$

In Eq. 15-6 f is the frequency at which $A_v B = A_{CL}$. If r_o is reduced, Eq 15-6 gives a larger C_L value. Thus, *an op-amp with a low output resistance can tolerate more load capacitance than one with a higher output resistance.*

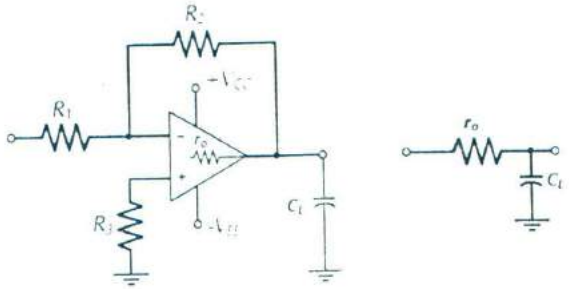
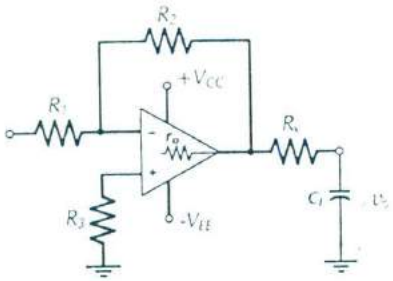
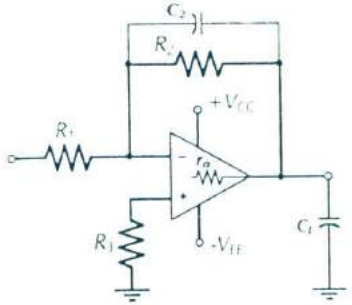


Figure 15-20
Load capacitance at an op-amp output can cause instability by introducing additional phase lag in the feedback network.

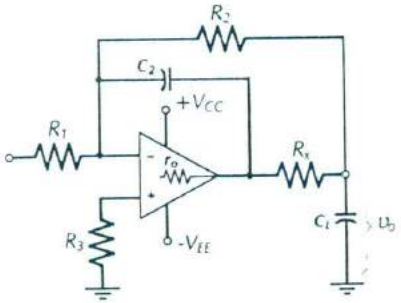
One method often used to counter instability caused by load capacitance is shown in Fig. 15-21(a). A resistor (R_x), usually ranging from 12 Ω to 400 Ω, is connected in series with the load capacitance. The presence of R_x (with R_2 connected at the op-amp output) can severely reduce the phase lag produced by r_o and C_L. However, R_x also has the undesirable effect of increasing the circuit output impedance to approximately the resistance of R_x.



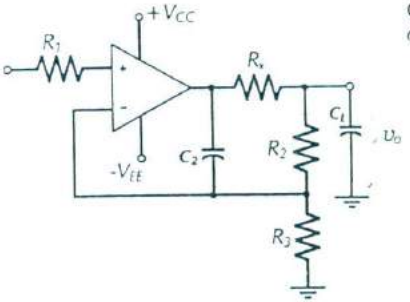
(a) Use of R_x to reduce phase lag



(b) Miller-effect compensation for C_L



(c) Inverting amplifier with combination of R_x and C_2 for C_L compensation



(d) Noninverting amplifier with R_x C_2 combination for C_L compensation

Figure 15-21
Compensation methods for load capacitance.

A Miller-effect capacitor (C_2) connected across feedback resistor R_2 may be used to compensate for the load capacitance, [see Fig. 15-21(b)]. In this case, C_2 introduces some phase-lead in the feedback network to counter the phase-lag. The equation for calculating a suitable capacitance for C_2 is, once again, similar to that for stray capacitance:

$$C_2 R_2 = C_L r_o \qquad \textbf{(15-7)}$$

A modified form of Miller-effect compensation for load capacitance is shown in Fig. 15-21(c). An additional resistor (R_x) is included in series with C_L to reduce the phase lag, as discussed. But now, R_2 is connected at the junction of R_x and C_L, so that (because of feedback) R_x has no significant effect on the circuit output impedance. Also, C_2 is connected from the op-amp output terminal to the inverting input. With this arrangement, Eq. 15-7 is modified to,

$$C_2 R_2 = C_L (r_o + R_x) \qquad \textbf{(15-8)}$$

It should be noted from Equations 15-7 and 15-8 that, as for stray capacitance, smaller resistance values for R_2 give larger, more convenient, compensating capacitor values.

Example 15-8

Calculate the load capacitance that might cause instability in the circuit of Fig. 15-22(a) if the amplifier cutoff frequency is 2 MHz and its output resistance is 25 Ω. Also, determine a suitable compensating capacitor value for the circuit as modified in Fig. 15-22(b) with a 0.1 μF load capacitance.

Solution

Load capacitance:

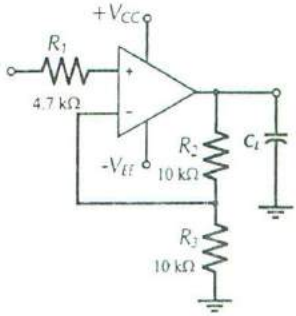
Eq. 15-6, $$C_L = \frac{1}{2\pi f (10 r_o)} = \frac{1}{2\pi \times 2\ \text{MHz} \times 10 \times 25\ \Omega}$$

$$= 318\ \text{pF}$$

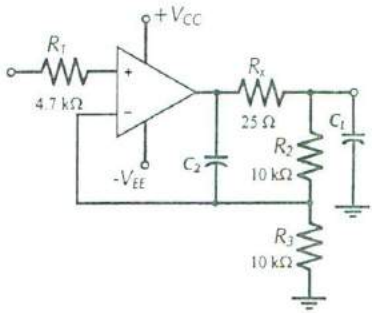
Compensation:

Eq. 15-8, $$C_2 = \frac{C_L (r_o + R_x)}{R_2} = \frac{0.1\ \mu\text{F} \times (25\ \Omega + 25\ \Omega)}{10\ \text{k}\Omega}$$

$$= 500\ \text{pF (standard value)}$$



(a) Noninverting amplifier with load capacitance (C_L)



(b) Amplifier compensated with R_x and C_2

Figure 15-22
Circuits for Example 15-8.

Practise Problems

15-5.1 Calculate the load capacitance that might cause instability in the circuit in Ex. 15-7 if the op-amp output resistance is 20 Ω. Determine a suitable Miller-effect compensating capacitor value.

15-5.2 The circuit is Problem 15-5.1 is modified as in Fig. 15-21(c) with $R_x = 5 R_o$ and $C_L = 0.5\ \mu\text{F}$. Calculate the required C_2 value.

15-6 Circuit Stability Precautions

Power Supply Decoupling

Feedback along supply lines is another source of op-amp circuit instability. This can be minimized by connecting 0.01 μF high-frequency capacitors from each supply terminal to ground (see Fig. 15-23). The capacitors must be connected as close as possible to the *IC* terminals. Sometimes larger-value capacitors are required.

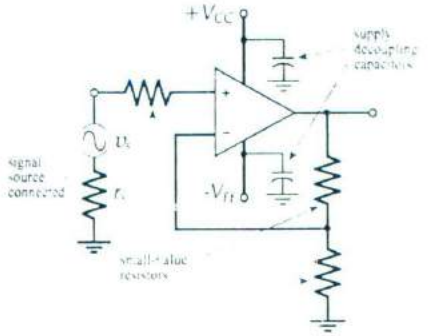


Figure 15-23
For op-amp circuit stability, keep resistor values to a minimum, use the recommended compensating components, bypass the supply terminals to ground, and keep the signal source connected.

Stability Precautions

The following precautions should be observed for circuit stability:

1. Where low-frequency performance is required, use an internally compensated op-amp. Alternatively, use Miller-effect compensation to give the lowest acceptable cutoff frequency.
2. Use small-value resistors in the feedback network, if possible, instead of using the largest possible resistor values.
3. With an op-amp that must be compensated, use the methods and components recommended by the *IC* manufacturer.
4. Keep all component leads as short as possible, and take care with component placement. A resistors connected to an op-amp input terminal should have the resistor body placed close to the input terminal.
5. Use 0.01 μF capacitors (or 0.1 μF capacitors if necessary) to bypass the supply terminals of op-amp (or groups of op-amps) to ground. Connect these capacitors close to the *ICs*.
6. Always have a signal source connected to a circuit being tested. Alternatively, ground the circuit input. With an open-circuited input, very small stray capacitances can cause instability.
7. Do not connect oscilloscopes or other instrument at the op-amp input terminals. Instrument input capacitance can cause instability.
8. If a circuit is unstable after all of the above precautions have been observed, reduce the value of all circuit resistors (except compensating resistors). Also, reduce the signal source resistance if possible.

Chapter-15 Review Questions

Section 15-1

15-1 Show how feedback in an op-amp inverting amplifier can produce instability. Explain the conditions necessary for oscillations to occur in an op-amp circuit.

15-2 Show how feedback in an op-amp noninverting amplifier circuit can produce instability.

15-3 Define: loop gain, loop phase shift, phase margin.

15-4 Sketch typical gain/frequency response and phase/frequency response graphs for an uncompensated operational amplifier. Identify the pole frequencies and rates of fall of voltage gain, and show the typical phase shift at each pole frequency.

15-5 Sketch typical gain/frequency response and phase/frequency response graphs for a compensated operational amplifier. Briefly explain.

15-6 Derive an equation for the open-loop gain of an operational amplifier when the loop gain equals 1.

Section 15-2

15-7 Sketch a lag compensation circuit. Explain its operation and show how it affects the frequency and phase response graphs of an operational amplifier.

15-8 Sketch a lead compensation circuit. Explain its operation and show how it affects the frequency and phase response graphs of an operational amplifier.

15-9 Show how Miller-effect compensation can be applied to an op-amp circuit. Briefly explain.

Section 15-3

15-10 Define bandwidth, gain-bandwidth product, and full-power bandwidth for an operational amplifier. Explain the circuit conditions that apply in each case.

15-11 Define slew-rate, and explain its effect on the output waveform from an operational amplifier.

Section 15-4

15-12 Discuss the effects of stray capacitance at the input terminals of an operational amplifier. Explain the precautions that should be observer to deal with input stray capacitance problems.

15-13 Show how Miller-effect compensation can be used to counter the effects of op-amp input stray capacitance.

Section 15-5

15-14 Discuss the effects of op-amp load capacitance.

15-15 Show how op-amp instability due to load capacitance can be countered by means of: an additional resistor, Miller-effect compensation, a combination of both.

Section 15-6

15-16 List precautions that should be observed for operational amplifier circuit stability. Briefly explain in each case.

Chapter-15 Problems

Section 15-1

15-1 Investigate the stability of the circuit in Fig. 15-11, if the *LM108* is replaced with an op-amp that has the gain/frequency and phase/frequency responses in Fig. 15-2.

15-2 Investigate the stability of the inverting amplifier circuit in Fig. 15-10(a) if the op-amp used is (a) a *741*, (b) an *AD843*. Use the response graphs in Fig. 15-3 and 15-4.

15-3 Investigate the stability of an amplifier circuit with A_{CL} = 70 dB if the op-amp has the gain/frequency and phase/frequency responses in Fig. 15-2.

Section 15-2

15-4 The phase-lag network in Fig. 15-7(a) has: R_1 = 8.2 kΩ, R_2 = 470 Ω, and C_1 = 3300 pF. Calculate the approximate phase lag at 7.5 kHz and at 750 kHz.

15-5 The phase-lead network in Fig. 15-7(c) has: R_1 = 560 Ω, R_2 = 27 kΩ, and C_1 = 1000 pF. Calculate the approximate phase lead at 6 kHz and 300 kHz.

15-6 If the circuit in Fig. 15-22(a) uses an *LM108* op-amp, determine suitable compensation capacitor values. Refer to the *LM108* information in Fig. 15-8.

15-7 Calculate a suitable Miller-effect compensating capacitor to stabilize the circuit in Fig. 15-19 at an 80 kHz cutoff frequency.

15-8 The circuit in Fig. 15-10(b) is to be stabilized at f_2 = 50 kHz. Determine the value of a suitable Miller-effect compensating capacitor.

Section 15-3

15-9 Determine the bandwidth of the circuit in Fig. 15-10(a) if the op-amp has the gain/frequency response graph in Fig. 15-2. Also, determine the bandwidth of the circuit in Fig 15-10(b) if the op-amp is a *741*.

15-10 Find the upper cutoff frequency for the circuit in Fig. 15-19 if the op-amp is (a) a *741*, (b) an *AD843*. Use the response graphs in Fig. 15-3 and 15-4.

15-11 Using the gain-bandwidth product, determine the upper cutoff frequencies for the circuits in Problem 15-10.

15-12 Use the gain-bandwidth product to determine the upper cutoff frequencies for the circuits in Figs. 15-10(a) and (b) if they both have *LM108* op-amps with C_f = 30 pF.

15-13 The circuits in Examples 14-5 and 14-8 use *741* op-amps. Use the gain-bandwidth product to determine the upper cutoff frequency for each circuit.

15-14 If the circuit in Fig. 15-11 has the *LM108* replaced with an *LF353*, use the gain-bandwidth product to determine the upper cutoff frequency.

15-15 Calculate the full-power bandwidth for an amplifier using *741* op-amp if the output voltage is to be (a) 5 V peak-to-peak, (b) 1 V peak-to-peak.

15-16 Recalculate the full power bandwidth in each case in Problem 15-15 if the *741* is replaced with an *LF353*.

15-17 Calculate the full-power bandwidth for the circuit in Example 14-5 if the peak output is to be 2 V. Also, determine the maximum peak output voltage that can be produced by the circuit at the cutoff frequency calculated in Problem 15-13.

15-18 Calculate the slew-rate limited cutoff frequency for the circuit in Example 14-8 if the peak input is 20 mV. Also, determine the maximum peak output voltage at the circuit cutoff frequency calculated in Problem 15-13.

Section 15-4

15-19 A circuit as in Fig. 15-10(a) with C_f removed has a cutoff frequency of 600 kHz. Determine the op-amp input stray capacitance that might cause instability; (a) when the signal source is open-circuited, (b) when a 300 Ω signal source is connected.

15-20 Determine the input stray capacitance that might make the circuit in Fig. 15-10(b) become unstable when a 300 Ω signal source is connected. Assume that the circuit cutoff frequency is 30 kHz and that C_f is removed.

15-21 Calculate the Miller-effect capacitor value required to compensate for 250 pF of input stray capacitance in the circuitry of Problem 15-19(b).

15-22 Calculate the Miller-effect capacitor value required to compensate for 90 pF of stray capacitance in the circuit of Problem 15-20.

15-23 An inverting amplifier (as in Fig. 15-19) uses a *LF353* op-amp, and has; r_s = 600 Ω, R_1 = 220 kΩ, R_2 = 2.2 MΩ, f_2 = 18 kHz. Calculate the input stray capacitance that might make the circuit unstable; (a) when the signal source is

connected, (b) when the signal source is open-circuited.

15-24 Repeat Problem 15-23 when R_1 and R_2 are each reduced by a factor of 10.

Section 15-5

15-25 Determine the load capacitance that might cause instability in the circuit in Fig. 15-10(a) with C_f removed, if the circuit cutoff frequency is 600 kHz, and $r_o = 100\ \Omega$.

15-26 An inverting amplifier (as in Fig. 15-19) uses an op-amp with a 300 Ω output resistance, and has; $R_1 = 220\ k\Omega$, $R_2 = 2.2\ M\Omega$. Calculate the load capacitance that might make the circuit unstable.

15-27 Calculate the Miller-effect capacitor value required to compensate for a 0.1 μF load capacitance in the circuit of Fig. 15-10(a) if $f_2 = 600$ kHz.

15-28 Calculate the Miller-effect capacitor value required to compensate for the load capacitance in Problem 15-26.

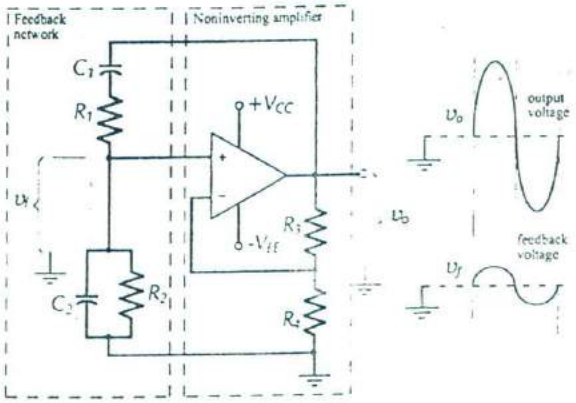
15-29 Determine the load capacitance that might cause instability in the circuit in Fig. 15-22(a), if the cutoff frequency is 400 kHz, and the op-amp has $r_o = 150\ \Omega$.

15-30 The circuit in Problem 15-29 is rearranged as in Fig. 15-22(b) with $R_x = 10\ r_o$. Calculate the required C_2 value to compensate for a 5000 pF load capacitance.

Practise Problem Answers

15-1.1 30°, 90°, 90°
15-2.1 -48.5°, 41.5°
15-2.2 82 pF
15-3.1 50 kHz
15-3.2 27 kHz, 1.13 MHz
15-3.3 296 kHz
15-4.1 0.05 pF, 34.5 pF
15-4.2 0.5 pF
15-5.1 995 pF, 2 pF
15-5.2 6000 pF

Chapter 16
Signal Generators



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Objectives

You will be able to:

1. Draw the following types of sine wave oscillator circuits, and explain the operation of each: Phase shift, Colpitts, Hartley, Wein bridge
2. Analyze each of the above oscillator circuits to determine the oscillation frequency.
3. Design each of the above oscillator circuits to produce a specified output frequency.
4. Sketch oscillator amplitude stabilization circuits and explain their operation.
5. Design circuits to limit oscillator outputs to a specified amplitude.
6. Draw square wave and triangular wave generator circuits. Sketch the circuit waveforms and explain the operation of each circuit.
7. Analyze square and triangular waveform generators to determine the amplitude and frequency of the output waveform.
8. Design square and triangular waveform generators to produce a specified output amplitude and frequency.
9. Explain piezoelectric crystals, sketch the crystal equivalent circuit, and the crystal impedance/frequency graph.
10. Show how crystals may be used for oscillator frequency stabilization, and design crystal-controlled oscillators.

Introduction

A sinusoidal oscillator usually consists of an amplifier and a phase-shifting network. The amplifier receives the output from the network, amplifies it, phase shifts it by 180°, and applies it to the network input. The network phase shifts the amplifier output by a further 180°, and attenuates it before feeding it back to the amplifier input. When the amplifier gain equals the inverse of the network attenuation, and the amplifier phase shift equals the network phase shift, the circuit is amplifying an input to produce an output which is attenuated to become the input. The circuit is generating its own input signal, and a state of oscillation exists.

Some signal generators produce square or triangular waveforms. These normally use nonlinear circuits and resistor/capacitor charging circuits.

16-1 Phase Shift Oscillators

Op-Amp Phase Shift Oscillator

Figure 16-1 shows the circuit of a *phase shift oscillator*, which consists of an inverting amplifier and an *RC* phase-shifting network. The amplifier phase-shifts its input by -180°, and the *RC phase-lead* network phase-shifts the amplifier output by a +180°, giving a total loop phase shift of zero. The attenuated feedback signal (at the amplifier input) is amplified to reproduce the output. In this condition the circuit is generating its own input signal, consequently, it is oscillating. The output and feedback voltage waveforms in Fig. 16-1 illustrate the circuit operation.

For a state of oscillation to be sustained in any sinusoidal oscillator circuit, certain conditions, known as the *Barkhausen criteria*, must be fulfilled:

The loop gain must be equal to (or greater than) one.
The loop phase shift must be zero.

The *RC* phase-lead network in Fig. 16-1 consists of three equal-value resistors and three equal-value capacitors. Resistor R_1 functions as the last resistor in the *RC* network and as the amplifier input resistor. A *phase-lag* network would give a total loop phase shift of -360°, and so it would work just as well as the phase lead network.

The frequency of the oscillator output depends upon the component values in the *RC* network. The circuit can be analyzed to show that the phase shift is 180° when

$$X_c = \sqrt{6}\,R$$

This gives an oscillation frequency,

$$f = \frac{1}{2\pi R C \sqrt{6}} \qquad (16\text{-}1)$$

As well as phase shifting the amplifier output, the *RC* network

attenuates the output. It can be shown that, when the required 180° phase shift is produced, the feedback factor (B) is always 1/29. This means that the amplifier must have a closed-loop voltage gain (A_{CL}) of at least 29 to give a loop gain ($B\,A_{CL}$) of one; otherwise the circuit will not oscillate. For example, if the amplifier output voltage is 10 V, the feedback voltage is,

$$v_f = B\,v_o = 10\text{ V}/29$$

To reproduce the 10 V output, v_f must be amplified by 29,

$$\begin{aligned} v_o &= A_{CL}\,v_f = 29 \times (10\text{ V}/29) \\ &= 10\text{ V} \end{aligned}$$

If the amplifier voltage gain is much greater than 29, the output waveform will be distorted. When the gain is slightly greater than 29, a reasonably pure sine wave output can be expected. The gain is usually designed to be just over 29 to ensure that the circuit oscillates. The output voltage amplitude normally peaks at $\pm(V_{CC} - 1\text{ V})$, unless a rail-to-rail op-amp is used (see Section 14-9).

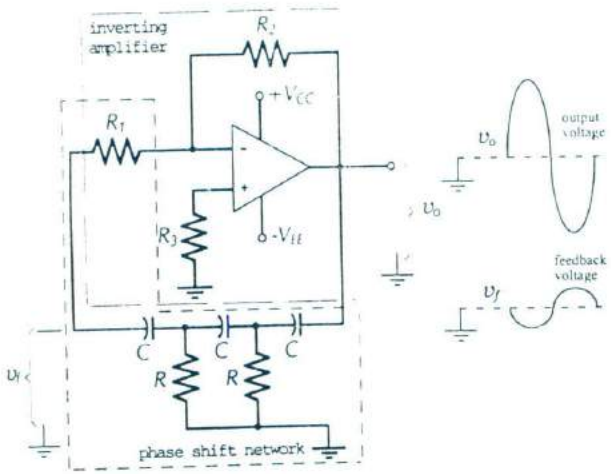


Figure 16-1
A phase shift oscillator consists of an inverting amplifier and an RC phase shifting feedback network. The RC network attenuates the output and phase shifts it by 180°. The amplifier amplifies the network output and phase shifts it through a further 180°.

Circuit Design

Design of a phase shift oscillator begins with design of the amplifier to have a closed-loop gain just greater than 29. The resistor values for the *RC* network are then selected equal to the amplifier input resistor (R_1), and the capacitor values are calculated from Eq. 16-1. In some cases, this procedure might produce capacitor values not much larger than stray capacitance. So, alternatively, the design might start with selection of convenient capacitor values. Equation 16-1 is then used to calculate the resistance of R (and R_1). Finally, R_2 is selected to give the required amplifier gain.

Example 16-1

Using a *741* op-amp with a ±10 V supply, design the phase shift oscillator in Fig. 16-2 to produce a 1 kHz output frequency.

Solution

Select $I_1 \approx 100 \times I_{B(max)} = 100 \times 500\ \text{nA}$

$= 50\ \mu\text{A}$

$v_o \approx \pm(V_{CC} - 1\ \text{V}) \approx \pm(10\ \text{V} - 1\ \text{V})$

$\approx \pm 9\ \text{V}$

$$v_i = \frac{v_o}{A_{CL}} = \frac{\pm 9\ \text{V}}{29}$$

$= \pm 0.31\ \text{V}$

$$R_1 = \frac{v_i}{I_1} = \frac{0.31\ \text{V}}{50\ \mu\text{A}}$$

$= 6.2\ \text{k}\Omega$ (use 5.6 kΩ standard value)

$R_2 = A_{CL} R_1 = 29 \times 5.6\ \text{k}\Omega$

$\approx 162\ \text{k}\Omega$ (use 180 kΩ to give $A_{CL} > 29$)

$R_3 = R_2 = 180\ \text{k}\Omega$ (the *dc* path through R_1 is interrupted by C)

$R = R_1 = 5.6\ \text{k}\Omega$

From Eq. 16-1, $$C = \frac{1}{2\pi R f \sqrt{6}} = \frac{1}{2\pi \times 5.6\ \text{k}\Omega \times 1\ \text{kHz} \times \sqrt{6}}$$

$\approx 0.01\ \mu\text{F}$ (standard value)

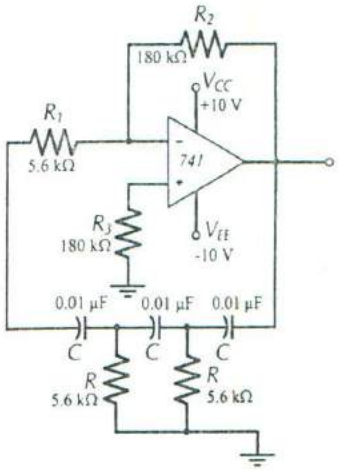


Figure 16-2
Phase shift oscillator circuit for Example 16-1.

Although the *741* op-amp used in Ex. 16-1 is likely to be quite suitable for the particular circuit, some care should always be taken when selecting an operational amplifier. It should be recalled (from Ch. 15) that when a large output voltage swing is required, the op-amp full-power bandwidth is involved. This must be considered when selecting an operational amplifier for an oscillator circuit.

BJT Phase Shift Oscillator

A phase shift oscillator using a single *BJT* amplifier is shown in Fig. 16-3. Once again, the amplifier and phase shift network each produce 180° of phase shift, the *BJT* amplifies the network output, and the network attenuates the amplifier output.

First thoughts about this circuit (in comparison to the op-amp phase shift oscillator) would suggest that a *BJT* amplifier with a voltage gain of 29 is required. An attempt to design such a circuit

reveals that in many cases the amplifier output is overloaded by the phase shift network, or else the network output is overloaded by the amplifier input. The problem can be solved by including an emitter follower in the circuit. However, the circuit can function satisfactorily without any additional components if the transistor is treated as a current amplifier, rather than as a voltage amplifier. In this case, circuit analysis gives,

$$f = \frac{1}{2\pi R C \sqrt{(6 + 4R_C/R)}} \qquad \textbf{(16-2)}$$

and,

$$h_{fe(min)} = 23 + \frac{29\,R}{R_C} + \frac{4\,R_C}{R} \qquad \textbf{(16-3)}$$

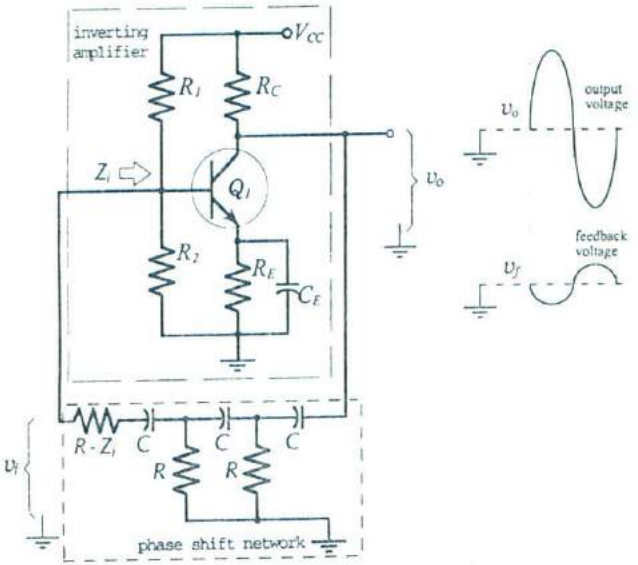


Figure 16-3
Phase shift oscillator using an inverting BJT amplifier and an RC feedback network.

The circuit oscillates only if the *BJT* current gain is equal to (or larger than) the minimum value determined from Eq. 16-3. With $R = R_C$, a minimum h_{fe} of 56 is required to sustain circuit oscillation. With $R = 10\,R_C$, $h_{fe(min)}$ must be greater than 300. The output waveform is likely to be distorted if h_{fe} is substantially greater than the calculated $h_{fe(min)}$. Because h_{fe} varies widely from one transistor to another, R_C should be partially adjustable to minimize distortion. Note that in Fig. 16-3, the amplifier input resistance (Z_i) constitutes part of the last resistor in the phase shift network.

Circuit Design

BJT phase shift oscillator design should be approached by first selecting R equal to or greater than the estimated amplifier Z_i. Then, R_C is selected equal to R, C is calculated from Eq. 16-2, and the rest of the component values are determined for the circuit *dc* conditions. The impedance of C_E should be much lower than $h_{ie}/(1 + h_{fe})$ at the oscillating frequency.

Practise Problems

16-1.1 Using a *BIFET* op-amp with rail-to-rail operation, design a phase shift oscillator to produce a 6.5 kHz, ±12 V output.

16-1.2 Design a *BJT* phase shift oscillator, as in Fig. 16-3, to produce a 900 Hz waveform with a 10 V peak-to-peak amplitude. Assume that the *BJT* has $h_{fe(min)} \approx 60$ and $h_{ie} \approx 1.5\ k\Omega$.

16-2 Colpitts Oscillators

Op-Amp Colpitts Oscillator

The *Colpitts oscillator* circuit show in Fig. 16-4 is similar to the op-amp phase shift oscillator, except that an *LC* network is used to produce the necessary phase shift in the feedback voltage. In this case, the *LC* network acts as a filter that passes the oscillating frequency and blocks all other frequencies. The filter circuit resonates at the required oscillating frequency. For resonance,

$$X_L = X_{CT}$$

where X_{CT} is the total capacitance in paraliel with the inductor. This gives the resonance frequency (and oscillating frequency) as,

$$f = \frac{1}{2\pi\sqrt{(L_1\ C_T)}} \qquad \textbf{(16-4)}$$

Capacitors C_1 and C_2 are connected in series across L_1; so,

$$C_T = \frac{C_1\ C_2}{C_1 + C_2} \qquad \textbf{(16-5)}$$

Consideration of the *LC* network shows that its attenuation (from the amplifier output to input) is due to the voltage divider effect of L and C_1. This gives,

$$B = \frac{X_{C1}}{X_{L1} - X_{C1}}$$

It can be shown that the required 180° phase shift occurs when

$$X_{C2} = X_{L1} - X_{C1}$$

and this gives,

$$B = \frac{X_{C1}}{X_{C2}} = \frac{C_2}{C_1}$$

As in the case of all oscillator circuits, the loop gain must be a minimum of one to ensure oscillation. Therefore,

$$A_{CL(min)}\,B = 1$$

or, $$A_{CL(min)} = \frac{C_1}{C_2} \qquad (16\text{-}6)$$

When deriving the above equations, it was assumed that the inductor coil resistance is very much smaller than the inductor impedance; that is, that the coil Q factor ($\omega L/R$) is large. This must be taken into considered when selecting an inductor. It was also assumed that the amplifier input resistance is much greater than the impedance of C_1 at the oscillating frequency. Because of the inductor resistance and the amplifier input resistance, and because of stray capacitance effects when the oscillator operates at a high-frequency, the amplifier voltage gain usually has to be substantially larger than C_1/C_2.

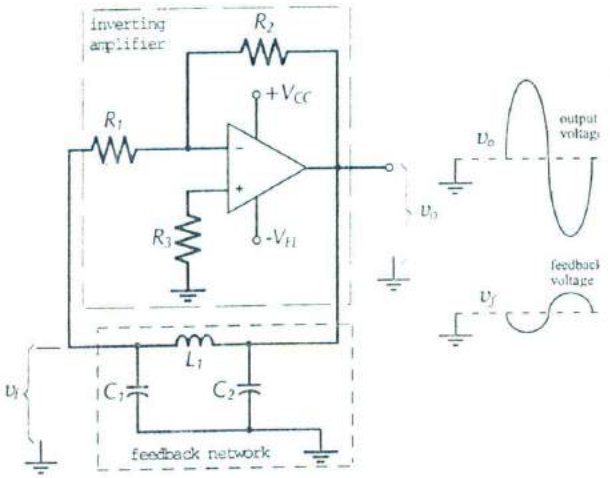


Figure 16-4
A Colpitts oscillator consists of an inverting amplifier and an LC phase shifting feedback network.

Circuit Design

Colpitts oscillator design can commence with selection of the smallest capacitor (C_2) much larger than stray capacitance, or with selection of a convenient value of L. To keep the amplifier input voltage to a fairly low level, the feedback network is often designed to attenuate the output voltage by a factor of 10. This requires that $C_1/C_2 \approx 10$. (It should be recalled that large A_{CL} values require larger op-amp bandwidths.) Also, X_{C2} should be much larger than the amplifier output impedance. Using the desired oscillating frequency, L can be calculated from Eq. 16-4. Amplifier input resistor R_1 must be large enough to avoid overloading the feedback network, ($R_1 >> X_{C1}$). Resistor R_2 is determined from A_{CL} and R_1.

Example 16-2

Design the Colpitts oscillator in Fig. 16-5 to produce a 40 kHz output frequency. Use a 100 mH inductor and an op-amp with a ±10 V supply.

Solution

From Eq. 16-4, $$C_T = \frac{1}{4\pi^2 f^2 L} = \frac{1}{4\pi^2 \times (40\text{ kHz})^2 \times 100\text{ mH}}$$
$$= 153.8\text{ pF}$$

For $C_1 \approx 10\,C_2$, $$C_1 \approx 10\,C_T = 10 \times 153.8\text{ pF}$$
$$\approx 1538\text{ pF (use 1500 pF standard value)}$$

From Eq. 16-5, $$C_2 = \frac{1}{(1/C_T) - (1/C_1)} = \frac{1}{(1/158.3\text{ pF}) - (1/1500\text{ pF})}$$
$$= 177\text{ pF (use 180 pF standard value)}$$

$$X_{C2} = \frac{1}{2\pi f C_2} = \frac{1}{2\pi \times 40\text{ kHz} \times 180\text{ pF}}$$
$$= 22\text{ k}\Omega$$

$X_{C2} >> Z_o$ of the amplifier

$$X_{C1} = \frac{1}{2\pi f C_1} = \frac{1}{2\pi \times 40\text{ kHz} \times 1500\text{ pF}}$$
$$= 2.65\text{ k}\Omega$$

$R_1 >> X_{C1}$

Select $R_1 = 10\,X_{C1} = 10 \times 2.65\text{ k}\Omega$
$= 26.5\text{ k}\Omega$ (use 27 kΩ standard value)

From Eq. 16-6, $$A_{CL(min)} = \frac{C_1}{C_2} = \frac{1500\text{ pF}}{180\text{ pF}}$$
$$= 8.33$$

$$R_2 = A_{CL}\,R_1 = 8.33 \times 27\text{ k}\Omega$$
$$= 225\text{ k}\Omega\text{ (use 270 k}\Omega\text{ standard value)}$$

$$R_3 = R_1 \| R_2 = 27\text{ k}\Omega \| 270\text{ k}\Omega$$
$$= 24.5\text{ k}\Omega\text{ (use 27 k}\Omega\text{ standard value)}$$

The op-amp full-power bandwidth (f_p) must be a minimum of 40 kHz when $v_o \approx \pm 9$ V and $A_{CL} = 8.33$.

from Eq. 15-2, $$f_2 = A_{CL} \times f_p = 8.33 \times 40\text{ kHz}$$
$$= 333\text{ kHz}$$

from Eq. 15-3, $$SR = 2\pi f_p v_p = 2\pi \times 40\text{ kHz} \times 8\text{ V}$$
$$= 2\text{ V}/\mu\text{s}$$

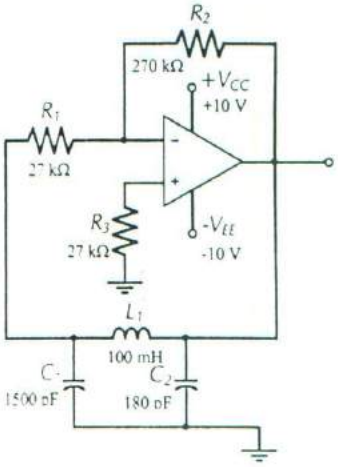
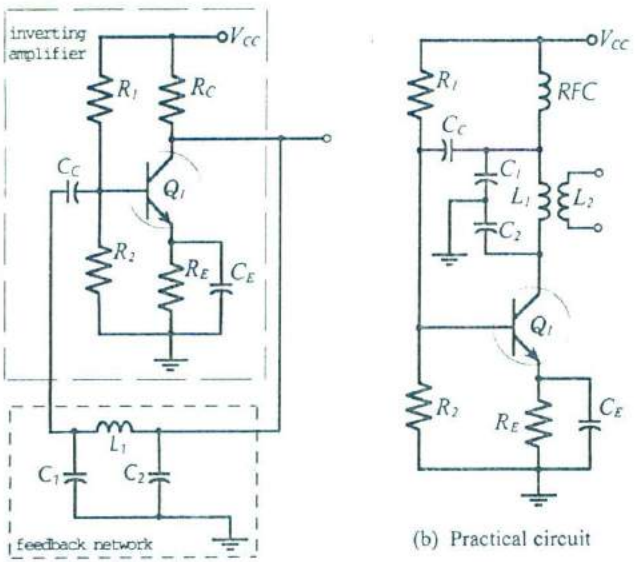


Figure 16-5
Colpitts oscillator circuit for Example 16-2.

BJT Colpitts Oscillator

A Colpitts oscillator using a single *BJT* amplifier is shown in Fig. 16-6(a). This is the basic circuit, and its similarity to the op-amp Colpitts oscillator is fairly obvious. A more complex version of the circuit is shown in Fig. 16-6(b). Components Q_1, R_1, R_2, R_E, and C_E in (b) are unchanged from (a), but collector resistor R_C is replaced with inductor L_1. A radio frequency choke (*RFC*) is included in series with V_{CC} and L_1. This allows *dc* collector current (I_C) to pass, but offers a very high impedance at the oscillating frequency, so that the top of L_1 is *ac* isolated from V_{CC} and ground. The output of the *LC* network (L_1, C_1, C_2) is coupled to via C_c to the amplifier input. The circuit output voltage (v_o) is derived from a secondary winding (L_2) coupled to L_1. As in the case of the *BJT* phase shift oscillator, the transistor current gain is important. Circuit analysis gives Eq. 16-4 for frequency, and for current gain,

$$h_{fe(min)} = \frac{C_1}{C_2} \qquad \textbf{(16-7)}$$



(a) Basic circuit

(b) Practical circuit

Figure 16-6
Colpitts oscillator using an inverting BJT amplifier and an LC feedback network.

Practise Problems

16-2.1 Design a Colpitts oscillator circuit to produce a 12 kHz, ±10 V output. Use a *741* op-amp.

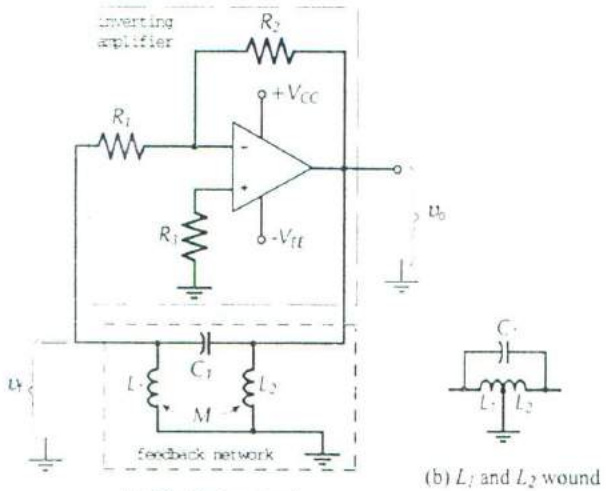
16-2.2 Design the oscillator in Fig. 16-6(a) to produce a 20 kHz, 6 V p-to-p output. Use a 10 mH inductor and assume that the *BJT* has $h_{ib} \approx 26\ \Omega$ and $h_{ie} \approx 1.5\ k\Omega$.

16-3 Hartley Oscillators

Op-Amp Hartley Oscillator

The *Hartley oscillator* circuit is similar to the Colpitts oscillator, except that the feedback network consists of two inductors and a capacitor instead of two capacitors and an inductor. Figure 16-7(a) shows the Hartley oscillator circuit, and Fig. 16-7(b) illustrates the fact that L_1 and L_2 may be wound on a single core so that there is mutual inductance (M) between the two windings. In this case, the total inductance is,

$$L_T = L_1 + L_2 + 2M \qquad (16\text{-}8)$$



(a) Oscillator circuit

(b) L_1 and L_2 wound on a single core

Figure 16-7
Hartley oscillator circuit using an op-amp inverting amplifier and an LC feedback network.

Oscillation occurs at the feedback network resonance frequency ;

$$f = \frac{1}{2\pi\sqrt{(C_1 L_T)}} \qquad (16\text{-}9)$$

The attenuation of the feedback network is

$$B = \frac{X_{L1}}{X_{L1} - X_{C1}}$$

It can be shown that the required 180° phase shift occurs when

$$X_{L2} = X_{L1} - X_{C1}$$

The loop gain must be a minimum of one, giving:

$$A_{CL(min)} = \frac{L_2}{L_1} \qquad (16\text{-}10)$$

Design procedure for a Hartley oscillator circuit is similar to that for a Colpitts oscillator.

Example 16-3

Design the Hartley oscillator in Fig. 16-8 to produce a 100 kHz output frequency with an amplitude of approximately ±8 V. For simplicity, assume that there is no mutual inductance between L_1 and L_2.

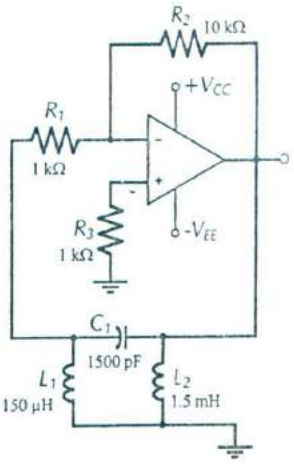


Figure 16-8
Hartley oscillator circuit for Example 16-3.

Solution

$$V_{CC} \approx v_o + 1\text{ V} = \pm(8\text{ V} + 1\text{ V})$$
$$\approx \pm 9\text{ V}$$

$$X_{L2} >> Z_o \text{ of the amplifier}$$

select $X_{L2} \approx 1\text{ k}\Omega$

$$L_2 = \frac{X_{L2}}{2\pi f} = \frac{1\text{ k}\Omega}{2\pi \times 100\text{ kHz}}$$
$$= 1.59\text{ mH} \quad \text{(use 1.5 mH standard value)}$$

select $$L_1 \approx \frac{L_2}{10} = \frac{1.5\text{ mH}}{10}$$
$$= 150\,\mu\text{H} \quad \text{(standard value)}$$

$$L_T = L_1 + L_2 = 1.5\text{ mH} + 150\,\mu\text{H} \text{ (assuming } M = 0)$$
$$= 1.65\text{ mH}$$

From Eq. 16-9, $$C_1 = \frac{1}{4\pi^2 f^2 L_T} = \frac{1}{4\pi^2 \times (100\text{ kHz})^2 \times 1.65\text{ mH}}$$
$$= 1535\text{ pF} \quad \text{(use 1500 pF with additional parallel capacitance, if necessary)}$$

$$C_1 >> \text{stray capacitance}$$

$$X_{L1} = 2\pi f L_1 = 2\pi \times 100\text{ kHz} \times 150\,\mu\text{H}$$
$$= 94.2\,\Omega$$

$$R_1 >> X_{L1}$$

Select $R_1 = 1\text{ k}\Omega$ (standard value)

From Eq. 16-10,
$$A_{CL(min)} = \frac{L_2}{L_1} = \frac{1.5\text{ mH}}{150\mu\text{H}}$$
$$= 10$$

$$R_2 = A_{CL} R_1 = 10 \times 1\text{ k}\Omega$$
$$= 10\text{ k}\Omega \text{ (standard value)}$$

$$R_3 = R_1 \| R_2 = 1\text{ k}\Omega \| 10\text{ k}\Omega$$
$$= 909\,\Omega \text{ (use 1 k}\Omega\text{ standard value)}$$

The op-amp full-power bandwidth (f_p) must be a minimum of 100 kHz when $v_o \approx \pm 8$ V and $A_{CL} = 10$.

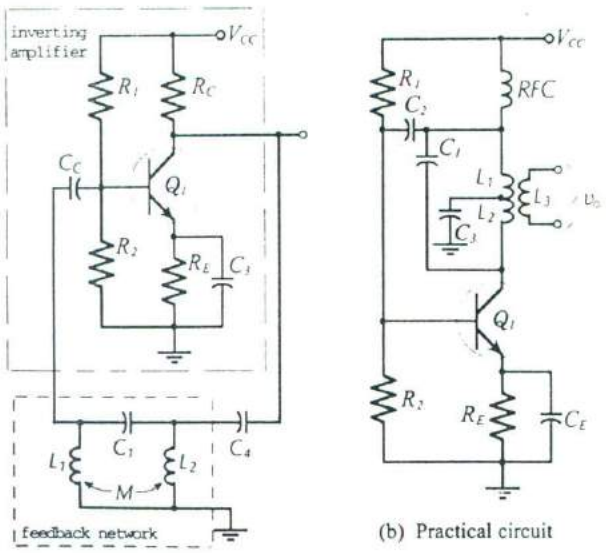
from Eq. 15-2, $f_2 = A_{CL} \times f = 10 \times 100$ kHz
$= 1$ MHz

from Eq. 15-3, $SR = 2\pi f_p v_p = 2\pi \times 100$ kHz $\times 8$ V
$= 5$ V/μs

BJT Hartley Oscillator

Figure 16-9 shows the circuit of a Hartley oscillator using a *BJT* amplifier. The basic circuit in Fig. 16-9(a) is similar to the op-amp Hartley oscillator, and its operation is explained in the same way as for the op-amp circuit. Note that coupling capacitors C_2 and C_4 are required to avoid *dc* grounding the transistor base and collector terminals through L_1 and L_2.

In the practical *BJT* Hartley oscillator circuit shown in Fig. 16-9(b) L_1, L_2, and C_1 constitute the phase shift network. In this case, the inductors are directly connected in place of the transistor collector resistor (R_C). The circuit output is derived from the additional inductor winding (L_3). The radio frequency choke (*RFC*) passes the direct collector current, but *ac* isolates the upper terminal of L_1 from the power supply. Capacitor C_2 couples the output of the feedback network back to the amplifier input. Capacitor C_4 at the *BJT* collector in Fig. 16-9(a) is not required in Fig. 16-9(b), because L_2 is directly connected to the collector terminal. The junction of L_1 and L_2 must now be capacitor coupled to ground (via C_3) instead of being direct coupled.



(a) Basic circuit

(b) Practical circuit

Figure 16-9
Hartley oscillator consisting of a BJT inverting amplifier and an LC feedback network.

Practise Problems

16-3.1 A Hartley oscillator circuit using a *741* op-amp is to produce a 7 kHz, ±10 V output. Determine suitable component values.

16-3.2 Analyze the *BJT* Hartley oscillator in Fig. 16-9(b) to determine the oscillating frequency. Some of the component values are: $L_1 = L_2 = 4.7$ mH; $C_1 = 600$ pF, $C_2 = C_3 = 0.03\ \mu$F. The mutual inductance between L_1 and L_2 is 100 μH.

16-4 Wein bridge Oscillator

The *Wein bridge* is an *ac* bridge that balances only at a particular supply frequency. In the *Wein bridge oscillator* (Fig. 16-10), a Wein bridge circuit is used as a feedback network between the amplifier output and input. The bridge is made up of all of the resistors and capacitors. The operational amplifier together with resistors R_3 and R_4 constitute a noninverting amplifier. The feedback network from the amplifier output to its noninverting input terminal is made up of components C_1, R_1, C_2 and R_2.

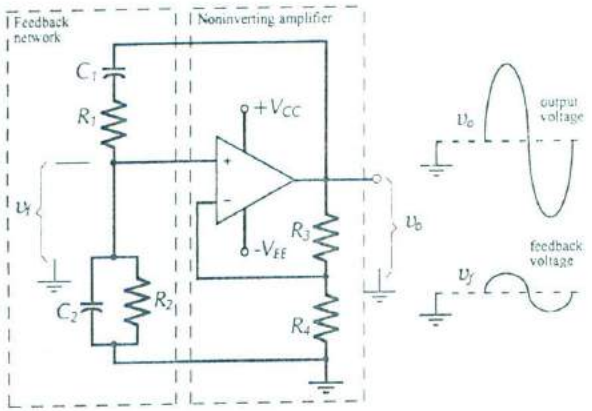


Figure 16-10
The Wein bridge oscillator circuit uses an operational amplifier and a Wein bridge which balances at a particular frequency.

At the balance frequency of the Wein bridge, the feedback voltage is in phase with the amplifier output. This (in-phase) voltage is amplified to reproduce the output. At all other frequencies, the bridge is off balance; that is, the feedback and output voltages do not have the correct phase relationship to sustain oscillations. The Barkhausen requirement for zero loop phase shift is fulfilled in this circuit by the amplifier and feedback network both having zero phase shift at the oscillation frequency.

Analysis of the bridge circuit shows that balance is obtained when two equations are fulfilled:

$$\frac{R_3}{R_4} = \frac{R_1}{R_2} + \frac{C_2}{C_1} \qquad (16\text{-}11)$$

and,
$$2\pi f = \frac{1}{\sqrt{(R_1 C_1 R_2 C_2)}} \qquad \textbf{(16-12)}$$

If $R_1 C_1 = R_2 C_2$, Eq. 16-12 yields,

$$f = \frac{1}{2\pi R_1 C_1} \qquad \textbf{(16-13)}$$

For simplicity, the components are often selected as, $R_1 = R_2$ and $C_1 = C_2$, causing Eq. 16-11 to give,

$$R_3 = 2 R_4 \qquad \textbf{(16-14)}$$

In this case, the amplifier closed-loop gain is, $A_{CL} = 3$.

Sometimes it is preferable to have an amplifier voltage gain substantially greater than 3, then the relationship between the component values is determined by Equations 16-11 and 16-12.

Design of a Wein bridge oscillator can be commenced by selecting a current level for each arm of the bridge. This should be much larger than the op-amp input bias current. Resistors R_3 and R_4 can then be calculated using the estimated output voltage and the closed-loop gain. After that, the other component values can be determined from the above equations.

An alternative design approach is to start by selecting a convenient value for the smallest capacitor in the circuit. The other component values are then calculated from the equations.

Example 16-4

Design the Wein bridge oscillator in Fig. 16-11 to produce a 100 kHz, ±9 V output. Design the amplifier to have a closed-loop gain of 3.

Solution

$$V_{CC} \approx \pm(V_o + 1\text{ V}) = \pm(9\text{ V} + 1\text{ V})$$
$$= \pm 10\text{ V}$$

for $A_{CL} = 3$, $R_1 = R_2$ and $C_1 = C_2$

also, $R_3 = 2 R_4$

select, $C_1 = 1000$ pF (standard value)

$C_2 = C_1 = 1000$ pF

From Eq. 16-13,
$$R_1 = \frac{1}{2\pi f C_1} = \frac{1}{2\pi \times 100\text{ kHz} \times 1000\text{ pF}}$$
$$= 1.59\text{ k}\Omega \text{ (use 1.5 k}\Omega\text{ standard value)}$$

$R_2 = R_1 = 1.5$ kΩ

select, $R_4 \approx R_2 = 1.5$ kΩ (standard value)

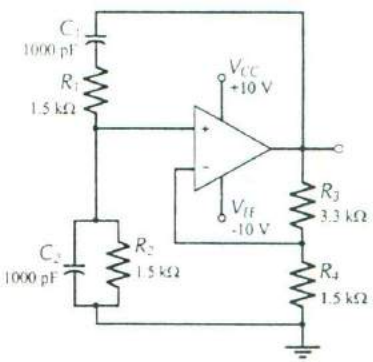


Figure 16-11
Wein bridge oscillator circuit for Example 16-4.

$R_3 = 2 R_4 = 2 \times 1.5\ k\Omega$
$= 3\ k\Omega$ (use 3.3 kΩ standard value)

The op-amp must have a minimum full-power bandwidth (f_p) of 100 kHz when $v_o \approx \pm 9$ V and $A_{CL} = 3$.

from Eq. 15-2, $f_2 = A_{CL} \times f = 3 \times 100\ kHz$
$= 300\ kHz$

from Eq. 15-3, $SR = 2 \pi f_p v_p = 2 \pi \times 100\ kHz \times 9\ V$
$\approx 5.7\ V/\mu s$

Practise Problems

16-4.1 Resistors R_1 and R_2 in Fig. 16-11 are switched to (a) 15 kΩ and (b) 5.6 kΩ. Calculate the new oscillating frequency in each case.

16-4.2 A Wein bridge oscillator using an op-amp is to produce a 15 kHz, ±14 V output. Design the circuit with the amplifier having $A_{CL} = 11$.

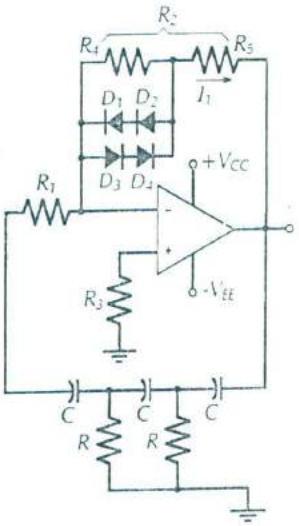
16-5 Oscillator Amplitude Stabilization

Output Amplitude

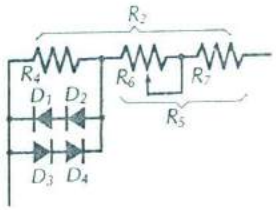
For all of the oscillator circuits discussed, the output voltage amplitude is determined by the amplifier maximum output swing. The output waveform may also be distorted by the amplifier output saturation limitations. To minimize distortion and reduce the output voltage to an acceptable level, *amplitude stabilization* circuitry must be employed. Amplitude stabilization operates by ensuring that oscillation is not sustained if the output exceeds a predetermined level.

Diode Stabilization Circuit for a Phase Shift Oscillator

The phase shift oscillator discussed in Section 16-1 must have a minimum amplifier gain of 29 for the circuit to oscillate. Consider the oscillator circuit in Fig. 16-12(a) that has part of resistor R_2 bypassed by series-parallel connected diodes. When the output amplitude is low, the diodes do not become forward biased, and so they have no effect on the circuit. At this time, the amplifier voltage gain is, $A_{CL} = R_2/R_1$. As always for a phase shift oscillator, A_{CL} is designed to exceed the critical value of 29. When the output amplitude becomes large enough to forward bias either D_1 and D_2, or D_3 and D_4, resistor R_4 is short-circuited, and the amplifier gain becomes, $A_{CL} = R_5/R_1$. This is designed to be too small to sustain oscillations. So, this circuit cannot oscillate with a high-amplitude output, however it can (and does) oscillate with a low-amplitude output.



(a) Phase shift oscillator with amplitude stabilization



(b) Use of adjustable resistor for distortion control

Figure 16-12
The output amplitude of a phase shift oscillator can be limited by using diodes to modify the amplifier gain.

In designing the amplitude stabilization circuit, the inverting amplifier is designed in the usual manner with one important difference. The current (I_1) used in calculating the resistor values must be selected large enough to forward bias the diodes into the near-linear region of their characteristics. This usually requires a minimum current around 1 mA. Resistor R_1 is calculated using,

$$R_1 = \frac{v_o/29}{I_1} \tag{16-15}$$

and R_2 is determined as,

$$R_2 = 29\,R_1 \tag{16-16}$$

The diodes should become forward biased just when the output voltage is at the desired maximum level. At this time, I_1 produces a voltage drop of 2 V_F across R_4.

so,
$$R_4 \approx \frac{2\,V_F}{I_1} \tag{16-17}$$

and,
$$R_5 = R_2 - R_4$$

The resultant component values should give $(R_4 + R_5)/R_1$ slightly greater than 29, and R_5/R_1 less than 29.

Some distortion of the waveform can occur if $(R_4 + R_5)/R_1$ is much larger than 29, however, attempts to make the gain close to 29 can cause the circuit to stop oscillating. Making a portion of R_5 adjustable, as illustrated in Fig. 16-12(b), provides for gain adjustment to give the best possible output waveform. Typically, R_6 should be approximately 40% of the calculated value of R_5, and R_7 should be 80% of R_5. This gives a ±20% adjustment of R_5.

The diodes selected should be low-current switching devices. The diode reverse breakdown voltage should exceed the circuit supply voltage, and the maximum reverse recovery time ($t_{rr(max)}$) should be around one-tenth of the time period of the oscillation frequency,

$$t_{rr(max)} = \frac{T}{10} \tag{16-18}$$

Example 16-5

Design the phase shift oscillator in Fig. 16-13 to produce a 5 kHz, ±5 V output waveform.

Solution

Select $I_1 \approx 1$ mA when $v_{o(peak)} = 5$ V

Eq. 16-15, $$R_1 = \frac{v_o/29}{I_1} = \frac{5\text{ V}/29}{1\text{ mA}}$$

$$= 170\ \Omega \text{ (use } 150\ \Omega)$$

Eq. 16-16, $R_2 = 29\,R_1 = 29 \times 150\ \Omega$
$\approx 4.4\ k\Omega$

Eq. 16-17, $R_4 = \dfrac{2\,V_F}{I_1} = \dfrac{2 \times 0.7\ V}{1\ mA}$
$= 1.4\ k\Omega$ (use 1.5 kΩ standard value)

$R_3 = R_2 - R_4 = 4.4\ k\Omega - 1.5\ k\Omega$
$= 2.9\ k\Omega$

$R_6 = 0.4\,R_5 = 0.4 \times 2.9\ k\Omega$
$= 1.16\ \Omega$ (use 1 kΩ adjustable)

$R_7 = 0.8\,R_5 = 0.8 \times 2.9\ k\Omega$
$= 2.32\ k\Omega$ (use 2.7 kΩ standard value)

$R_3 \approx R_2 = 4.4\ k\Omega$ (use 4.7 kΩ standard value)

$R = R_1 = 150\ \Omega$

From Eq. 16-1, $C = \dfrac{1}{2\,\pi\,R\,f\,\sqrt{6}} = \dfrac{1}{2\,\pi \times 150\ \Omega \times 5\ kHz \times \sqrt{6}}$
$= 0.087\ \mu F$ (use 0.082 μF standard value)

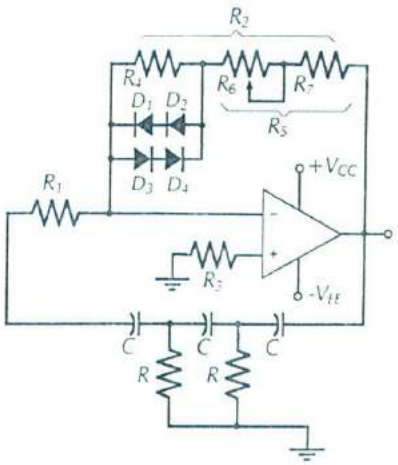


Figure 16-13
Amplitude-controlled phase shift oscillator circuit for Ex. 16-5.

Diode Stabilization Circuit for a Wein Bridge Oscillator

Figures 16-14, and 16-15 show two output amplitude stabilization methods that can be used with a Wein bridge oscillator. These can also be applied to other oscillator circuits, because they all operate by limiting the amplifier voltage gain.

The circuit in Fig. 16-14 uses diodes and operates in the same way as the amplitude control for the phase-shift oscillator. Resistor R_6 becomes shorted by the diodes when the output amplitude exceeds the design level, thus rendering the amplifier gain too low to sustain oscillations.

FET Stabilization Circuit for a Wein Bridge Oscillator

The circuit in Fig. 16-15 is slightly more complex than the diode circuit, however, like other circuits, it stabilizes the oscillator output amplitude by controlling the amplifier gain. The channel resistance (r_{DS}) of the *p*-channel *FET* (Q_1) is in parallel with resistor R_4. Capacitor C_3 ensures that Q_1 has no effect on the amplifier *dc* conditions. The amplifier voltage gain is,

$$A_{CL} = \frac{R_3 + R_4 \| r_{DS}}{R_4 \| r_{DS}} \qquad \textbf{(16-19)}$$

The *FET* gate-source bias voltage is derived from the amplifier *ac* output. The output voltage is divided across resistors R_5 and R_6.

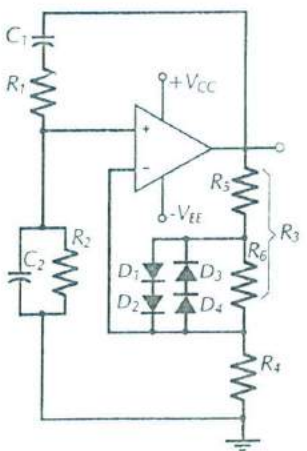


Figure 16-14
Wein bridge oscillator with its output amplitude stabilized by a diode circuit that modifies the amplifier gain.

and rectified by diode D_1. Capacitor C_4 smoothes the rectified waveform to give the *FET dc* bias voltage (V_{GS}) . The polarity shown on the circuit diagram reverse biases the gate-source of the *p*-channel device. When the output amplitude is low, V_{GS} is low and this keeps the *FET* drain-source resistance (r_{DS}) low. When the output gets larger, V_{GS} is increased causing r_{DS} to increase. The increase in r_{DS} reduces A_{CL}, thus preventing the circuit from oscillating with a high output voltage level. It is seen that the *FET* is behaving as a *voltage variable resistance* (*VVR*).

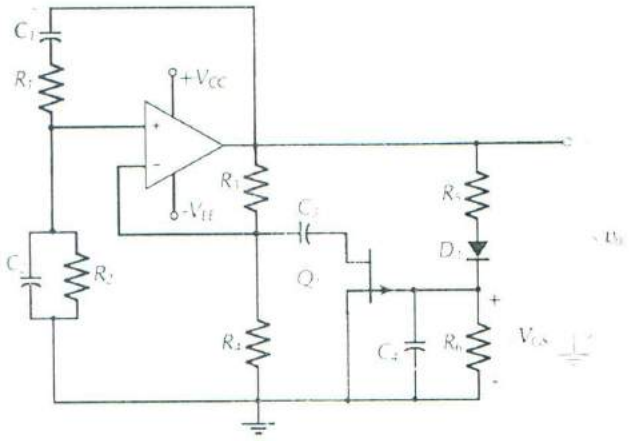


Figure 16-15
Wein bridge oscillator with the output amplitude stabilized by a FET voltage controlled resistance circuit.

Design of a FET Stabilization Circuit

To design the *FET* amplitude stabilization circuit, knowledge of a possibly suitable *FET* is required; in particular, the channel resistance at various gate-source voltages must be known.

Suppose the circuit is to oscillate when r_{DS} = 6 kΩ at V_{GS} = 1 V, and that the peak output is to be $V_{o(pk)}$ = 6 V. Resistors R_5 and R_6 should be selected to give V_{GS} = 1 V when $V_{o(pk)}$ = 6 V, allowing for V_F across the diode. Capacitor C_4 smoothes the half-wave rectified waveform, and discharges via R_6 during the time interval between peaks of the output waveform. The capacitance of C_4 is calculated to allow perhaps a 10% discharge during the time period of the oscillating frequency. The voltage divider current (I_5) should be a minimum of around 100 μA for satisfactory diode operation.

C_3 is a coupling capacitor; its impedance at the oscillating frequency should be much smaller than the r_{DS} of the *FET*. Resistors R_3 and R_4 are calculated using Eq. 16-19 to give the required amplifier voltage gain when r_{DS} = 6 kΩ.

Example 16-6

Design the *FET* output amplitude stabilization circuit in Fig. 16-16 to limit the output amplitude of the Wein bridge oscillator in Example 16-4 to ±6 V. Assume that the r_{ds} = 500 Ω at V_{GS} = 1 V, and 800 Ω at V_{GS} = 3 V.

Solution

Select $R_4 \approx r_{DS}$ at $V_{GS} = 1$ V

$\approx 600\ \Omega$ (use 560 Ω)

$R_4 \| r_{DS} = 560\ \Omega \| 600\ \Omega$

$\approx 290\ \Omega$

for $A_{CL} = 3$, $R_3 = 2\,(R_4 \| r_{DS}) = 2 \times 290\ \Omega$

$= 640\ \Omega$ (use 680 Ω)

Select, $I_5 \approx 200\ \mu$A when $V_{o(peak)} = 6$ V

$$R_6 = \frac{V_{GS}}{I_5} = \frac{1\text{ V}}{200\ \mu\text{A}}$$

$= 5$ kΩ (use 4.7 kΩ)

$$R_5 = \frac{V_{o(peak)} - (V_{GS} + V_{D1})}{I_5} = \frac{6\text{ V} - (1\text{ V} + 0.7\text{ V})}{200\ \mu\text{A}}$$

$= 21.5$ kΩ (use 22 kΩ)

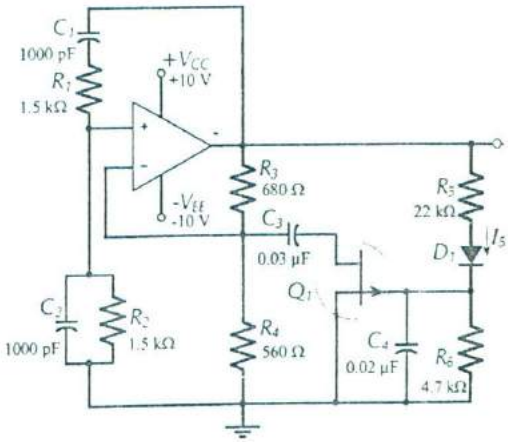


Figure 16-16
Wein bridge oscillator circuit for Example 16-6.

C_4 discharge voltage,

$$\Delta V_C = 0.1\ V_{GS} = 0.1 \times 1\text{ V} = 0.1\text{ V}$$

C_4 discharge time, $T = \frac{1}{f} = \frac{1}{100\text{ kHz}}$

$= 10\ \mu$s

$$I_C \approx \frac{V_{R6}}{R_6} \approx I_5 \approx 200\ \mu\text{A}$$

$$C_4 = \frac{I_C\,T}{\Delta V_C} = \frac{200\ \mu\text{A} \times 10\ \mu\text{s}}{0.1\text{ V}}$$

$= 0.02\ \mu$F (standard value)

$X_{C3} = \frac{r_{DS}}{10}$ at the oscillating frequency

$$C_3 = \frac{1}{2\pi f r_{DS}/10} = \frac{1}{2\pi \times 100\text{ kHz} \times 500\ \Omega/10}$$

$= 0.032\ \mu$F (use 0.03 μF)

D_1 should be a low current switching diode with a $t_{rr} << T$.

Practise Problems

16-5.1 An op-amp phase shift oscillator is to produce a 3.3 kHz, ±7 V output. Design the circuit to use diode amplitude stabilization.

16-5.2 Modify the Wein bridge oscillator circuit in Ex. 16-4 to stabilize the output amplitude to ±5 V. Use the diode circuit in Fig. 16-14.

16-6 Square Wave Generator

A *square wave generator* can be constructed by adding a resistor and capacitor to an inverting Schmitt trigger circuit (see Section 14-10). Figure 16-17 shows the circuit, which is also known as an *astable multivibrator*. The operational amplifier together with resistors R_2 and R_3 constitute the inverting Schmitt trigger circuit. Capacitor C_1 controls the voltage at the Schmitt input, and resistor R_1 charges and discharges C_1 from the Schmitt output.

The circuit waveforms in Fig. 16-17 illustrate the square wave generator operation. When the output is *high* (at the op-amp output saturation level), current flows through R_1 charging C_1 positively until v_{C1} equals the Schmitt *UTP*. The Schmitt output then switches to the op-amp negative saturation level. Current now commences to flow out of the capacitor via R_1, causing v_{C1} to decrease until it arrives at the *LTP* of the Schmitt circuit. At this point, the Schmitt output switches to its positive level once again, and the cycle recommences.

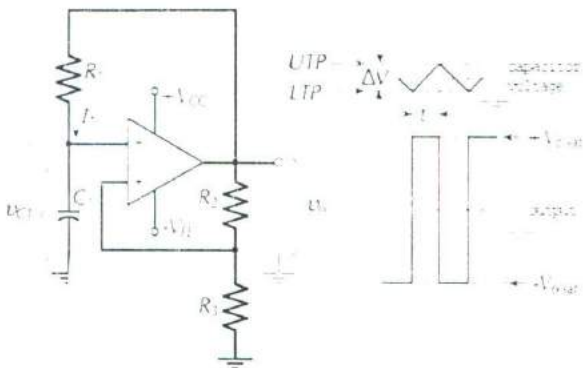


Figure 16-17
Square wave generator consisting of an inverting Schmitt trigger circuit and a series RC circuit.

Design of this very simple square wave generator involves design of the Schmitt trigger circuit, and determination of suitable R_1 and C_1 values for the trigger voltage levels and the required charge and discharge times. Selecting the *UTP* and *LTP* very much smaller than the op-amp output levels keeps the voltage drop across R_1 approximately constant. This means that the capacitor charging current is also maintained fairly constant, and so the simple constant-current equation can be used for the capacitor:

$$C_1 = \frac{I_1 \times t}{\Delta V} \qquad \textbf{(16-20)}$$

In Eq. 16-20, I_1 is the average charging current to the capacitor (through R_1), t is the charging time (see Fig. 16-17), and ΔV is the capacitor voltage change between the *UTP* and *LTP*, as illustrated. Charging current I_1 should be selected much larger than the op-amp input bias current; then R_1 and C_1 are calculated. Alternatively, a convenient value of C_1 can first be selected. The level of I_1 is then determined from Eq. 16-20.

If a Schmitt trigger circuit with a large difference between the *UTP* and *LTP* is used, the capacitor changing equation[1] is,

$$e_c = E - (E - E_o)\varepsilon^{-t/RC} \qquad \textbf{(16-21)}$$

Example 16-7

Design the square wave generator in Fig. 16-18 to produce a 1 kHz square wave with an amplitude of approximately ±14 V. Use a *741* op-amp.

Solution

$$V_{CC} \approx \pm(V_o + 1\text{ V}) \approx \pm(14\text{ V} + 1\text{ V})$$
$$\approx \pm 15\text{ V}$$

$$V_{R3} = UTP = -LTP << V_{CC}$$

Select $V_{R3} \approx 0.5$ V

Select $I_2 \approx 100 \times I_{B(max)} = 100 \times 500\text{ nA}$
$= 50\,\mu\text{A}$

$$R_3 = \frac{V_{R3}}{I_2} = \frac{0.5\text{ V}}{50\,\mu\text{A}}$$
$$= 10\text{ k}\Omega \text{ (standard value)}$$

$$R_2 = \frac{V_o - V_{R3}}{I_2} = \frac{14\text{ V} - 0.5\text{ V}}{50\,\mu\text{A}}$$
$$= 270\text{ k}\Omega \text{ (standard value)}$$

$$t = \frac{T}{2} = \frac{1}{2f} = \frac{1}{2 \times 1\text{ kHz}}$$
$$= 0.5\text{ ms}$$

$$\Delta V = UTP - LTP = 0.5\text{ V} - (-0.5\text{ V})$$
$$= 1\text{ V}$$

Select $C_1 = 0.1\,\mu$F (convenient value)

From Eq. 16-20, $I_1 = \frac{C_1 \Delta V}{t} = \frac{0.1\,\mu\text{F} \times 1\text{ V}}{0.5\text{ ms}}$
$= 200\,\mu\text{A}$

$V_{R1(ave)} \approx 14$ V

$$R_1 = \frac{V_{R1}}{I_1} = \frac{14\text{ V}}{200\,\mu\text{A}}$$
$$= 70\text{ k}\Omega \text{ (use 68 k}\Omega \text{ standard value)}$$

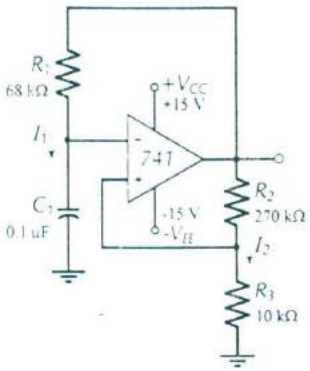


Figure 16-18
Square wave generator circuit for Example 16-7.

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[1] David A. Bell, *Solid State Pulse Circuits 4th ed.*, (1997) p. 33.

Practise Problems

16-6.1 The square wave generator designed in Example 16-7 is to be modified to make the output frequency adjustable. Determine the maximum and minimum values for R_1 to produce a frequency range of 500 Hz to 5 kHz.

16-6.2 A Schmitt trigger circuit with ±0.8 V trigger points and a ±9 V supply is to be used in a 9 kHz square wave generator (as in Fig. 16-17). Determine suitable R_1 and C_1 values.

16-7 Triangular Wave Generator

Integrator

The circuit in Fig. 16-19 is an *integrator*: its output amplitude can be shown to be directly proportional to the area of the input pulse (amplitude x time). The circuit is simiar to an op-amp inverting amplifier, except that capacitor C_1 replaces the resistor usually connected between the output and inverting input terminals. As in the case of the inverting amplifier, the op-amp inverting input terminal remains at ground level (a virtual ground) because the noninverting input is grounded. The output voltage depends upon the capacitor charge:

$$V_o = V_{C1}$$

If the capcitor charge is $V_{C1} = 0$, then the output is $V_o = 0$. If $V_{C1} = -1$ V (negative on the right, as illustrated), $V_o = -1$ V. If $V_{C1} = +1$ V (positive on the right), $V_o = +1$ V.

The circuit input current is,

$$I_1 = \frac{V_i}{R_1}$$

With V_i constant, I_1 is a constant current flowing into C_1. The capacitor constant current charging equation can be used to calculate the capacitor voltage:

$$V_{C1} = \frac{I_1 t}{C_1}$$

or,

$$\boldsymbol{V_o = \frac{I_1 t}{C_1}} \qquad \textbf{(16-22)}$$

In Eq. 16-22, t is the time duration of I_1, or the input pulse width, as illustrated in Fig. 16-19.

When the input voltage is positive ($+V_i$), I_1 is a positive quantity flowing through R_1 and into C_1 in the direction shown on the circuit diagram. This causes C_1 to charge, positive on the left, negative on the right, as illustrated. With the input voltage constant, I_1 is a constant current, and V_o increases constantly in a negative direction, as shown. When the polarity of the input

voltage is reversed (to $-V_i$), the direction of I_1 is reversed, and the charging direction of C_1 is also reversed. Thus, V_o commences to grow in a positive direction. So, a square wave input to the integrating circuit produces a triangular wave output, as illustrated.

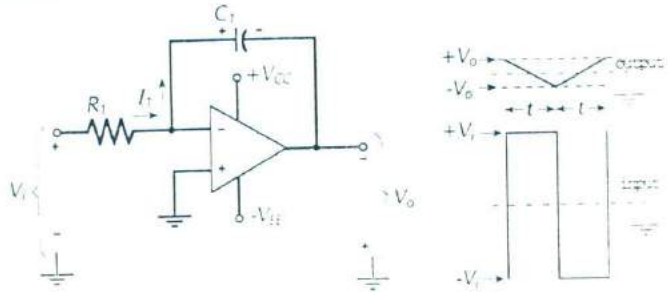


Figure 16-19
An integrator circuit produces a triangular waveform output from a square wave input.

Integrator Combined with Schmitt Trigger

Figure 16-20 shows an integrator combined with a noninverting Schmitt trigger circuit, (see Section 14-10). As will be explained, this combination constitutes a *triangular waveform generator*. The Schmitt trigger output is applied to the integrator input, and the integrator output functions as the Schmitt circuit input. The waveforms illustrate the operation of the circuit.

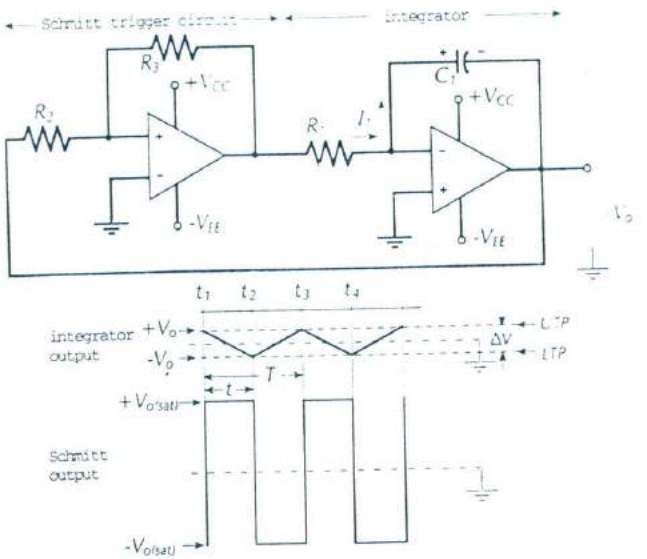


Figure 16-20
Triangular waveform generator consisting of a noninverting Schmitt trigger circuit and an integrator. The Schmitt output is the integrator input, and the integrator output is applied as the Schmitt input.

During the time from instant t_1 to instant t_2, the Schmitt output is positive (at $+V_{o(sat)}$), and the integrater output is changing at a constant rate in a negative-going direction. The output change is ΔV; from $+V_o$ to $-V_o$. The Schmitt circuit is designed to have upper and lower trigger points (*UTP* and *LTP*) equal to the desired levels of $+V_o$ and $-V_o$. Thus, when the integrator output arrives at the *LTP*,

the Schmitt output (the integrator *input*) switches from $+V_{o(sat)}$ to $-V_{o(sat)}$. The integrator input is now a constant negative voltage, so that the integrator output direction is reversed. From t_2 to t_3, the integrator output increases linearly from $-V_o$ to $+V_o$, that is from the Schmitt *LTP* to its *UTP*. At the *UTP* the Schmitt output reverses again, causing the integrator output to reverse direction once more. The cycle repeats again and again producing a triangular waveform at the integrator output terminal.

The frequency of the triangular output wave can be varied by altering the charging rate of capacitor C_1. This is done by making R_1 adjustable, so that I_1 can be increased or decreased. Reducing the resistance of R_1 increases the level of I_1 and causes C_1 to be charged faster. This reduces the time (t) between $+V_o$ and $-V_o$, and thus increases the output frequency. An increase in the resistance of R_1 reduces I_1, increases t, and results in a lower output frequency. The output amplitude of the triangular wave can be varied by altering the Schmitt *UTP* and *LTP*. This can be done by making one of the Schmitt resistors (R_2 or R_3) partially adjustable.

Circuit Design

A waveform generator is normally designed to produce a specified output amplitude and frequency. This means that the Schmitt Circuit trigger points must be equal to the required positive and negative output peaks of the triangular wave, (see Section 14-10). Also, the integrator has to accept the Schmitt output as its input, and its capacitor charging time should equal half the time period of the specified output frequency. Resistor R_1 might be made partially variable to precisely set the output to the required frequency.

Example 16-8

Design a triangular waveform generator to produce a ±3 V, 500 Hz output. Use *741* op-amps with a ±9 V supply.

Solution

Integrator design:

$$V_i \approx \pm(V_{CC} - 1\text{ V}) = \pm(9\text{ V} - 1\text{ V})$$
$$= \pm 8\text{ V}$$

$$\Delta V = +V_o - (-V_o) = 3\text{ V} - (-3\text{V})$$
$$= 6\text{ V}$$

$I_1 >> I_{B(max)}$ for the op-amp

select, $I_1 = 1$ mA

$$R_1 = \frac{V_i}{I_1} = \frac{8\text{ V}}{1\text{ mA}}$$
$$= 8\text{ k}\Omega \text{ (use } 8.2\text{ k}\Omega$$

$$t = \frac{1}{2f} = \frac{1}{2 \times 500\ \text{Hz}}$$

$$= 1\ \text{ms}$$

from Eq. 16-22. $$C_1 = \frac{I_1 t}{\Delta V} = \frac{1\ \text{mA} \times 1\ \text{ms}}{6\ \text{V}}$$

$$= 0.16\ \mu\text{F}\ \text{(use 0.15 standard value)}$$

Schmit design:

select, $I_2 = 1\ \text{mA}$

$$R_2 = \frac{UTP}{I_2} = \frac{3\ \text{V}}{1\ \text{mA}}$$

$$= 3\ \text{k}\Omega\ \text{(use 3.3 k}\Omega\text{)}$$

$$R_3 = \frac{V_1}{I_2} = \frac{8\ \text{V}}{1\ \text{mA}}$$

$$= 8\ \text{k}\Omega\ \text{(use 8.2 k}\Omega\text{)}$$

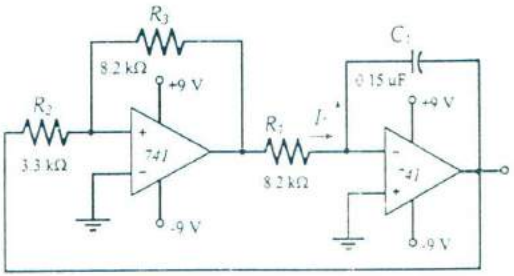


Figure 16-21
Triangular waveform generator designed in Ex. 16-8.

Practise Problems

16-7.1 A triangular waveform generator circuit (as in Fig. 16-21) has the following component values: $R_1 = 4.7\ \text{k}\Omega$, $R_2 = 3.9\ \text{k}\Omega$, $R_3 = 22\ \text{k}\Omega$, $C_1 = 0.05\ \mu\text{F}$. If the supply is $V_{CC} = \pm 12\ \text{V}$ determine the amplitude and frequency of the output.

16-7.2 Design a triangular wave generator to have $V_o = \pm 2.5\ \text{V}$, and an output frequency adjustable from 200 Hz to 400 Hz. Use *741* op-amps with $V_{CC} = \pm 15\ \text{V}$.

16-8 Oscillator Frequency Stabilization

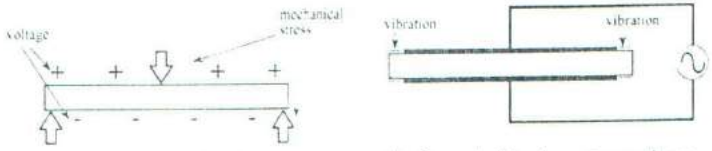
Frequency Stability

The output frequency of oscillator circuits is normally not as stable as required for a great many applications. The component values all have tolerances, so that the actual oscillating frequency may easily be 10% higher or lower than the desired frequency. However, by making a capacitor or resistor partially adjustable, the frequency of most oscillator circuits can be set fairly precisely. Such adjustments may not be convenient in production circuits.

A further problem is that component values vary with the changes in temperature, and this causes changes in oscillating frequency. The component temperature changes might be due to variations in the ambient temperature, or the result of component power dissipation. A well-designed circuit (of any type) normally uses as little power as possible to avoid component heating and to reduce the power supply load. Oscillator frequency stability can be dramatically improved by the use of *piezoelectric crystals*.

Piezo Electric Crystals

If a mechanical stress is applied to a wafer of quartz crystal, a voltage proportional to the pressure appears at the surfaces of the crystal, [see Fig. 16-22(a)]. Also, the crystal vibrates, or *resonates*, when an alternating voltage with the natural resonance frequency of the crystal is applied to its surfaces, [Fig. 16-22(b)]. All materials with this property are termed *piezoelectric*. Because the crystal resonance frequency is extremely stable, piezoelectric crystals are used to stabilize the frequency of oscillators.



(a) Crystal with mechanical stress (b) Crystal with alternating voltage

Figure 16-22
A piezoelectric crystal under stress produces a surface voltage. It also vibrates when an ac voltage is applied to its surfaces.

Quartz crystals for electronics applications are cut from the natural material in several different shapes. The crystals are ground to precise dimensions, and silver or gold electrodes are plated on opposite sides for electrical connections. The crystal is usually mounted inside a vacuum-sealed glass envelope or in a hermetically-sealed metal can. Figure 16-23 shows a typical crystal contained in a metal can enclosure. Crystals are also available in surface-mount and other types of enclosures.

Crystals Equivalent Circuit

The electrical equivalent circuit for a crystal is shown in Fig. 16-24(a). The crystal behaves as a series *RLC* circuit (R_s, L_s, C_s) in parallel with the capacitance of the connecting terminals (C_p). The series *RLC* components are referred to as the *motional resistance* (R_s), the *motional inductance* (L_s), and the *motional capacitance* (C_s), because they represent the piezoelectric performance of the crystal.

C_p is sometimes referred to as a *parasitic capacitance*. Because of the presence of C_p, the crystal has a *parallel resonance frequency* (f_p) when C_p resonates with the series circuit reactance, as well as a *series resonance frequency* (f_s), when L_s and C_s resonate. At series resonance the device impedance is reduced to R_s, and at parallel resonance the impedance is very high.

Figure 16-24(b) shows that, like all *RLC* circuits, the impedance of the crystal equivalent circuit is capacitive below the series resonance frequency and inductive above f_s. At frequencies greater than f_s, the series *RLC* circuit becomes inductive until it resonates with the parallel capacitance at f_p. The impedance of the complete circuit then becomes capacitive (with increasing frequency) as the reactance of C_p is reduced. The two resonance frequencies (f_s and f_p) are very close together.

A measure of the quality of a resonance circuit is the ratio of reactance to resistance, termed the *Q factor*. Because the resistive component of the crystal equivalent circuit is relatively small,

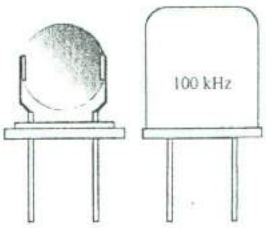
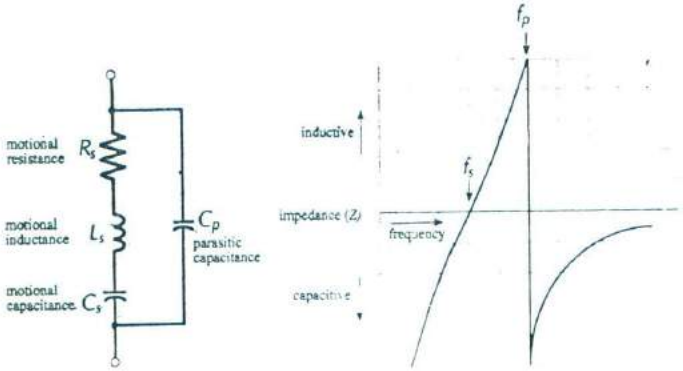


Figure 16-23
Electronic crystal contained in a metal can.

crystals have very large Q factors. Crystal Q factors range approximately from 2000 to 100 000, compared to a maximum of about 400 for an actual LC circuit. Resonance frequencies of available crystals are typically 10 kHz to 200 MHz.



(a) Crystal equivalent circuit (b) Crystal impedance/frequency graph

Figure 16-24
The equivalent circuit for a piezoelectric crystal is a series RLC with a parallel capacitance. The circuit has two resonance frequencies: if $_s$ and if $_p$.

When a series LRC circuit is operating at its resonance frequency the inductive and capacitive reactances cancel each other, and the power supplied is dissipated in the resistance. If the power dissipation increases the temperature of a crystal, the resonance frequency can drift by a small amount. Most crystals maintain their frequency to within a few cycles of the resonance frequency at 25°C. For greater frequency stability, crystals are sometimes enclosed in an insulated, thermostatically controlled, *crystal oven*.

Crystals Control of Oscillators

The frequency of an oscillator may be stabilized by using a crystal operating at either its series or parallel resonance frequency. The circuit is then usually referred to as a *crystal oscillator*.

In many circuits the crystal is connected in series with the feedback network. The crystal offers a low impedance at its series resonance and a high impedance at all other frequencies, so that oscillation occur only at the crystal series resonance frequency. The *Pierce oscillator* in Fig. 16-25 would appear to be such a circuit, however, it actually operates as a Colpitts oscillator. Capacitors C_1 and C_2 are present at the input and output of the inverting amplifier [compare to Fig. 16-6(a)]. A Colpitts oscillator also has an inductor connected between the amplifier input and output. In Fig. 16-25 the crystal behaves as an inductance by operating at a frequency slightly above f_s, (see Fig. 16-24).

The circuit in Fig. 16-25 is often used as a square wave generator or *clock oscillator* for digital circuit applications. In this situation, the amplifier gain is made as large as possible, so that Q_1 is driven between saturation and cutoff to produce a square wave output.

Figure 16-26 shows one method of modifying a Wein Bridge oscillator for frequency stabilization. The crystal is connected in

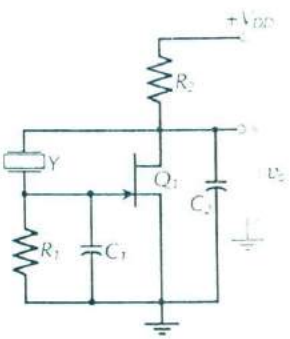


Figure 16-25
Pierce oscillator circuit using a crystal that operates at its series resonance frequency.

series with C_1 and R_1, and in this situation it offers a low resistance at its series resonance frequency (f_s), and a relatively high impedance at all other frequencies. Feedback voltage from the output via C_1 and R_1 is severely attenuated at all frequencies except f_s, so the circuit can oscillate only at f_s.

A crystal-controlled Wein bridge oscillator circuit is first designed without the crystal. A crystal is selected with f_s equal to the desired frequency. Then, the circuit is modified by subtracting the crystal series resonance resistance (R_s) from the calculated value of the series resistor, (R_1 in Fig. 16-26). Alternatively, circuit design could start by selection of a crystal. R_1 is then made larger than R_s, and $R_2 = (R_1 + R_s)$. C_1 and C_2 are calculated from f_s and R_2.

The crystal power dissipation must be kept below the specified maximum. Too much power can overheat the crystal and cause drift in the resonance frequency. Also, like other devices, too much power dissipation can destroy a crystal. Typical maximum crystal drive powers are 1 mW to 10 mW, but manufacturers usually recommend operating at 1/10 of the specified maximum.

The *dc* insulation resistance of crystals ranges from 100 MΩ to 500 MΩ. This allows them to be directly connected into a circuit without the need for coupling capacitors. Care must be taken in any crystal oscillator circuit to ensure that the crystal does not interrupt the flow of a necessary direct current.

The typical frequency stability of oscillators that do not use crystals is around 1 in 10^4. This means, for example, that the frequency of a 1 MHz oscillator might be 100 Hz higher or lower than 1 MHz. Using a crystal, the frequency stability can be improved to better than 1 in 10^6, which gives a ±1 Hz variation in the output of a 1 MHz oscillator.

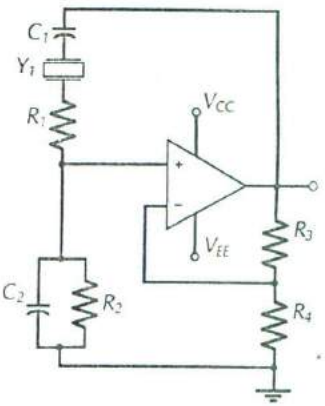


Figure 16-26
Use of a series-connected crystal to stabilize the frequency of a Wein bridge oscillator circuit.

Example 16-9

Redesign the Wein bridge oscillator in Example 16-4 to use a 100 kHz crystal with R_S = 1.5 kΩ.

Solution

select $R_1 = 2R_s = 2 \times 1.5\ \text{k}\Omega$
$= 3\ \text{k}\Omega$ (use 2.7 kΩ standard value)

$R_2 = R_1 + R_s = 2.7\ \text{k}\Omega + 1.5\ \text{k}\Omega$
$= 4.2\ \text{k}\Omega$ (use 3.9 kΩ standard value)

From Eq. 16-13, $C_1 = \dfrac{1}{2\pi f R_2} = \dfrac{1}{2\pi \times 100\ \text{kHz} \times 3.9\ \text{k}\Omega}$
$= 408\ \text{pF}$ (use 390 pF standard value)

$R_4 \approx R_2 = 3.9\ \text{k}\Omega$ (standard value)

$R_3 = 2R_4 = 2 \times 3.9\ \text{k}\Omega$
$= 7.8\ \text{k}\Omega$ (use 8.2 kΩ standard value)

Example 16-10

The Pierce oscillator in Fig. 16-27 has a crystal with f_s = 1 MHz and R_s = 700 Ω. Calculate the inductance offered by the crystal at the circuit oscillating frequency. Also, estimate the power dissipated in the crystal.

Solution

eq. 16-5, $$C_T = \frac{C_1 \times C_2}{C_1 + C_2} = \frac{1000\ \text{pF} \times 100\ \text{pF}}{1000\ \text{pF} + 100\ \text{pF}}$$

$$= 90.9\ \text{pF}$$

at resonance, $$X_L = X_{CT}$$

$$2\pi f L = \frac{1}{2\pi f C_T}$$

or, $$L = \frac{1}{(2\pi f)^2 C_T} = \frac{1}{(2\pi \times 1\ \text{MHz})^2 \times 90.9\ \text{pF}}$$

$$= 279\ \mu\text{H}$$

$$i_p = \frac{V_{DD}}{R_1 + R_2 + R_s} = \frac{5\ \text{V}}{1\ \text{M}\Omega + 10\ \text{k}\Omega + 700\ \Omega}$$

$$\approx 5\ \mu\text{A}$$

$$P_D = (0.707\, i_p)^2 R_s = (0.707 \times 5\ \mu\text{A})^2 \times 700\ \Omega$$

$$= 9\ \text{nW}$$

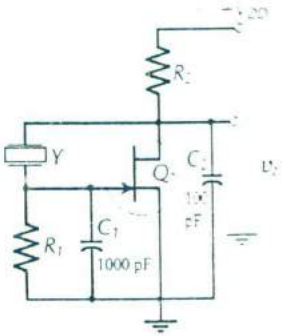


Figure 16-27
Crystal oscillator circuit for Example 16-10.

Practise Problems

16-8.1 A 40 kHz crystal with R_s = 3 kΩ is to be used with the Colpitts oscillator in Fig. 16-5. Determine the necessary circuit modifications and estimate the peak power dissipation in the crystal.

16-8.2 A Pierce oscillator (as in Fig. 16-27) has a crystal with L = 500 μH at f_s = 1 MHz. Select suitable capacitor values and calculate the minimum amplifier voltage gain.

16-8.3 Design a 50 kHz, crystal controlled, Wein bridge oscillator to use a crystal with R_s = 2 kΩ. The available supply voltage is V_{CC} = ±12 V. Specify the op-amp bandwidth.

Chapter-16 Review Questions

Section 16-1

16-1 State the Barkhausen criteria for a sinewave oscillator, and explain why they must be fulfilled to sustain oscillations.

16-2 Draw the circuit diagram of an op-amp phase shift oscillator. Sketch the circuit waveforms, and briefly explain the oscillator operation.

16-3 Write the oscillating frequency equation for a phase shift oscillator. Discuss the phase shift network attenuation and the amplifier gain requirements.

16-4 Sketch the circuit diagram for a phase shift oscillator that uses a single-stage *BJT* amplifier. Briefly explain the circuit operation.

Section 16-2

16-5 Draw the circuit diagram of an op-amp Colpitts oscillator. Sketch the oscillator waveforms, and briefly explain the circuit operation.

16-6 Write the frequency equation for a Colpitts oscillator. Discuss the phase shift network attenuation and the amplifier gain requirements.

16-7 Sketch circuit diagrams for a Colpitts oscillator using a single-stage *BJT* amplifier. Briefly explain the circuit operation.

Section 16-3

16-8 Draw the circuit diagram of an op-amp Hartley oscillator. Sketch the oscillator waveforms, and explain the circuit operation.

16-9 Write the frequency equation for a Hartley oscillator. Discuss the phase shift network attenuation and the amplifier gain requirements.

16-10 Sketch circuit diagrams for a Hartley oscillator using a single-stage *BJT* amplifier. Briefly explain the circuit operation.

Section 16-4

16-11 Draw the circuit diagram of an op-amp Wein bridge oscillator. Sketch the oscillator waveforms, and explain the circuit operation.

16-12 Write the frequency equation for a Wein bridge oscillator. Discuss the phase shift network attenuation and the amplifier gain requirements.

Section 16-5

16-13 Show how the output amplitude of a phase shift oscillator can be stabilized by means of a diode circuit. Explain the circuit operation.

16-14 Sketch a diode amplitude stabilization circuit for a Wein bridge oscillator, and explain its operation.

16-15 Draw a *FET* circuit diagram for stabilizing the output amplitude of a Wein Bridge oscillator. Explain the circuit operation.

Section 16-6

16-16 Draw the circuit diagram of a square wave generator that uses an inverting Schmitt trigger circuit. Sketch the circuit waveforms, and explain its operation.

Section 16-7

16-17 Sketch an op-amp integrating circuit together with the circuit waveforms. Explain the circuit operation.

16-18 Draw the circuit diagram of a triangular waveform generator that uses an integrator circuit and a noninverting Schmitt trigger. Sketch the waveforms and explain the circuit operation.

16-19 Discuss how the output amplitude and frequency can be made adjustable in a triangular wave generator.

Section 16-8

16-20 Describe a piezoelectric crystal as used with electronic circuits. Sketch the crystal equivalent circuit and impedance/frequency graph. Explain the behaviour of electronic crystals.

16-21 Show how piezoelectric crystals are employed for oscillator stabilization. Explain.

Chapter-16 Problems

Section 16-1

16-1 Design a phase shift oscillator to have a 3 kHz output frequency. Use a *741* op-amp with $V_{CC} = \pm 12$ V.

16-2 A phase shift oscillator is to use three 0.05 μF capacitors and an op-amp with $V_{CC} = \pm 9$ V. Design the circuit to have $f = 7$ kHz. Select a suitable operation amplifier.

16-3 Redesign the circuit in Problem 16-1 to use a single-stage *BJT* amplifier. Use a *2N3904* transistor with $V_{CC} = 15$ V.

16-4 The phase shift oscillator circuit in Fig. 16-1 has the following component values: $R_1 = 3.9$ kΩ, $R_2 = 120$ kΩ, $R_3 = 120$ kΩ, $R = 3.9$ kΩ, $C = 0.025$ μF. Calculate the circuit oscillating frequency.

16-5 Determine new capacitor values for the phase shift oscillator in Problem 16-1 to switch its frequency to (a) 700 Hz, (b) 5 kHz.

Section 16-2

16-6 Using a *741* op-amp with $V_{CC} = \pm 10$ V, design a Colpitts oscillator to have a 30 kHz oscillating frequency.

16-7 Design a Colpitts oscillator to have $f = 55$ kHz, and to use a 20 mH inductor and a *741* op-amp with $V_{CC} = \pm 18$ V.

16-8 The Colpitts oscillator circuit in Fig. 16-4 has: R_1 = 18 kΩ, R_2 = 180 kΩ, R_3 = 18 kΩ, L = 75 mH, C_1 = 3000 pF, and C_2 = 300 pF. Calculate the circuit oscillating frequency.

16-9 Design a 20 kHz Colpitts oscillator using a 10 mH inductor and a single-stage *BJT* amplifier. Use a *2N3904* transistor with V_{CC} = 20 V.

Section 16-3

16-10 Design a 6 kHz Hartley oscillator circuit to use a *741* op-amp, and an inductor with L_1 = 10 mH and L_2 = 100 mH.

16-11 Calculate the oscillating frequency for the Hartley oscillator in Fig. 16-7 if the components are: R_1 = 3.3 kΩ, R_2 = 56 kΩ, R_3 = 3.3 kΩ, L_1 = 3 mH, L_2 = 50 mH, and C_1 = 1500 pF.

16-12 An op-amp Hartley oscillator has two inductors with L_1 = 5 mH, L_2 = 40 mH, and a total inductance of L_T = 50 mH. Determine the capacitor value to give f = 2.25 kHz. Also, calculate the required amplifier voltage gain.

Section 16-4

16-13 Design a 15 kHz Wein bridge oscillator to use an op-amp with V_{CC} = ±14 V. Specify the operational amplifier.

16-14 A Wein bridge oscillator uses two 5000 pF capacitors and a *741* op-amp with V_{CC} = ±12 V. Complete the circuit design to produce a 9 kHz output frequency.

16-15 The Wein bridge oscillator in Fig. 16-10 has the following components: R_1 = R_2 = R_4 = 5.6 kΩ, R_3 = 12 kΩ, C_1 = C_2 = 2700 pF. Calculate the oscillating frequency.

16-16 The oscillator in Problem 16-15 has its capacitors changed to 0.05 μF, and resistors R_1 and R_2 are adjustable from 4.7 kΩ to 6.7 kΩ. Calculate the maximum and minimum output frequencies.

Section 16-5

16-17 The phase shift oscillator in Problem 16-1 is to have its output amplitude stabilized to ±7 V. Design a suitable diode amplitude stabilization circuit.

16-18 Design a diode amplitude stabilization circuit to limit the output of the Wein bridge oscillator in Example 16-4 to a maximum of ±4 V.

16-19 Design a 3 kHz Wein bridge oscillator using a diode circuit to stabilize the output to ±10 V. A ±20 V supply is to be used, and a suitable op-amp is to be selected.

16-20 Modify the circuit for Problem 16-19 to use a *FET* stabilization circuit, as in Fig. 16-15. Use a *FET* with r_{DO} = 200 Ω at V_{GS} = 3 V, and r_{DS} = 600 Ω at V_{GS} = 5 V.

Section 16-6

16-21 The square wave generator circuit in Fig. 16-17 has the following quantities: R_1 = 33 kΩ, R_2 = 56 kΩ, R_3 = 2.2 kΩ, C_1 = 0.15 μF, V_{CC} = ±12 V. A rail-to-rail op-amp is used. Determine the output amplitude and frequency.

16-22 Design a square wave generator circuit (as in Fig. 16-17) to produce a 3 kHz, ±9 V output. Select a suitable op-amp.

16-23 A square wave generator circuit is to use a *BIFET* op-amp with V_{CC} = ±18 V. Design the circuit to produce an output frequency adjustable from 500 Hz to 5 kHz.

16-24 Modify the circuit designed for problem 16-22 to make the output adjustable from 2.5 kHz to 3.5 kHz.

Section 16-7

16-25 Design a triangular waveform generator to produce a ±1 V, 1 kHz output. Use *741* op-amps with V_{CC} = ±12 V.

16-26 Modify the circuit designed for Problem 16-25 to make the output adjustable from 500 Hz to 1.5 kHz.

16-27 Determine the amplitude and frequency of the output from a triangular waveform generator (as in Fig. 16-20) that has the following components and supply voltage: R_1 = 10 kΩ, R_2 = 3.9 kΩ, R_3 = 22 kΩ, C_1 = 0.5 μF, V_{CC} = ±12 V.

16-28 Determine the output frequency range from the circuit in Problem 16-27 if R_1 is replaced with a 4.7 kΩ resistor in series with a 10 kΩ potentiometer.

Section 16-8

16-29 The oscillating frequency of the Hartley oscillator circuit in Fig. 16-8 is to be stabilized by means of a 100 kHz crystal with R_S = 700 Ω. Determine the necessary modifications, and estimate the peak power dissipation in the crystal.

16-30 Select suitable capacitor values for a Pierce oscillator (as in Fig. 16-27) that uses a 3 MHz crystal. The crystal has L = 390 μH at the oscillating frequency.

16-31 A 200 kHz crystal with R_S = 700 Ω is used in the Wein bridge oscillator circuit in Fig. 16-26. Design the circuit using A_{CL} = 3 for the amplifier. Assume that V_{CC} = ±15 V and that the output is limited to ±5 V.

Practise Problem Answers

16-1.1 10 kΩ, 10 kΩ, 330 kΩ, 1000 pF

16-1.2 V_{CC} = 18 V, R_1 = (56 kΩ + 2.2 kΩ), R_2 = 27 kΩ, R_C = 3.3 kΩ, $(R - Z_{in})$ = 1.8 kΩ, R = 3.3 kΩ, C = (0.15 μF||2000 pF), C_E = 75 μF

16-2.1 12 kΩ, 120 kΩ, 12 kΩ, 0.01 μF, 220 mH, 1000 pF, ±12 V

16-2.2 V_{CC} = 15 V, R_1 = (68 kΩ + 8.2 kΩ), R_2 = 47 kΩ, R_C = 4.7 kΩ, R_E = 4.7 kΩ, C_1 = 0.06 μF, C_2 = 6000 pF, C_C = 0.05 μF, C_E = 3 μF

16-3.1 ±12 V, 1 kΩ, 10 kΩ, 1 kΩ, 2.2 mH, 22 mH, 0.02 μF
16-3.2 66.3 kHz
16-4.1 10.6 kHz, 28.4 kHz
16-4.2 10 kΩ, 2.2 kΩ, 27 kΩ, 2.2 kΩ, 1000 pF, 5000 pF
16-5.1 220 Ω, 5.6 kΩ, 1.5 kΩ, 2 kΩ, 3.9 kΩ, 220 Ω, 0.082 μF
16-5.2 1.5 kΩ, 2.2 kΩ, 1.5 kΩ
16-6.1 12 kΩ, 150 kΩ
16-6.2 0.1 μF, 2.7 kΩ
16-7.1 ±1.42 V, 6.13 kHz
16-7.2 (6.8 kΩ + 10 kΩ pot.), 0.5 μF, 2.2 kΩ, 12 kΩ
16-8.1 Crystal in series with R_1 = 22 kΩ, 2.8 μW
16-8.2 270 pF, 62 pF, 4.4
16-8.3 3.9 kΩ, 5.6 kΩ, 560 pF, 560 pF, 12 kΩ, 5.6 kΩ, 150 kHz

Chapter 17
Linear and Switching Voltage Regulators

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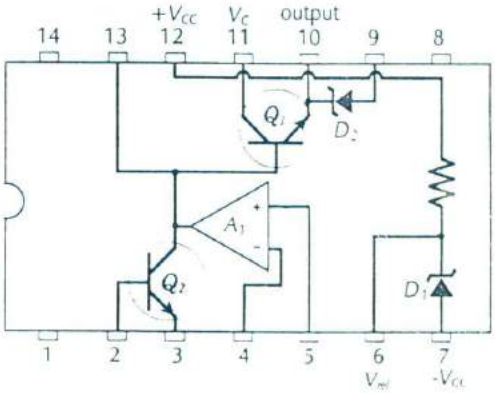
Problems 601
Practise Problem Answers 604



Objectives

You will be able to:

1. Sketch transistor series regulator circuits, and explain their operation.
2. Show how regulator circuits may be improved by the use of error amplifiers, additional series-pass transistors, preregulation etc., and how the output voltage may be adjusted.
3. Design transistor series regulators circuits to fulfil a given specification.
4. Analyze transistor series regulators to determine source effect, load effect, line regulation, load regulation, and ripple reduction.
5. Sketch operational amplifier series regulator circuits, and explain their operation.
6. Design op-amp series regulators circuits to fulfil a given specification.
7. Sketch and explain the basic circuit of a 723 IC voltage regulator, and design circuits using 723 ICs.
8. Sketch IC regulator block diagrams, and determine external component values for various applications.
9. Sketch the block diagram and waveforms for a switching regulator, and explain its operation.
10. Sketch circuits and waveforms for step-down, step-up, and inverting converters, and explain their operation.
11. Design LC filter circuit for various switching converters.
12. Show how an IC controller circuit is used with switching converters, and calculate values for the externally-connected components.

Introduction

Almost all electronic circuits require a direct voltage supply. This is usually derived from the standard industrial or domestic *ac* supply by transformation, rectification, and filtering. The resultant *raw dc* is not stable enough for most purposes, and it usually contains an unacceptably large *ac* ripple waveform. Voltage regulator circuit are employed to render the voltage more constant and to attenuate the ripple.

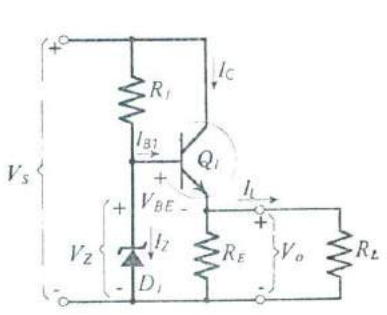
Unregulated power supplies and Zener diode regulators are discussed in Chapter 3. Zener diode regulators are normally used only where the load current does not exceed 25 mA. A transistor operating as an emitter follower circuit may be connected to a Zener diode regulator to supply larger load currents. The regulator circuit performance is tremendously improved when an *error amplifier* is included, to detect and amplify the difference between the output and the voltage reference source, and to provide feedback to correct the difference.

A variety of voltage regulator circuits are available in integrated circuit form.

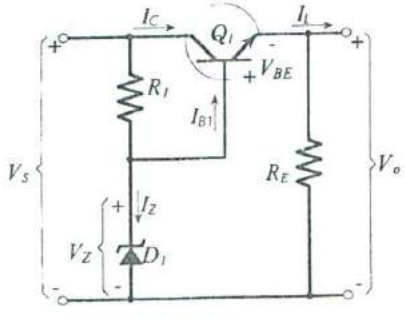
17-1 Transistor Series Regulator

Basic Circuit

When a low-power Zener diode is used in the simple regulator circuit described in Section 3-6, the load current is limited by the maximum diode current. A high-power Zener used in such a circuit can supply higher levels of load current, but much power is wasted when the load is light. The emitter follower regulator shown in Fig. 17-1 is an improvement on the simple regulator circuit because it draws a large current from the supply only when required by the load. In Fig. 17-1(a), the circuit is drawn in the form of the common collector amplifier (emitter follower) discussed in Section 6-6. In Fig. 17-1(b), the circuit is shown in the form usually referred to as a *series regulator*. Transistor Q_1 is termed a *series-pass transistor*.



(a) Emitter follower voltage regulator



(b) Series voltage regulator circuit

Figure 17-1
To supply a large output current from a Zener diode voltage regulator, a transistor (Q_1) is connected as an emitter follower. This converts the circuit into a series voltage regulator.

The output voltage (V_o) from the series regulator is (V_Z - V_{BE}), and the maximum load current ($I_{L(max)}$) can be the maximum emitter current that Q_1 is capable of passing. For a *2N3055* transistor (specification in Appendix 1-8), I_L could approach 15 A. When I_L is zero, the current drawn from the supply is approximately (I_Z + $I_{C(min)}$), where $I_{C(min)}$ is the minimum collector current to keep Q_1 operational. The Zener diode circuit (R_1 and D_1) has to supply only the base current of the transistor. The series voltage regulator is, therefore, much more efficient than a simple Zener diode regulator.

Regulator with Error Amplifier

A series regulator using an additional transistor as an *error amplifier* is shown in Fig. 17-2. The error amplifier improves the line and load regulation of the circuit, (see Section 3-5). The amplifier also makes it possible to have an output voltage greater than the Zener diode voltage. Resistor R_2 and diode D_1 are the Zener diode reference source. Transistor Q_2 and its associated components constitute the error amplifier, that controls the series-pass transistor (Q_1). The output voltage is divided by resistors R_3 and R_4, and compared to the Zener voltage level (V_Z). C_1 is a large-value capacitor, usually 50 μF to 100 μF, connected at the output to suppress any tendency of the regulator to oscillate.

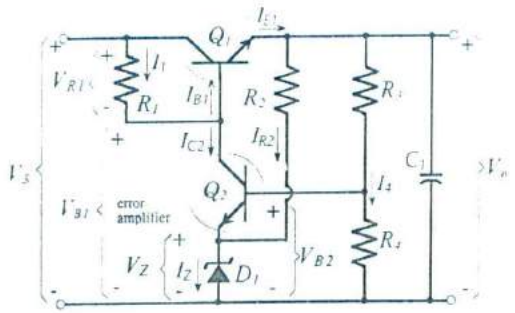


Figure 17-2
Series voltage regulator circuit with an error amplifier. The error amplifier improves the regulator line and load regulation, and gives an output voltage greater than the Zener diode voltage.

When the circuit output voltage changes, the change is amplified by transistor Q_2 and fed back to the base of Q_1 to correct the output voltage level. Suppose that the circuit is designed for V_o = 12 V, and that the supply voltage is V_S = 18 V. A suitable Zener diode voltage in this case might be V_Z = 6 V. For this V_Z level, the base voltage of Q_2 must be, V_{B2} = V_Z + V_{BE2} = 6.7 V. So, resistors R_3 and R_4 are selected to give V_{B2} = 6.7 V and V_o = 12 V. The voltage at the base of Q_1 is, V_{B1} = V_o + V_{BE1} = 12.7 V. Also, V_{R1} = V_S - V_{B1} = 5.3 V. The current through R_1 is largely the collector current of Q_2.

Now suppose the output voltage drops slightly for some reason. When V_o decreases, V_{B2} decreases. Because the emitter voltage of Q_2 is held at V_Z, any decrease in V_{B2} appears across the base-emitter of Q_2. A reduction in V_{BE2} causes I_{C2} to be reduced. When I_{C2} falls, V_{R1} is reduced, and the voltage at the base of Q_1 rises (V_{B1} = V_S - V_{R1}) causing the output voltage to increase. Thus, a decrease in V_o produces a feedback effect which causes V_o to increase back

toward its normal level. Taking the same approach, a rise in V_o above its normal level produces a feedback effect which pushes V_o down again toward its normal level.

When the input voltage changes, the voltage across resistor R_1 changes in order to keep the output constant. This change in V_{R1} is produced by a change in I_{C2}, which itself is produced by a small change in V_o. Therefore, a supply voltage change (ΔV_S) produces a small output voltage change (ΔV_o). The relationship between ΔV_S and ΔV_o depends upon the amplification of the error amplifier. Similarly, when the load current (I_L) changes, I_{B1} alters as necessary to increase or decrease I_{E1}. The I_{B1} variation is produced by a change in I_{C2} which, once again, is the result of an output voltage variation ΔV_o.

Series Regulator Performance

The performance of a series regulator without an error amplifier (Fig. 17-1) is similar to that of a Zener diode regulator, (see Section 3-6), except in the case of the load effect. The series-pass transistor tends to improve the regulator load effect by a factor equal to the transistor h_{FE}.

The error amplifier in the regulator in Fig 17-3 (reproduced from Fig. 17-2) improves all aspects of the circuit performance by an an amount directly related to the amplifier voltage gain (A_v). When V_S changes by ΔV_S, the output change is,

$$\Delta V_o = \frac{\Delta V_S}{A_v} \qquad (17\text{-}1)$$

If ΔV_S is produced by a variation in the *ac* supply voltage, the power supply source effect is reduced by a factor of A_v. ΔV_S might also be the result of an increase or decrease in load current that causes a change in the average level of the *dc* supply voltage. Thus, the load effect of the power supply is reduced by a factor of A_v.

Now consider the effect of supply voltage ripple on the circuit in Fig. 17-3. The ripple waveform appears at the collector of transistor Q_1. If there was no negative feedback, it would also be present at Q_1 base and at the regulator output. However, like supply voltage changes, the input ripple is reduced by a factor of A_v when it appears at the output. The ripple rejection ratio is calculated as the decibel ratio of the input and output ripple voltages.

Example 17-1

The supply voltage for the regulator in Fig. 17-3 has V_S = 21 V on no load, and V_S = 20 V when $I_{L(max)}$ = 40 mA. The output voltage is V_o = 12 V, and the regulator has an error amplifier with a gain of 100. Calculate the source effect, load effect, line regulation, and load regulation for the complete power supply. Also determine the ripple rejection ratio in decibels.

Solution

Eq. 3-20, Source Effect = ΔV_o for (ΔV_S = 10%)

Eq. 17-1, $$\Delta V_o = \frac{\Delta V_S}{A_v} = \frac{10\% \text{ of } 21 \text{ V}}{100}$$
$$= 21 \text{ mV}$$

Eq. 3-22, Load Effect $= \Delta V_o$ for $\Delta I_{L(max)}$

Eq. 17-1, $$\Delta V_o = \frac{\Delta V_S}{A_v} = \frac{21 \text{ V} - 20 \text{ V}}{100}$$
$$= 10 \text{ mV}$$

Eq. 3-21, Line regulation $= \dfrac{\text{(Source Effect)} \times 100\%}{E_o}$
$$= \frac{21 \text{ mV} \times 100\%}{12 \text{ V}}$$
$$= 0.175\%$$

Eq. 3-23, Load regulation $= \dfrac{\text{(Load Effect)} \times 100\%}{E_o}$
$$= \frac{10 \text{ mV} \times 100\%}{12 \text{ V}}$$
$$= 0.08\%$$

ripple rejection $= 20 \log (1/A_v) = 20 \log (1/100)$
$= -40$ dB

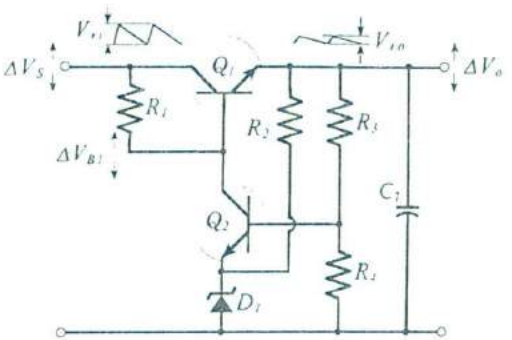


Figure 17-3
Voltage variations at the input of a regulator with an error amplifier are reduced by a factor equal to the amplifier voltage gain.

Regulator Design

To design a series regulator circuit (as in Fig. 17-3), the Zener diode is selected to have V_Z less than the output voltage. A Zener diode voltage approximately equal to 0.75 V_o is usually suitable. Appropriate current levels are chosen for each resistor, and the resistor values are calculated using Ohm's law. Transistor Q_1 is selected to pass the required load current and to survive the necessary power dissipation. A heat sink (see Section 8-8) is normally required for the series-pass transistor in a regulator that supplies large load currents. As discussed, a large capacitor is usually connected across the output to ensure amplifier *ac* stability. (C_1 in Fig. 17-3).

The difference between the regulator input and output voltages is the collector-emitter voltage of the series-pass transistor (Q_1), and this voltage must be large enough to keep the transistor operational. The minimum level of V_{CE1} (known as the *dropout voltage*) occurs at the lowest point in the ripple waveform of (rectified and filtered) *raw dc* input. If V_{CE1} is too small for correct operation at this point, a large-amplitude ripple waveform appears at the regulator output.

Example 17-2

Design the voltage regulator circuit in Fig. 17-4 to produce $V_o = 12$ V and $I_{L\,max} = 40$ mA. The supply voltage is $V_s = 20$ V.

Solution

Select, $V_Z \approx 0.75\ V_o = 0.75 \times 12\ V$

$= 9$ V

For D_1, use a *1N757* Zener diode with $V_Z = 9.1$ V (see Appendix 1-4)

For minimum D_1 current,

Select $I_{R2} = 10$ mA

$$R_2 = \frac{V_o - V_Z}{I_{R2}} = \frac{12\ V - 9.1\ V}{10\ mA}$$

$= 290\ \Omega$ (use 270 Ω standard value)

$$I_{1(max)} \approx I_{L(max)} + I_{R2} = 40\ mA + 10\ mA$$

$= 50$ mA

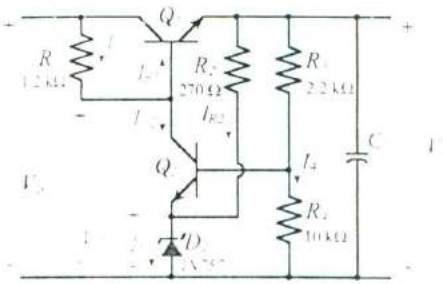


Figure 17-4
Voltage regulator circuit for Example 17-2.

Specification for Q_1,

$V_{CE(max)} = V_s = 20$ V

$I_{C\,max} \approx I_{L\,max} = 50$ mA

$P_{D(max)} = (V_s - V_o) \times I_{L\,max} = (20\ V - 12\ V) \times 50\ mA$

$= 400$ mW

Assuming $h_{FE(min)} = 50$,

$$I_{B(max)} = \frac{I_{L\,max}}{h_{FE(min)}} = \frac{50\ mA}{50}$$

$= 1$ mA

$I_{C2} > I_{B(max)}$

select, $I_{C2} = 5$ mA

$$R_1 = \frac{V_s - V_{BE}}{I_{C2} + I_{B1}} = \frac{20\ V - (12\ V + 0.7\ V)}{5\ mA + 1\ mA}$$

$= 1.21$ kΩ (use 1.2 kΩ standard value)

$I_Z = I_{E2} + I_{R2} = 5\ mA + 10\ mA$

$= 15$ mA

$I_4 >> I_{B1(max)}$

select, $I_4 = 1$ mA

$$R_4 = \frac{V_Z + V_{BE2}}{I_4} = \frac{9.1\text{ V} + 0.7\text{ V}}{1\text{ mA}}$$
$$= 9.8\text{ k}\Omega \text{ (use 10 k}\Omega \text{ standard value)}$$

$$R_3 = \frac{V_o - V_{R4}}{I_4} = \frac{12\text{ V} - 9.8\text{ V}}{1\text{ mA}}$$
$$= 2.2\text{ k}\Omega \text{ (standard value)}$$

Practise Problems

17-1.1 A 12 V dc power supply has an 18 V input (V_S) from a rectifier and filter circuit. There is a 1 V drop in V_S from no load to full load. If the regulator has an error amplifier with $A_v = 70$, calculate the source effect, load effect, line regulation, and load regulation.

17-1.2 A voltage regulator circuit as in Fig. 17-4 has $V_S = 25$ V, and is to produce $V_o = 15$ V with $I_{L(max)} = 60$ mA. Design the circuit and specify the series transistor. Assume $h_{FE1(min)} = 100$.

17-2 Improving Regulator Performance

Error Amplifier Gain

The performance of a regulator is dependent on the voltage gain of the error amplifier, (see Eq. 17-1). A higher gain amplifier gives better line and load regulation. So, anything that improves the amplifier voltage gain will improve the regulator performance. Two possibilities to increase A_v are: using as transistor with a high h_{FE} value for Q_2, and using the highest possible resistance value for R_1.

Output Voltage Adjustment

Regulator circuits such as the one designed in Example 17-2 are unlikely to have V_o exactly as specified. This is because of component tolerances, as well as, perhaps, not finding standard values close to the calculated values. Hence, some form of adjustment is required to enable the output voltage to be set to the desired level. In Fig. 17-5 the potentiometer (R_5) connected between resistors R_3 and R_4 provides output adjustment. The maximum output voltage level is produced when the potentiometer moving contact is at the bottom of R_5:

$$V_{o(max)} = \frac{R_3 + R_4 + R_5}{R_4} \times V_{B2} \qquad (17\text{-}2)$$

Minimum V_o occurs when the moving contact is at the top of R_5:

$$V_{o(min)} = \frac{R_3 + R_4 + R_5}{R_4 + R_5} \times V_{B2} \qquad (17\text{-}3)$$

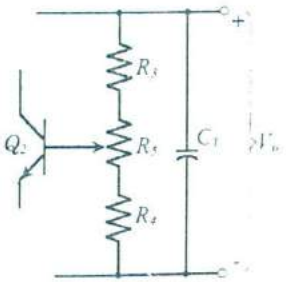


Figure 17-5
Use of a potentiometer to provide regulator output voltage adjustment.

Example 17-3

Modify the voltage regulator circuit in Ex. 17-2 (as in Fig. 17-6) to make V_o adjustable from 11 V to 13 V.

Solution

select $I_{4(min)} = 1$ mA

For $V_o = 11$ V, (moving contact at top of R_5)

$$R_3 = \frac{V_o - V_{B2}}{I_{4(min)}} = \frac{11\text{ V} - 9.8\text{ V}}{1\text{ mA}}$$

$$= 1.2\text{ k}\Omega \text{ (standard value)}$$

$$R_4 + R_5 = \frac{V_{B2}}{I_{4(min)}} = \frac{9.8\text{ V}}{1\text{ mA}}$$

$$= 9.8\text{ k}\Omega$$

For $V_o = 13$ V (moving contact at bottom of R_5)

I_4 becomes, $$I_4 = \frac{V_o}{R_3 + R_4 + R_5} = \frac{13\text{ V}}{1.2\text{ k}\Omega + 9.8\text{ k}\Omega}$$

$$= 1.18\text{ mA}$$

$$R_4 = \frac{V_{B2}}{I_4} = \frac{9.8\text{ V}}{1.18\text{ mA}}$$

$$= 8.3\text{ k}\Omega \text{ (use 8.2 k}\Omega \text{ standard value)}$$

$$R_5 = (R_4 + R_5) - R_4 = 9.8\text{ k}\Omega - 8.2\text{ k}\Omega$$

$$= 2.6\text{ k}\Omega \text{ (use 2.5 k}\Omega \text{ standard value potentiometer)}$$

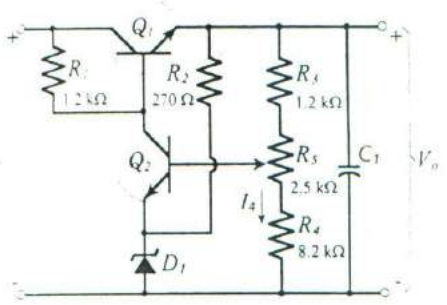


Figure 17-6
Adjustable output regulator circuit for Example 17-3.

High Output Current Circuit

For the circuit in Fig. 17-6 to function correctly, the collector current of Q_2 must be larger than the maximum base current flowing into Q_1. In regulators that supply a large output current, I_{B1} can be too large for I_{C2} to control. In this case, an additional transistor (Q_3) should be connected at the base of Q_1 to form a *Darlington Circuit* (or *Darlington Pair*), as in Fig. 17-7. Transistor Q_1 is usually a high power *BJT* requiring a heat sink (see Section 8-8), and Q_3 is a low power device. The Q_3 base current is,

$$I_{B3} = \frac{I_L}{h_{FE1} \times h_{FE3}} \qquad \textbf{(17-4)}$$

The current gain for the Darlington is ($h_{FE1} \times h_{FE3}$), and the level of I_{B3} is low enough that I_{C2} may easily be made much greater than I_{B3}. Note resistor R_6 in Fig. 17-7, which is included to provide a suitable minimum Q_3 operating current when I_L is very low.

Darlington transistors consisting of a pair of (low-power and high-power) *BJTs* fabricated together and packaged as a single

device are available. These are usually referred to as *power Darlingtons*. The *2N6039* is an *npn* power Darlington with an h_{FE} specified as 750 minimum, 18 000 maximum. Resistor R_6 in Fig. 17-7 is not required when a power Darlington is used.

Example 17-4

Modify the voltage regulator circuit in Ex. 17-2 to change the load current to 200 mA. Use a Darlington circuit (as in Fig. 17-7), and assume that $h_{FE1} = 20$, and that $h_{FE3} = 50$. Specify transistor Q_1.

Solution

$$I_{E1(max)} \approx I_{L(max)} + I_{R2} = 200\text{ mA} + 10\text{ mA}$$
$$= 210\text{ mA}$$

$$I_{B1(max)} = \frac{I_{E1(max)}}{h_{FE1}} = \frac{210\text{ mA}}{20}$$
$$= 10.5\text{ mA}$$

$$I_{B3(max)} = \frac{I_{B1(max)}}{h_{FE3}} = \frac{10.5\text{ mA}}{50}$$
$$= 0.21\text{ mA}$$

$$I_{C2} > I_{B3(max)}$$

select, $I_{C2} = 1\text{ mA}$

$$R_1 = \frac{V_S - V_{B3}}{I_{C2} + I_{B3}} = \frac{20\text{ V} - (12\text{ V} + 0.7\text{ V} + 0.7\text{ V})}{1\text{ mA} + 0.21\text{ mA}}$$
$$= 5.45\text{ k}\Omega \text{ (use 5.6 k}\Omega\text{ standard value)}$$

select, $I_6 = 0.5\text{ mA}$

$$R_6 = \frac{V_o + V_{BE1}}{I_6} = \frac{12\text{ V} + 0.7\text{ V}}{0.5\text{ mA}}$$
$$= 25.4\text{ k}\Omega \text{ (use 22 k}\Omega\text{ standard value)}$$

Specification for Q_1,

$$V_{CE1(max)} \approx V_S = 20\text{ V}$$

$$I_{C1(max)} \approx I_{E1(max)} = 210\text{ mA}$$

$$P_{D(max)} = (V_S - V_o) \times I_{E1(max)} = (20\text{ V} - 12\text{ V}) \times 210\text{ mA}$$
$$= 1.68\text{ W}$$

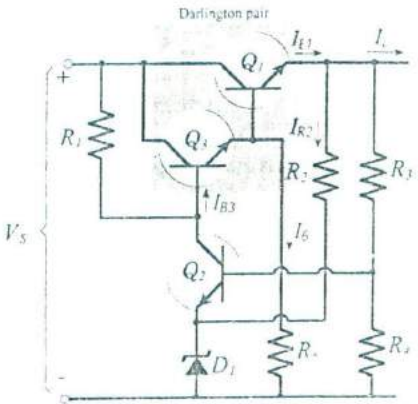


Figure 17-7
An additional transistor (Q_3) connected at the base of Q_1 to constitute a Darlington circuit allows a voltage regulator to supply a higher output current.

Preregulation

Refer to Fig. 17-8, which is a partially reproduction of Fig. 17-2. Note that resistor R_1 is supplied from the regulator input, and consider what happens when the supply voltage drops by 1 V. If I_{C2}

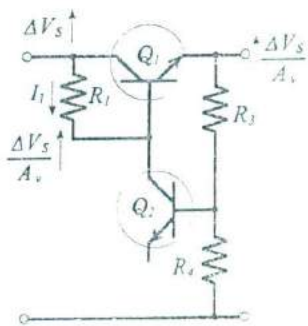


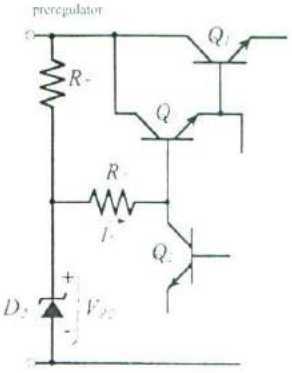
Figure 17-8
A change in a regulator supply voltage (ΔV_S) produces an output change ($\Delta V_o = \Delta V_S / A_v$).

does not change, the voltage across R_1 remains constant, and the 1 V drop also occurs at the base of Q_1 and at the output of the regulator. This does not happen, of course. Instead, I_{C2} changes to reduce the voltage across R_1 and thus keep the output voltage close to its normal level. The change in I_{C2} is produced by a small change in the output voltage. If R_1 is connected to a *constant-voltage source* instead of the input, the change in I_{C2} would not be required when V_S changes, and consequently, the output voltage change would not occur.

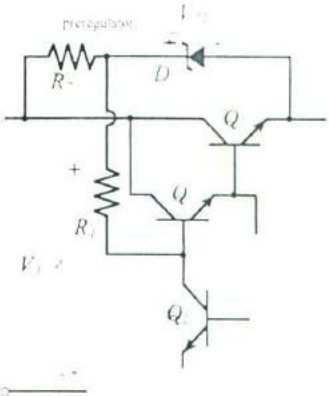
Now look at Fig. 17-9(a) where R_1 is shown connected to another Zener diode voltage source (R_7 and D_2). This arrangement is called a *preregulator*. When V_S changes, the change in V_{Z2} that occurs is negligible compared to ΔV_S. Thus, virtually no change is required in I_{C2} and V_o. A preregulator substantially improves the line and the load regulation of a regulator circuit.

The minimum voltage drop across R_1 should typically be 3 V. (Small values of R_1 give low amplifier voltage gain.) Also, a minimum of perhaps 6 V is required across R_7 to keep a reasonably constant current level through D_2. The voltage (V_{Z2}) for D_2 is usually a relatively high voltage for a Zener diode. It may be necessary to use two diodes in series to give the desired voltage.

Figure 17-9(b) shows another preregulator circuit that has R_7 and D_2 connected across transistor Q_1. This gives an R_1 supply voltage of $V_1 = (V_{\cdot\cdot} + V_{Z2})$.



(a) Preregulator at the input



(b) Preregulator connected between input and output

Figure 17-9
A preregulator circuit improves the performance of a voltage regulator.

Example 17-5

Determine suitable component values for a preregulator circuit as in Fig. 17-9(a) for the voltage regulator modified in Ex. 17-4.

Solution

select $V_{R1(min)} = 3$ V

$$R_1 = \frac{V_{R1}}{I_{C2} + I_{B3}} = \frac{3\text{ V}}{1\text{ mA} + 0.21\text{ mA}}$$

$= 2.5\text{ k}\Omega$ (use 2.7 kΩ standard value)

$$V_{Z2} = V_o + V_{BE1} + V_{BE3} + V_{R1}$$
$$= 12\text{ V} + 0.7\text{ V} + 0.7\text{ V} + 3\text{ V}$$
$$= 16.4\text{ V}$$

(Use a *1N966A* with $V_Z = 16$ V. Alternatively, use a *1N753* and a *1N758* connected in series. See Appendix 1-4)

$I_{R7} >> I_1$ and $I_{Z2} > (I_{ZK}$ for Zener diode D_2

select $I_{R7} = 5$ mA

$$R_2 = \frac{V_S - V_{Z2}}{I_{R7}} = \frac{20\text{ V} - 16\text{ V}}{5\text{ mA}}$$

$= 800\ \Omega$ (use 820 Ω standard value)

Constant Current Source

The constant-current source shown in Fig. 17-10 may be used in place of resistor R_1 as an alternative to a preregulator circuit. This arrangement passes all the required current to Q_3 base and Q_2 collector, but behaves as a very high resistance ($1/h_{oe4}$) at the collector of transistor Q_2. Consequently, it increases the error amplifier voltage gain and results in a substantial improvement in the regulator performance. To design the constant current source, V_{CE4} should typically be a minimum of 3 V. The various voltage drops and current levels are then easily determined for component selection.

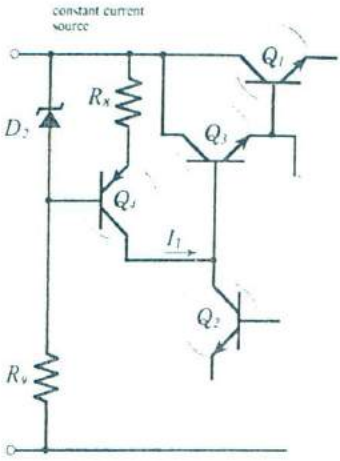


Figure 17-10
A constant-current source can be used as an alternative to a preregulator circuit to improve regulator performance.

Differential Amplifier

Figure 17-11 shows a regulator that uses a differential amplifier, or *difference amplifier*, (see Section 12-8). In this circuit, Zener diode D_2 is the voltage reference source, and D_1 is used only to provide an appropriate voltage level at the emitter of transistor Q_2. V_o is divided to provide V_{B6}, and V_{B6} is compared to V_{Z2}. Any difference in these two voltages is amplified by Q_5, Q_6, Q_2, and the associated components, and then applied to the base of Q_3 to change the output in the required direction.

The performance of the regulator is improved by the increased voltage gain of the error amplifier. However, the performance is also improved in another way. In the regulator circuit in Figs. 17-2 and 17-7, when I_{C1} changes, the current through D_1 is also changed. ($I_{Z1} = I_{R2} + I_{E2}$). This causes the Zener voltage to change by a small amount, and this change in V_{Z1} produces a change in output voltage. In the circuit in Fig. 17-11, the current through the reference diode (D_2) remains substantially constant because it is supplied from the regulator output. Therefore, there is no change in output voltage due to a change in the reference voltage.

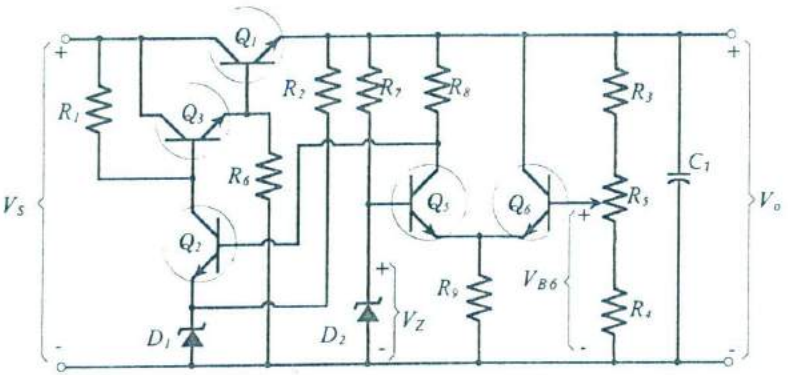


Figure 17-11
Use of a differential amplifier (Q_5 and Q_6 etc.,) improves the regulator performance by improving the gain of the error amplifier, and by using D_2 as a stable voltage reference source.

Example 17-6

Design the differential amplifier stage for the regulator in Fig. 17-11. Use the Q_1, Q_2, Q_3 stage already designed in Examples 17-2 and 17-4. The output voltage is to be adjustable from 10 V to 12 V.

Solution

$$V_{C5} = V_{B2} = 9.8\ \text{V}$$

select $V_{CE5} = 3\ \text{V}$

$$V_{R9} = V_{C5} - V_{CE5} = 9.8\ \text{V} - 3\ \text{V}$$
$$= 6.8\ \text{V}$$

$$V_{Z2} = V_{R9} + V_{BE5} = 6.8\ \text{V} + 0.7\ \text{V}$$
$$= 7.5\ \text{V} \text{ (use a 1N755 Zener diode)}$$

$I_{C5} >> I_{B2}$

select $I_{C5} = 1\ \text{mA}$

$$R_8 = \frac{V_o - V_{C2}}{I_{C5}} = \frac{12\ \text{V} - 9.8\ \text{V}}{1\ \text{mA}}$$
$$= 2.2\ \text{k}\Omega \text{ (standard value)}$$

$$I_{R9} \approx 2 \times I_{C5} = 2\ \text{mA}$$

$$R_9 = \frac{V_{R9}}{I_{R9}} = \frac{6.8\ \text{V}}{2\ \text{mA}}$$
$$= 3.4\ \text{k}\Omega \text{ (use 3.3 k}\Omega\text{ standard value)}$$

$I_{Z2} >> I_{B5}$ and $I_{Z2} > (I_{ZK}$ for the Zener diode)

select $I_{Z2} = 10\ \text{mA}$

$$R_7 = \frac{V_o - V_{Z2}}{I_{Z2}} = \frac{12\ \text{V} - 7.5\ \text{V}}{10\ \text{mA}}$$
$$= 450\ \Omega \text{ (use 470 }\Omega\text{ standard value)}$$

$I_4 >> I_{B6}$

select $I_4 = 1\ \text{mA}$

$$V_{B6} = V_{Z2} = 7.5\ \text{V}$$

when $V_o = 11$ V, (moving contact at the top of R_5)

$$R_3 = \frac{V_o - V_{B6}}{I_4} = \frac{11\ \text{V} - 7.5\ \text{V}}{1\ \text{mA}}$$
$$= 3.5\ \text{k}\Omega \text{ (use 3.3 k }\Omega\text{ standard value)}$$

I_4 becomes, $$I_4 = \frac{V_o - V_{B6}}{R_3} = \frac{11\ \text{V} - 7.5\ \text{V}}{3.3\ \text{mA}}$$
$$= 1.06\ \text{mA}$$

$$R_4 + R_5 = \frac{V_{B6}}{I_4} = \frac{7.5\ \text{V}}{1.06\ \text{mA}}$$
$$= 7.07\ \text{k}\Omega$$

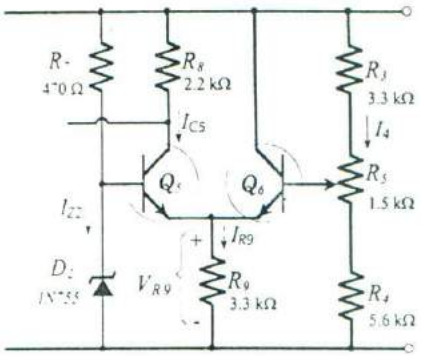


Figure 17-12
Differential amplifier circuit for Example 17-6.

When V_o = 13 V, (moving contact at the bottom of R_5)

I_4 becomes, $$I_4 = \frac{V_o}{R_3 + R_4 + R_5} = \frac{13\text{ V}}{3.3\text{ k}\Omega + 7.07\text{ k}\Omega}$$
$$= 1.25\text{ mA}$$

$$R_4 = \frac{V_{B6}}{I_4} = \frac{7.5\text{ V}}{1.25\text{ mA}}$$
$$= 6.25\text{ k}\Omega \text{ (use 5.6 k}\Omega \text{ standard value)}$$

$$R_5 = (R_4 + R_5) - R_4 = 7.07\text{ k}\Omega - 5.6\text{ k}\Omega$$
$$= 1.47\text{ k}\Omega \text{ (use 1.5 k}\Omega \text{ standard value potentiometer)}$$

Practise Problems

17-2.1 A voltage regulator circuit as in Fig. 17-6 uses a 6.2 V Zener diode. Determine suitable resistor values for R_3, R_4, and R_5 to produce an output adjustable from 9 V to 12 V.

17-2.2 A voltage regulator has an 18 V supply, a 10 V output, and a 150 mA load current. The circuit uses Darlington connected transistors, as in Fig. 17-7. Calculate suitable resistor values, and specify transistor Q_1. Assume that $h_{FE1} = 20$ and $h_{FE3} = 50$.

17-2.3 Determine suitable components for the constant current circuit in Fig. 17-10. Assume that the supply voltage is 20 V, the output is 12 V, and that I_{B3} is 100 μA.

17-3 Current Limiting

Short-Circuit Protection

Power supplies used in laboratories are subject to overloads and short circuits. Short-circuit protection by means of current limiting circuits is necessary in such equipment to prevent the destruction of components when an overload occurs. Transistor Q_7 and resistor R_{10} in Fig. 17-13(a) constitute a *current limiting circuit*. When the load current (I_L) flowing through resistor R_{10} is below the normal maximum level, the voltage drop V_{R10} is not large enough to forward bias the base-emitter junction of Q_7. In this case, Q_7 has no effect on the regulator performance.

When the load current reaches the selected maximum ($I_{L(max)}$), V_{R10} biases Q_7 on. Current I_{C7} then produce a voltage drop across resistor R_1 that drives the output voltage down to near zero.

The voltage/current characteristic of the regulator is shown in Fig. 17-13(b). It is seen that output voltage remains constant as the load current increases up to $I_{L(max)}$. Beyond $I_{L(max)}$, V_o drops to zero, and a short-circuit current (I_{SC}) slightly greater than $I_{L(max)}$ flows at the output. Under this circumstance, series pass transistor Q_1 is carrying all of the short-circuit current and has virtually all of the supply voltage developed across its terminals.

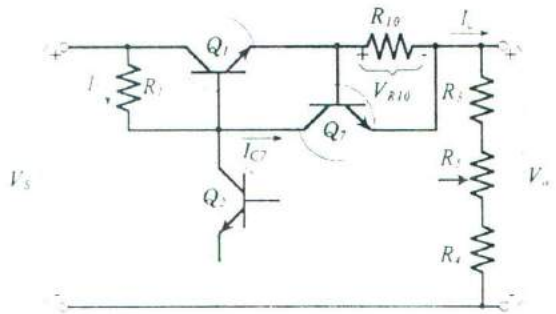
So, the power dissipation in Q_1 is,

$$P_1 = V_S \times I_{SC} \qquad (17\text{-}5)$$

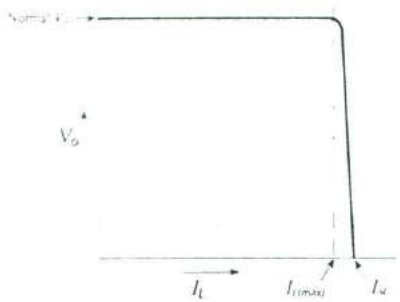
Obviously, Q_1 must be selected to survive this power dissipation.

Design of the current limiting circuit in Fig. 17-13 is very simple. Assuming that Q_7 is a silicon transistor, it should begin to conduct when $V_{R10} \approx 0.5$ V. Therefore, R_{10} is calculated as,

$$R_{10} \approx \frac{0.5\ V}{I_{L(max)}} \qquad (17\text{-}6)$$



(a) Current limiting circuit



(b) V_o/I_o characteristic of current limiting circuit

Figure 17-13
Regulator overload protection circuit. When I_L increases to a selected maximum level, V_{R10} causes Q_7 to conduct, and this pulls Q_1 base down causing V_o to be reduced to near zero.

Fold-Back Current Limiting

A problem with the simple short-circuit protection method just discussed is that there is a large amount of power dissipation in the series pass transistor while the regulator remains short-circuited. The foldback current limiting circuit in Fig. 17-14(a) minimizes this transistor power dissipation. The graph of V_o/I_L in Fig. 17-14(b) shows that the regulator output voltage remains constant until $I_{L(max)}$ is approached. Then the current reduces (or folds back) to a lower short-circuit current level (I_{SC}). The lower level of I_{SC} produces a lower power dissipation in Q_1.

To understand how the circuit in Fig. 17-14 operates, first note

that when the output is shorted, V_o equals zero. Consequently, the voltage drop across resistor R_{11} is almost zero. The voltage across R_{10} is (I_{SC} x R_{10}), and (as in the simple short-circuit protection circuit) this is designed to just keep transistor Q_3 biased *on*. When the regulator is operating normally with I_L less than $I_{L(max)}$, the voltage drop across R_{11} is,

$$V_{R11} \approx \frac{V_o \times R_{11}}{R_{11} + R_{12}}$$

To turn Q_7 *on*, the voltage drop across R_{10} must become larger than V_{R11} by enough to forward bias the base-emitter junction of Q_7. Using $V_{BE7} \approx 0.5$ V, and making $V_{R11} \approx 0.5$ V gives

$$I_{L(max)} R_{10} = 0.5 \text{ V} + 0.5 \text{ V} = 1 \text{ V}$$

With $I_{SC} R_{10} = 0.5$ V,

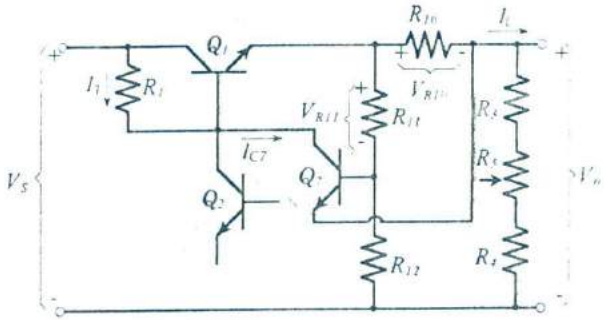
$$I_{L(max)} \approx 2 I_{SC} \quad \text{[see Fig. 17-14(b)]}$$

If V_{R11} is selected as 1 V,

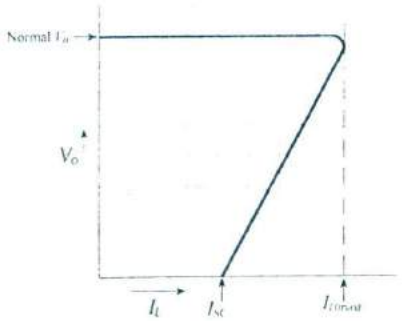
$$I_{L(max)} R_{10} = 0.5 \text{ V} + 1 \text{ V} = 1.5 \text{ V}$$

and,

$$I_{L(max)} \approx 3 I_{SC}$$



(a) Foldback current limiting circuit



(b) Characteristic of foldback current limiting circuit

Figure 17-14
Foldback current limiting. The short-circuit current (I_{SC}) is less than $I_{L(max)}$, thus minimizing the power dissipation in Q_1.

The fold-back current limiting circuit is designed by first calculating R_{10} to give the desired level of I_{SC}. Then, the voltage divider resistors (R_{11} and R_{12}) are calculated to provide the necessary voltage drop across R_{11} for the required relationship between I_{SC} and I_{Lmax}.

Example 17-7

Design a foldback current limiting circuit for a voltage regulator with a 12 V output. The maximum output current is to be 200 mA, and the short-circuit current is to be 100 mA.

Solution

$$I_{SC} = 100 \text{ mA}$$

select $V_{R10} \approx 0.5$ V at short-circuit

$$R_{10} = \frac{V_{R10}}{I_{SC}} = \frac{0.5 \text{ V}}{100 \text{ mA}}$$

$$= 5\ \Omega \text{ (use 4.7 } \Omega \text{ standard value)}$$

at $I_{L(max)}$ $V_{R10} = I_{L(max)} \times R_{10} = 200 \text{ mA} \times 4.7\ \Omega$

$$= 0.94 \text{ V}$$

$$V_{R11} = I_{L(max)} R_{10} - 0.5 \text{ V}$$

$$= 0.44 \text{ V}$$

$$I_{11} >> I_B.$$

select $I_{11} = 1$ mA

$$R_{11} = \frac{V_{R11}}{I_{11}} = \frac{0.44 \text{ V}}{1 \text{ mA}}$$

$$= 440\ \Omega \text{ (use 470 } \Omega \text{ standard value)}$$

$$R_{12} = \frac{V_o + V_{R10} - V_{R11}}{I_{11}} = \frac{12 \text{ V} + 0.94 \text{ V} - 0.44 \text{ V}}{1 \text{ mA}}$$

$$= 12.5 \text{ k}\Omega \text{ (use 12 k}\Omega \text{ standard value)}$$

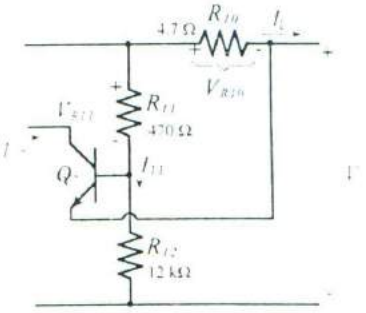


Figure 17-15
Foldback current limiting circuit for Example 17-7.

Practise Problems

17-3.1 A short-circuit protection circuit, as in Fig 17-13, is to be designed to limit the output of a 15 V regulator to 400 mA. Select a suitable value for R_{10}, and specify Q_1. Assume that $V_S = 25$ V.

17-3.2 Modify the circuit designed for Problem 17-3.1 to convert it to fold-back current limiting with a 150 mA short-circuit current.

17-4 Op-amp Voltage Regulators

Voltage Follower Regulator

Refer once again to the voltage regulator circuit in Fig. 17-11. The complete error amplifier has two input terminals at the bases of Q_5 and Q_6 and one output at the collector of Q_2. Transistor Q_6 base is an inverting input and Q_5 base is a noninverting input. The error amplifier circuit is essentially an operational amplifier. Thus, IC operational amplifiers with their extremely high open-loop voltage gain are ideal for use as error amplifiers in *dc* voltage regulator circuits. Normally, an internally compensated op-amp (such as the *741*) is quite suitable for most voltage regulator applications.

A simple voltage follower regulator circuit is illustrated in Fig. 17-16. In this circuit, the op-amp output voltage always follows the voltage at the noninverting terminal, consequently, V_o remains constant at V_Z. The only design calculations are those required for design of the Zener diode voltage reference circuit (R_1 and D_1), and for the specification of Q_1.

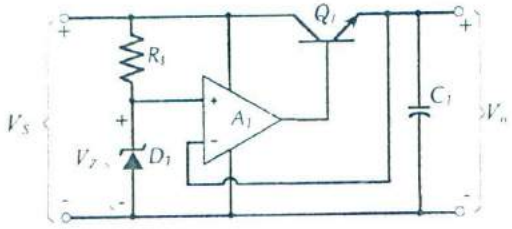


Figure 17-16
Operational amplifier connected as a voltage follower regulator. The output voltage is held constant at V_Z.

Adjustable Output Regulator

The circuit in Fig. 17-17 is that of a variable-output, highly stable *dc* voltage regulator. As in the transistor circuit in Fig. 17-11, the reference diode in Fig. 17-17 is connected at the amplifier noninverting input, and the output voltage is divided and applied to the inverting input. The operational amplifier positive supply terminal has to be connected to regulator supply voltage. If it were connected to the regulator output, the op-amp output voltage (at Q_2 base) would have to be approximately 0.7 V higher than its positive supply terminal, and this is impossible.

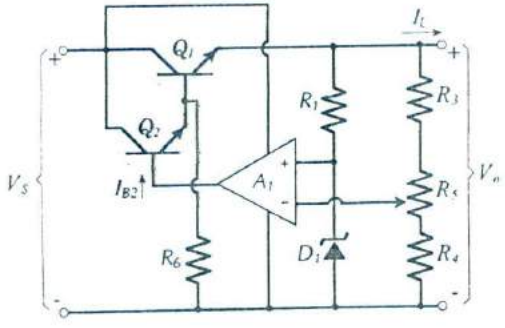


Figure 17-17
Highly stable, adjustable output, voltage regulator using an operational amplifier.

Design of the regulator circuit in Fig. 17-17 involves selection of R_1 and D_1, design of the voltage divider network (R_3, R_4, and R_5), and specification of transistors Q_1 and Q_2. Clearly, an op-amp voltage regulator is more easily designed than a purely transistor regulator circuit.

Example 17-8

Design the voltage regulator circuit in Fig. 17-18 to give an output voltage adjustable from 12 V to 15 V. The maximum output current is to be 250 mA, and the supply voltage is 20 V. Assuming $h_{fE1} = 20$ and $h_{fE2} = 50$, estimate the op-amp maximum output current.

Solution

$$V_Z \approx 0.75\, V_{o(min)} = 0.75 \times 12\ \text{V}$$
$$= 9\ \text{V}$$

Use a 1N757 diode with $V_Z = 9.1$ V

$$I_Z >> (\text{op-amp } I_{B(max)}), \text{ and } I_Z > (I_{ZK} \text{ for the diode})$$

Select $I_Z = 10$ mA

$$R_1 = \frac{V_{o(min)} - V_Z}{I_{Z1}} = \frac{12\ \text{V} - 9.1\ \text{V}}{10\ \text{mA}}$$
$$= 290\ \Omega \text{ (use 270 } \Omega \text{ standard value)}$$

$I_{3(min)} >> (\text{op-amp } I_{B(max)})$

select $I_{3(min)} = 1$ mA

when $V_o = 12$ V, (moving contact at top of R_5)

$$R_3 = \frac{V_o - V_Z}{I_{3(min)}} = \frac{12\ \text{V} - 9.1\ \text{V}}{1\ \text{mA}}$$
$$= 2.9\ \text{k}\Omega \text{ (use 2.7 k}\Omega \text{ standard value)}$$

$$R_4 + R_5 = \frac{V_Z}{I_{3(min)}} = \frac{9.1\ \text{V}}{1\ \text{mA}}$$
$$= 9.1\ \text{k}\Omega$$

When $V_o = 15$ V, (moving contact at bottom of R_5)

I_3 becomes, $$I_3 = \frac{V_o}{R_3 + R_4 + R_5} = \frac{15\ \text{V}}{2.7\ \text{k}\Omega + 9.1\ \text{k}\Omega}$$
$$= 1.27\ \text{mA}$$

$$R_4 = \frac{V_Z}{I_3} = \frac{9.1\ \text{V}}{1.27\ \text{mA}}$$
$$= 7.16\ \text{k}\Omega \text{ (use 6.8 k}\Omega \text{ standard value)}$$

$$R_5 = (R_4 + R_5) - R_4 = 9.1\ \text{k}\Omega - 6.8\ \text{k}\Omega$$

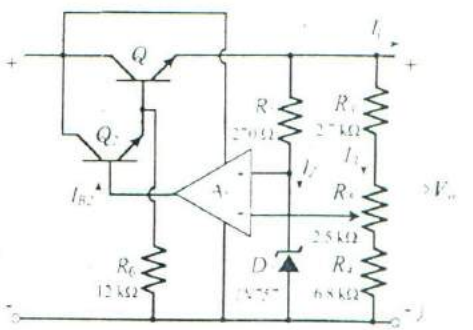


Figure 17-18
Op-amp voltage regulator for Example 17-8.

$= 2.3\ \text{k}\Omega$ (use 2.5 kΩ potentiometer)

select $I_{R6} = 1\ \text{mA}$

$$R_6 = \frac{V_{Z2}}{I_{R6}} = \frac{12\ \text{V}}{0.5\ \text{mA}}$$

$= 24\ \text{k}\Omega$ (use 22 kΩ standard value)

op-amp output current,

$$I_{B2} = \frac{I_{L(max)}}{h_{fE1} \times h_{fE2}} = \frac{250\ \text{mA}}{20 \times 50}$$

$= 0.25\ \text{mA}$

Current Limiting with an Op-amp Regulator

When a large output current is to be supplied by an operational amplifier voltage regulator, one of the current limiting circuits described in Section 17-3 may be used with one important modification. Figure 17-19 shows the modification. A resistor (R_{13}) must be connected between the op-amp output terminal and the junction of Q_{2B} and Q_{7C}. When an overload causes the regulator output voltage to go to zero, the op-amp output goes high (close to V_S) as it attempts to return V_o to its normal level. Consequently, because the op-amp normally has a very low output resistance, R_{13} is necessary to allow I_{C7} to drop the voltage at Q_2 base to near ground level. The additional resistor at the op-amp output is calculated as $R_{13} \approx V_S/I_{C7}$. Resistor R_{13} must not be so large that an excessive voltage drop occurs across it when the regulator is supposed to be operating normally.

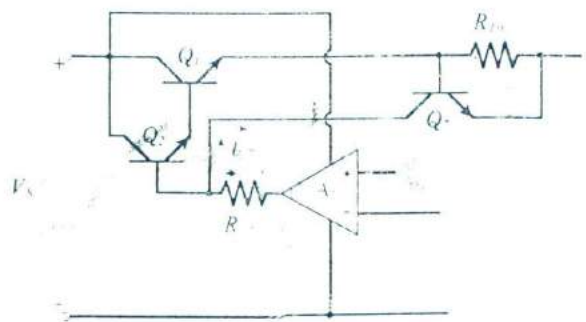


Figure 17-19
When current limiting is used with an op-amp regulator, a resistor (R_{13}) must be included in series with the op-amp output.

Practise Problems

17-4.1 Design an op-amp voltage regulator circuit as in Fig. 17-17) to produce an output adjustable from 15 V to 18 V, with a 300 mA maximum load current. The supply voltage is 25 V.

17-4.2 Design a fold-back current limiting circuit for the regulator in Problem 17-4.1. Use $I_{L(max)} = 300$ mA and $I_{SC} = 20$ mA when $V_o = 15$ V.

17-5 IC Linear Voltage Regulators

723 IC Regulator

The basic circuit of a 723 IC voltage regulator in a dual-in-line package is shown in Fig. 17-20. This IC has a voltage reference source (D_1), an error amplifier (A_1), a series pass transistor (Q_1), and a current limiting transistor (Q_2), all contained in one small package. An additional Zener diode (D_2) is included for voltage dropping in some applications. The IC can be connected to function as a positive or negative voltage regulator with an output voltage ranging from 2 V to 37 V, and output current levels up to 150 mA. The maximum supply voltage is 40 V, and the line and load regulations are each specified as 0.01%. A partial specification for the 723 regulator is given in Appendix 1-16.

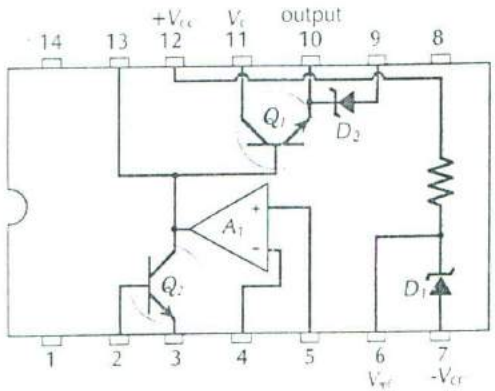


Figure 17-20
The 723 IC voltage regulator contains a reference diode (D_1), and error amplifier (A_1), a series-pass transistor (Q_1), a current limiting transistor (Q_2), and a voltage-dropping diode (D_2).

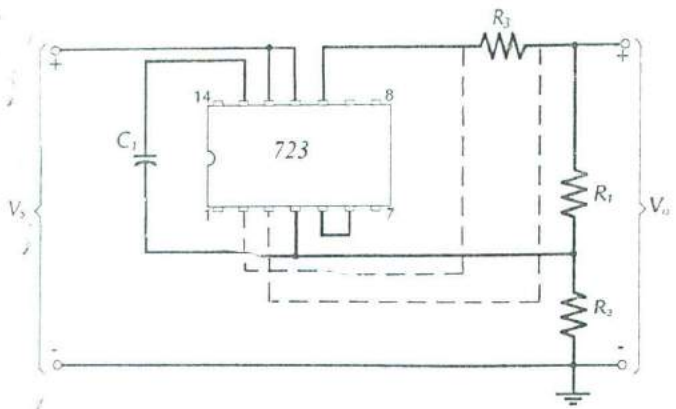


Figure 17-21
Voltage regulator circuit using a 723 IC regulator. The output voltage range is 7 V to 37 V.

Figure 17-21 shows a 723 connected to function as a positive voltage regulator. The complete arrangement (including the internal circuitry shown in Fig. 17-20) is similar to the op-amp regulator circuit in Fig. 17-17. One difference between the two circuits is the 100 pF capacitor (C_1) connected to the error amplifier output and its inverting input terminal. This capacitor is used

instead of a large capacitor at the output terminals to prevent the regulator from oscillating. (Sometimes both capacitors are required.) By appropriate selection of resistors R_1 and R_2 in Fig. 17-21, the regulator output can be set to any level between 7.15 V (the reference voltage) and 37 V. A potentiometer can be included between R_1 and R_2 to make the output voltage adjustable.

The dashed lines (in Fig. 17-21) show connections for simple (non-foldback) current limiting. Fold-back current limiting can also be used with the *723*.

It is important to note that, as for all linear regulator circuits, the supply voltage at the lowest point on the ripple waveform should be at least 3 V greater than the regulator output; otherwise a high-amplitude output ripple might occur. The total power dissipation in the regulator should be calculated to ensure that it does not exceed the specified maximum. The specification lists 1.25 W as the maximum power dissipation at a free air temperature of 25°C for a *DIL* package. This must be derated at 10 mW/°C for higher temperatures. For a metal can package, $P_{D(max)}$ = 1 W at 25°C free air temperature, and the derating factor is 6.6 mW/°C. An external series-pass transistor may be Darlington-connected to (internal transistor) Q_1, to enable a *723* regulator to handle larger load current. This is illustrated in Fig. 17-22.

A regulator output voltage less than the 7.15 V reference level can be obtained by using a voltage divider across the reference source (terminals 6 and 7 in Fig. 17-20). Terminal 5 is connected to the reduced reference voltage, instead of to terminal 6.

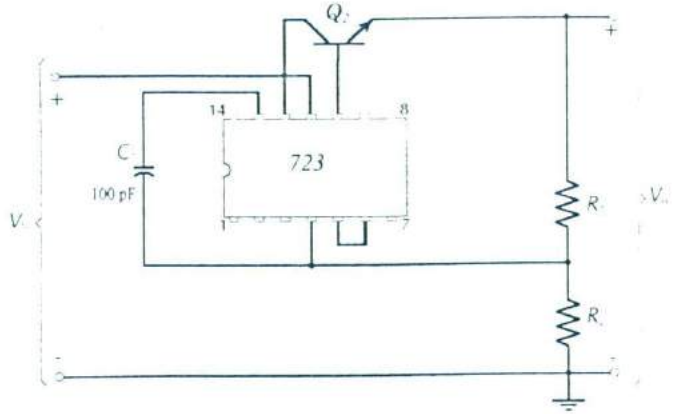


Figure 17-22
An external series-pass transistor may be added to a 723 IC voltage regulator to supply higher load currents than the 723 can normally handle.

Example 17-9

The regulator circuit in Fig. 17-21 is to have an output of 10 V. Calculate resistor values for R_1 and R_2, select a suitable input voltage, and determine the maximum load current that may be supplied if $P_{D(max)}$ = 1000 mW.

Solution

$I_2 >>$ (error amplifier input bias current)

Select $I_2 = 1$ mA

$$V_{R2} = V_{ref} = 7.15 \text{ V}$$

$$R_2 = \frac{V_{ref}}{I_2} = \frac{7.15 \text{ V}}{1 \text{ mA}}$$

$= 7.15$ kΩ (use 6.8 kΩ standard value, and recalculate I_2)

I_2 becomes, $$I_2 = \frac{V_{ref}}{R_2} = \frac{7.15 \text{ V}}{6.8 \text{ k}\Omega}$$

$= 1.05$ mA

$$R_1 = \frac{V_o - V_{ref}}{I_1} = \frac{10 \text{ V} - 7.15 \text{ V}}{1.05 \text{ mA}}$$

≈ 2.85 KΩ (use 2.7 kΩ standard value)

For satisfactory operation of the series pass transistor,

select $V_S - V_o = 5$ V

$$V_S = V_o + 5 \text{ V} = 10 \text{ V} + 5 \text{ V}$$
$$= 15 \text{ V}$$

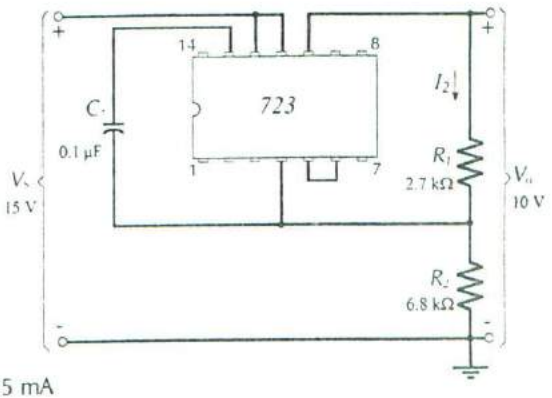


Figure 17-23
Regulator circuit for Ex. 17-9.

The internal circuit current is,

$$I_{(standby)} + I_{ref} \approx 25 \text{ mA}$$

The 723 internal power dissipation on no-load is,

$$P_i = V_S \times (I_{(standby)} + I_{ref}) = 15 \text{ V} \times 25 \text{ mA}$$
$$= 375 \text{ mW}$$

Maximum power dissipated in the (internal) series-pass transistor,

$$P_D = (\text{specified } P_{D(max)}) - P_i = 1000 \text{ mW} - 375 \text{ mW}$$
$$= 625 \text{ mW}$$

Maximum load current,

$$I_{L(max)} = \frac{P_D}{V_S - V_o} = \frac{625 \text{ mW}}{5 \text{ V}}$$
$$= 125 \text{ mA}$$

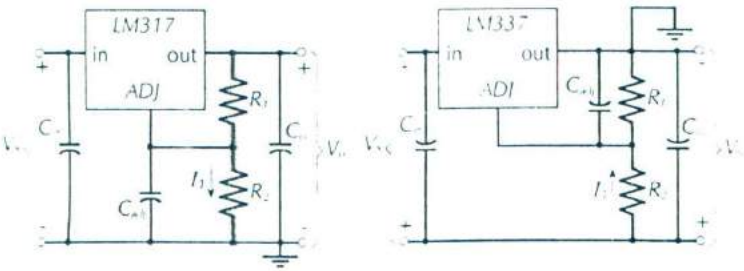
LM317 and LM337 IC Regulators

The *LM317* and *LM337 IC* regulators are three-terminal devices which are extremely easy to use. The *317* is a positive voltage regulator [Fig. 17-24(a)], and the *337* is a negative voltage regulator

[Fig. 17-24(b)]. In each case, *input* and *output* terminals are provided for supply and regulated output voltage, and an adjustment terminal (*ADJ*) is included for output voltage selection. The output voltage range is 1.2 V to 37 V, and the maximum load current ranges from 300 mA to 2 A, depending on the device package type. Typical line and load regulations are specified as 0.01%/(volt of V_o), and 0.3%/(volt of V_o), respectively.

The internal reference voltage for the *317* and *337* regulators is typically 1.25 V, and V_{ref} appears across the *ADJ* and *output* terminals. Consequently, the regulator output voltage is,

$$V_o = \frac{R_1 + R_2}{R_1} \times V_{REF} \qquad (17\text{-}7)$$



(a) *LM317* positive voltage regulator (b) *LM337* negative voltage regulator

Figure 17-24
Application of the LM317 and LM337 integrated circuit voltage regulators. The internal reference voltage appears across resistor R_1.

To determine suitable values for R_1 and R_2 for a desired output voltage, first select the voltage divider current (I_1) to be much larger than the current that flows in the *ADJ* terminal of the device. This is specified as 100 μA maximum on the device data sheet. The resistors are calculated using the relationship in Eq. 17-7.

Note the capacitors included in the regulator circuits. Capacitor C_{in} is necessary only when the regulator is not located close to the power supply filter circuit. C_{in} eliminates the oscillatory tendencies that can occur with long connecting leads between the filter and regulator. Capacitor C_o improves the transient response of the regulator and ensures *ac* stability, and C_{adj} improves the ripple rejection ratio.

Figure 17-25 shows the terminal connections for *LM317* and *LM337* regulators in *221A*-type packages.

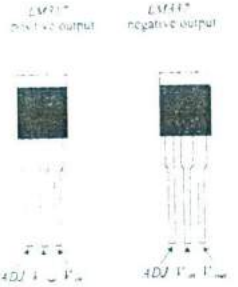


Figure 17-25
Terminal connections for LM317 and LM337 IC regulators contained in 221A packages.

Example 17-10

An *LM317* regulator is to provide a 6 V output from a 15 V supply. The load current is 200 mA. Determine suitable resistance values for R_1 and R_2, (in Fig. 17-24) and calculate the regulator power dissipation.

Solution

$$I_1 >> I_{ADJ}$$

Select $I_1 = 1$ mA

$$R_1 = \frac{V_{ref}}{I_1} = \frac{1.25\text{ V}}{1\text{ mA}}$$

$= 1.25$ kΩ (use 1.2 kΩ standard value)

$$R_2 = \frac{V_o - V_{ref}}{I_1} = \frac{6\text{ V} - 1.25\text{ V}}{1\text{ mA}}$$

$= 4.75$ kΩ (use 4.7 kΩ standard value)

$P_D = (V_S - V_o) \times I_{L(max)} = (15\text{ V} - 6\text{ V}) \times 200\text{ mA}$

$= 1.8$ W

LM340 Regulators

LM340 devices are three-terminal positive voltage regulators with fixed output voltages ranging from a low of 5 V to a high of 23 V. The regulator is selected for the desired output voltage and then simply provided with a voltage (V_S) from a power supply filter circuit, as illustrated in Fig. 17-26. Here again, capacitor C_1 is required only when the regulator is not located close to the filter.

The *LM340* data sheet specifies the regulator performance for an output current of 1 A. The tolerance on the output voltage is ±2%, the line regulation is *0.01% per output volt*, and the load regulation is *0.3% per amp of load current*. The IC includes current limiting, and a thermal shutdown circuit that protects against excessive internal power dissipation. As with all series regulators, a heat sink must be used when high power dissipation is involved.

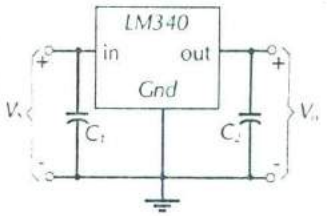


Figure 17-26
The LM340 is a fixed output IC voltage regulator with an output selectable from 5 V to 23 V.

Practise Problems

17-5.1 Design the regulator circuit in Fig. 17-22 to have an 18 V, 200 mA output. Include short circuit protection, and specify Q_2.

17-5.2 Using an *LM317*, design a 9 V, 150 mA voltage regulator. Select a supply voltage, and calculate the regulator power dissipation.

17-6 Switching Regulator Basics

Switching Regulator Operation

A switching regulator can be thought of as similar to a linear regulator, but with the series-pass transistor operating as a switch that is either *off*, or switched *on* (in a saturated state). The output voltage from the switch is a pulse waveform which is smoothed into a *dc* voltage by the action of an *LC* filter.

Switching regulators can be classified as:

- *step-down converter* (output voltage lower than input)
- *step-up converter* (output higher than input)
- *inverting converter* (output polarity opposite to input)

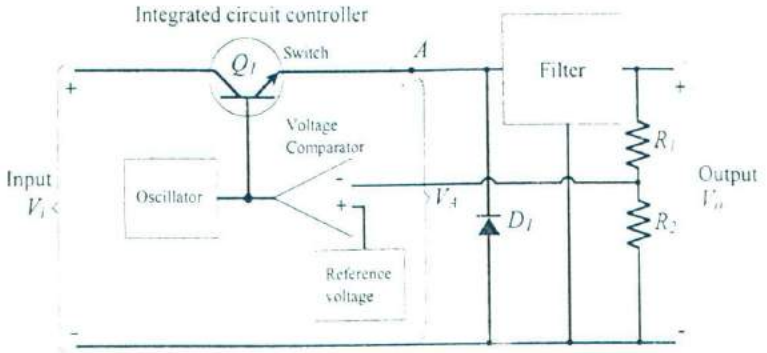


Figure 17-27
A switching regulator has a switch (contained in an IC controller), a filter, and a diode. The switch converts the dc input into a pulse waveform, and the filter smoothes the pulse wave into a direct voltage with a ripple waveform.

The basic block diagram of a step-down switching regulator in Fig. 17-27 consists of a transistor *switch* (Q_1) (also termed a *power switch*), an *oscillator*, a *voltage comparator*, a *voltage reference source*, a *diode* (D_1), and a *filter*. The switch, oscillator, comparator, and reference source are all usually contained within an integrated circuit *controller*, as illustrated. The filter usually consists of an inductor and capacitor. The operation of the regulator is as follows:

- The *dc* input voltage (V_i) is converted into a pulse waveform (V_A) by the action of the switch (Q_1) turning *on* and *off*. This is illustrated by the waveforms in Fig. 17-28.
- The oscillator switches Q_1 *on*, causing current to flow to the filter, and the output voltage to rise.
- The voltage comparator compares the output voltage (divided by R_1 and R_2) to the reference voltage, and it holds Q_1 *on* until V_o equals V_{ref}. Then, Q_1 is turned *off* again.
- The pulse waveform (V_A) at the filter input is produced by Q_1 turning *on* and *off*.
- The filter smoothes the pulse waveform to produce a *dc* output voltage (V_o) with a *ripple* waveform (V_r).
- The ripple waveform is the result of the filter capacitor charging via the filter inductor during t_{on}, and then discharging to the load during t_{off} via D_1. (The is further explained in Section 17-7.)

In the operation described above, the controller can be thought of as a *pulse width modulator*; the *on* time of Q_1 (*pulse width* of its output) is increased or decreased as necessary to supply the required output current. Other systems involve control of the switch *off* time.

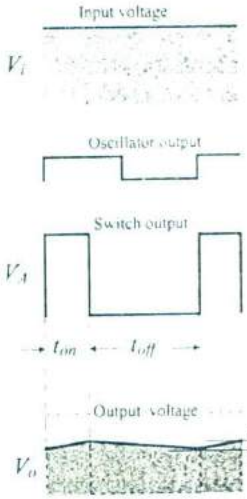


Figure 17-28
Switching regulator waveforms. The switch output is a pulse waveform, and the filter output is a dc voltage with a ripple.

Comparison of Linear and Switching Regulators

The power dissipated in the series-pass transistor in a linear regulator is wasted power. This is not very important when the load current is lower than 500 mA. With high current levels, the regulator efficiency becomes important, and there can also be serious heat dissipation problems.

In a switching regulator, the power dissipation in the switching transistor (whether it is *on* or *off*) is very much smaller than in the

series-pass transistor of a linear regulator with a similar output voltage and load current. So, a switching regulator is more efficient than a linear regulator.

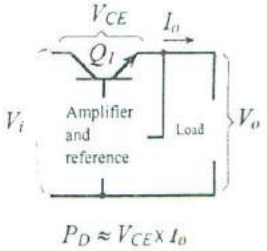
The approximate efficiency of a linear regulator can be calculated by assuming that the only wasted power (P_D) is that dissipated in the series-pass transistor, [see Fig. 17-29(a)].

$$P_i \approx P_o + (V_{CE} \times I_o) \qquad \textbf{(17-8)}$$

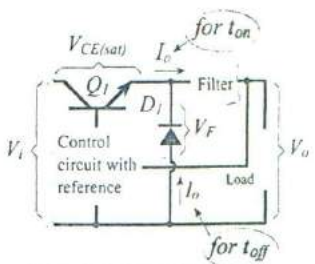
To estimate the efficiency of a switching regulator, it should be noted that D_1 (in Fig. 17-27) is biased *off* when Q_1 is *on*, and that D_1 is *on* when Q_1 is *off*. So, the power dissipated in the switching transistor and diode can be taken as the total wasted power, [Fig. 17-29(b)]. The Q_1 and D_1 power dissipations can be calculated in terms of the actual current level in each device and the *on* and *off* times. This analysis shows that P_D for each device is simply [(average output current) x (device voltage drop)]. So,

$$P_i \approx P_o + I_o(V_{CE(sat)} + V_F) \qquad \textbf{(17-9)}$$

As discussed, there is much less power dissipation in the transistor and diode in a switching regulator than in the series-pass transistor of a linear regulator with the same output conditions. So, a lower power transistor can be used in the switching regulator. Also, with a switching regulator there is usually no need for the heat sink normally required with a series regulator. Example 17-11 compares switching and linear regulators with similar load requirements.



(a) Linear regulator



(b) Switching regulator

Figure 17-29
Comparison of power dissipated in linear and switching regulators.

Example 17-11

Calculate the efficiencies of a linear regulator and a switching regulator that each supply 10 V, 1 A loads. The series-pass transistor of the linear regulator has $V_{CE} = 7$ V. The switching regulator has $V_{CE(sat)} = V_F = 1$ V.

Solution

$$P_o = V_o \times I_o = 10\text{ V} \times 1\text{ A}$$
$$= 10\text{ W}$$

Linear Regulator

Eq. 17-8,
$$P_i \approx P_o + (V_{CE} \times I_o) = 10\text{ W} + (7\text{ V} \times 1\text{ A})$$
$$= 17\text{ W}$$

$$\text{Efficiency} = \frac{P_o \times 100\%}{P_i} = \frac{10\text{ W} \times 100\%}{17\text{ W}}$$
$$= 59\%$$

Switching Regulator

Eq. 17-9,
$$P_i \approx P_o + I_o(V_{CE(sat)} + V_f) = 10\text{ W} + 1\text{ A}\,(1\text{ V} + 1\text{ V})$$
$$= 12\text{ W}$$

$$\text{Efficiency} = \frac{P_o \times 100\%}{P_i} = \frac{10\ \text{W} \times 100\%}{12\ \text{W}}$$
$$= 83\%$$

The efficiency calculations in this example are approximate, because power dissipations in other parts of the circuits are neglected.

As well as efficiency, there are other considerations in the choice between linear and switching regulators. The output ripple voltage with a switching regulator is substantially larger than with a linear regulator. The line effect can be similar with both types of regulator, but the load effect is usually largest with a switching regulator. For low levels of output power, a switching regulator is usually more expensive than a linear regulator. A linear regulator is usually the best choice for output power levels up to 10 W. A switching regulator should be considered when the output is above 10 W. Table 17-1 compares the two voltage regulator types.

Table 17-1 Comparison of linear and switching regulator performance.

	Linear Regulator	Switching Regulator
Typical Efficiency	30% to 70%	85%
Line Effect	< 10 mV	< 10 mV
Load Effect	< 10 mV	> 50 mV
Ripple Voltage	< 10 mV (120 Hz)	100 mV (10 kHz to 200 kHz)

Practise Problems

17-6.1 Calculate the approximate efficiencies of linear and switching voltage regulators which each supply a 15 V, 750 mA load. The input voltage to both regulators is V_i = 21 V. The switching regulator uses a *FET* with a drain-source resistance of $r_{DS(on)}$ = 0.6 Ω as the power switch, and a diode with V_f = 0.7 V

17-7 Step-Down, Step-Up, and Inverting Converters

Step-Down Converter

A *step-down* switching regulator, or *step-down converter* (also termed a *buck* converter), produces a *dc* output voltage lower than its input voltage. The basic circuit arrangement for a step-down converter is shown in Fig. 17-30. Note the presence of the *catch diode* (D_1). This is normally reverse biased when Q_1 is *on*, but becomes forward biased when Q_1 switches *off*.

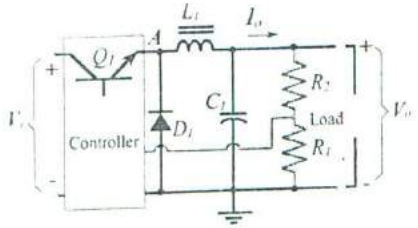
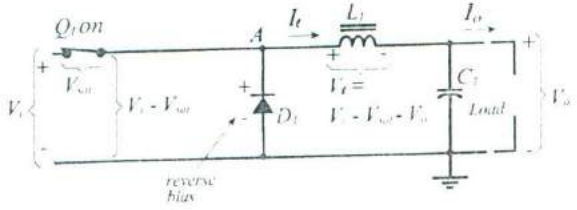
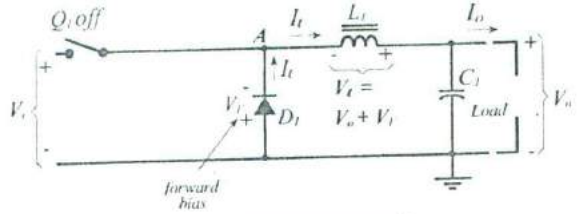


Figure 17-30
Step-down converter circuit.

Figure 17-31(a) illustrates the situation when Q_1 is *on* (in saturation). Inductor current (I_ℓ) flows from V_i, producing an inductor voltage drop (V_ℓ) which is + on the left, - on the right. At this time D_1 is reverse biased. When Q_1 switches *off* [Fig. 17-31(b)], the inductor has stored energy, and it opposes any change in current level. In order to maintain inductor current flow (with Q_1 *off*), the inductor voltage reverses, becoming - on the left, + on the right, as illustrated. The reversed polarity of V_ℓ forward biases D_1 to provide a path for I_ℓ. If D_1 was not present in the circuit, the inductor voltage would become large enough to break down the junctions of Q_1. So, D_1 *catches* V_ℓ and stops it from increasing; hence the name *catch diode*.



(a) Circuit conditions with Q_1 *on*



(b) Circuit conditions with Q_1 *off*

Figure 17-31
In a step-down converter, inductor current I_ℓ flows while Q_1 is on, producing a voltage drop (V_ℓ). When Q_1 switches off, V_ℓ reverses and D_1 becomes forward biased to keep I_ℓ flowing.

Step-Down Converter Equations

Figure 17-32 shows the circuit waveforms during the Q_1 *on* and *off* times (t_{on} and t_{off}). These are; switch voltage (V_A) at *point A* (Q_1 emitter), inductor voltage (V_ℓ), inductor current (I_ℓ), and output voltage (V_o). Equations for calculating component values can be derived by considering the circuit conditions and the waveforms.

The input voltage (V_i) appears at the collector of transistor Q_1. When Q_1 is *on*, the voltage across the inductor and capacitor (in series) is (V_i - V_{sat}), and the inductor voltage is (V_i - V_{sat} - V_o), [see Fig. 17-31(a)]. When Q_1 switches *off*, the inductor voltage becomes

$(V_o + V_F)$. [Fig. 17-31(b)]. Typically, $V_F = 0.7$ V, and V_{sat} ranges from 0.2 V to 1.5 V, depending on the transistor and the load current. The energy supplied *to the inductor* during t_{on} is proportional to $[t_{on} \times (V_i - V_{sat} - V_o)]$, and the energy supplied *by the inductor* to the output during t_{off} is proportional to $[t_{off} \times (V_o + V_F)]$. Because the inductor input energy must equal its output energy,

$$t_{on}(V_i - V_{sat} - V_o) = t_{off}(V_o + V_F)$$

giving,
$$\frac{t_{on}}{t_{off}} = \frac{V_o + V_F}{V_i - V_{sat} - V_o} \qquad \textbf{(17-10)}$$

From Fig. 17-32,

$$t_{on} + t_{off} = T = 1/f \qquad \textbf{(17-11)}$$

The inductor is charged from the supply via Q_1 during t_{on}, and it discharges to the load and the output capacitor via D_1 during t_{off}. When the output current is a maximum ($I_{o(max)}$), the inductor current (I_l) can be allowed to change from zero to a peak level.

$$I_p = 2\, I_{o(max)} \qquad \textbf{(17-12)}$$

This is the absolute maximum inductor current change ($\Delta I = I_p$) that can occur when the circuit is operating correctly.

An equation for the inductance may be derived from a knowledge of the inductor voltage and the inductor current change during t_{on}.

$$L = \frac{e_L \Delta t}{\Delta I}$$

Giving,
$$L_{1(min)} = \frac{(V_i - V_{sat} - V_o)\, t_{on}}{I_p} \qquad \textbf{(17-13)}$$

The output voltage waveform (Fig. 17-32) is also the capacitor voltage waveform. As illustrated, the capacitor voltage increases while I_l is greater than I_o, and decreases during the time that I_l is less than I_o. While I_l is less than I_o, the average inductor current is $\Delta I/4$ below I_o, and the capacitor must supply this current to the load. The time involved is $T/2$, and the capacitor voltage change is the peak-to-peak output ripple voltage (V_r). So, an equation for the minimum capacitance of C_1 can be derived as,

$$C_1 = \frac{I\, t}{\Delta V} = \frac{(\Delta I/4) \times T/2}{V_r}$$

or,
$$C_{1(min)} = \frac{I_p}{8 f V_r} \qquad \textbf{(17-14)}$$

It should be noted that Equations 17-13 and 17-14 give minimum inductor and capacitor values. The use of component values larger than the minimum will result in a lower ripple voltage at the regulator output.

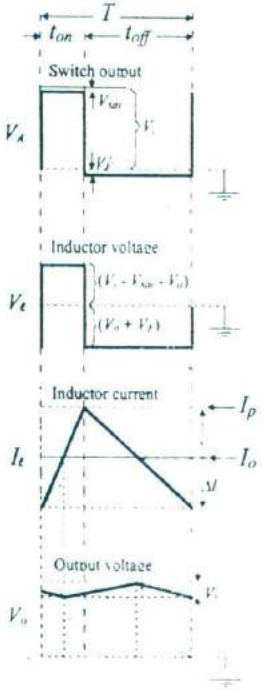


Figure 17-32
Step-down converter waveforms.

When selecting components, the capacitor *equivalent series resistance* (*ESR*) and the inductor *winding resistance* (R_W) must be taken into account. *ESR* can affect the output ripple voltage. The maximum *ESR* should usually be limited to ($0.1\ V_r/\Delta I$). If R_W is too large, it will produce an excessive voltage drop across the inductor. The maximum winding resistive voltage drop should typically not exceed 0.2 V. Also, the peak level of the inductor current must be passed without saturating the core.

Resistance values for R_1 and R_2 (in Fig. 17-30) depend on the output and reference voltages. This is treated in Section 17-8.

Example 17-12

A switching regulator with a 30 V input is to have a 12 V, 500 mA output with a 100 mV maximum ripple. The switching frequency is to be 50 kHz. Calculate the minimum filter components values. Assume that $V_{sat} = 1$ V.

Solution

$$T = \frac{1}{f} = \frac{1}{50\ \text{kHz}}$$

$$= 20\ \mu\text{s}$$

Eq. 17-10,
$$\frac{t_{on}}{t_{off}} = \frac{V_o + V_f}{V_i - V_{sat} - V_o} = \frac{12\ \text{V} + 0.7\ \text{V}}{30\ \text{V} - 1\ \text{V} - 12\ \text{V}}$$

$$= 0.75$$

or,
$$t_{on} = 0.75\, t_{off}$$

Eq. 17-11,
$$T = t_{on} + t_{off} = 0.75\, t_{off} + t_{off}$$

or,
$$t_{off} = \frac{T}{1.75} = \frac{20\ \mu\text{s}}{1.75}$$

$$\approx 11.4\ \mu\text{s}$$

$$t_{on} = T - t_{off} = 20\ \mu\text{s} - 11.4\ \mu\text{s}$$

$$= 8.6\ \mu\text{s}$$

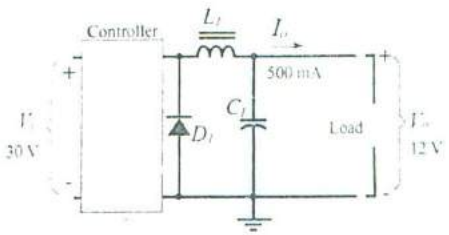


Figure 17-33
Step-down converter circuit for Example 17-12.

Eq. 17-12,
$$I_p = 2\, I_{o(max)} = 2 \times 500\ \text{mA}$$

$$= 1\ \text{A}$$

Eq. 17-13,
$$L_{1(min)} = \frac{(V_i - V_{sat} - V_o)\, t_{on}}{I_p} = \frac{(30\ \text{V} - 1\ \text{V} - 12\ \text{V}) \times 8.6\ \mu\text{s}}{1\ \text{A}}$$

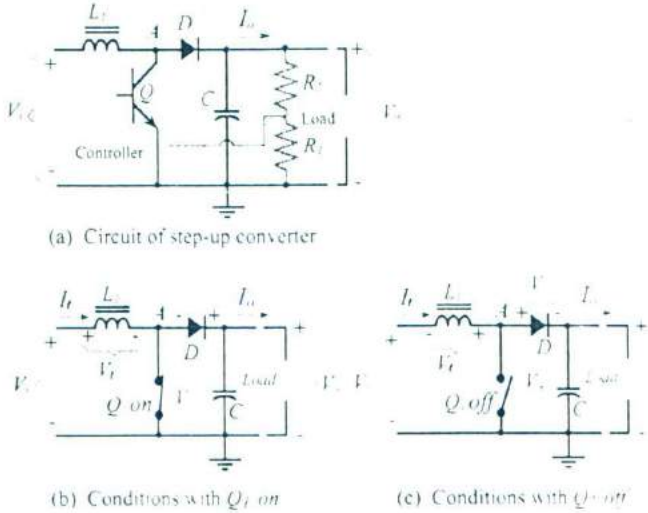
$$= 146\ \mu\text{H}$$

Eq. 17-14,
$$C_{1(min)} = \frac{I_p}{8\, f\, V_r} = \frac{1\ \text{A}}{8 \times 50\ \text{kHz} \times 100\ \text{mV}}$$

$$= 25\ \mu\text{F}$$

Step-Up Converter

A *step-up converter*, or *boost converter*, produces a *dc* output voltage higher than its supply voltage. In the circuit shown in Fig. 17-34(a), L_1 is directly connected to the supply, and D_1 is in series with L_1 and C_1. The collector of Q_1 is connected to the junction of L_1 and D_1 (*point A*), and its emitter is grounded.



(a) Circuit of step-up converter

(b) Conditions with Q_1 *on*

(c) Conditions with Q_1 *off*

Figure 17-34
In a step-up converter circuit, the inductor current I_L flows while Q_1 is on, producing V_L. When Q_1 switches off, V_L reverses and D_1 becomes forward biased. The output voltage is $V_o = V_i + V_L$.

When Q_1 is *on* [Figure 17-34(b)], D_1 is reverse biased, and

$$V_L = V_i - V_{sat}$$

When Q_1 is *off* [Figure 17-34(c)], V_L reverses polarity to keep I_L flowing. The output voltage is now,

$$V_o = V_i + V_L - V_F$$

So, the output voltage is larger than the input, and its actual level can be set by selection of R_1 and R_2 [in Fig. 17-34(a)].

The voltage at *point A* has the pulse waveform (V_A) illustrated in Fig. 17-35. During t_{on} (Q_1 *on* time), $V_A = V_{sat}$, and during t_{off}, $V_A = (V_i + V_L)$. The inductor current increases to I_p during t_{on}, and decreases during t_{off} as L_1 discharges to C_1 and the load. The output voltage (V_o across C_1) decreases during t_{on}, because D_1 is reverse biased and C_1 is supplying all the load current. During t_{off}, D_1 is forward biased and C_1 is recharged from L_1. V_o increases while I_L is greater than I_o, and decreases when I_L is less than I_o.

From the circuit conditions and the waveforms, the following equations can be derived:

$$\frac{t_{on}}{t_{off}} = \frac{V_o + V_F - V_i}{V_i - V_{sat}} \qquad \textbf{(17-15)}$$

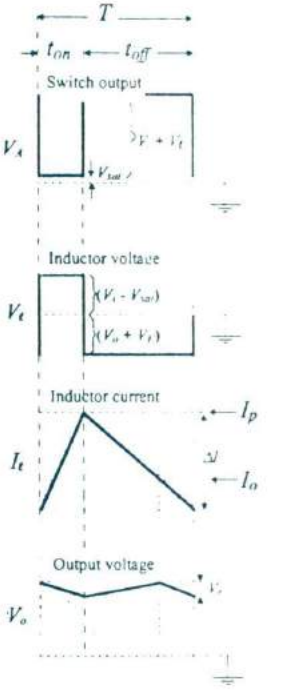
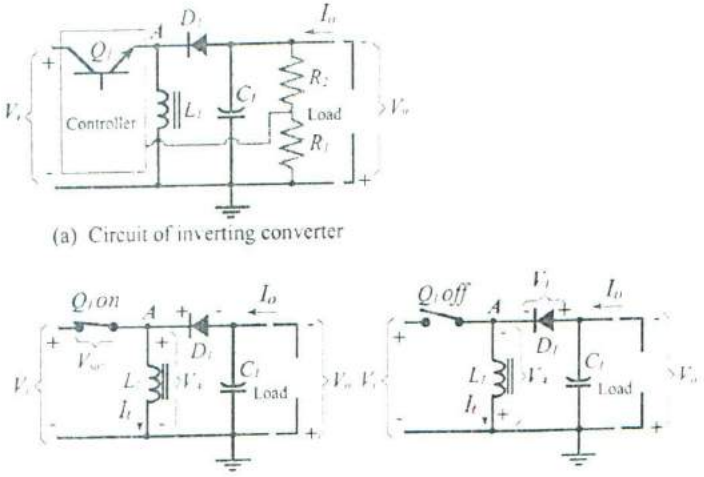


Figure 17-35
Step-up converter circuit waveforms.

$$I_p = \frac{2\,T\,I_{o(max)}}{t_{off}} \qquad \textbf{(17-16)}$$

$$L_{1(min)} = \frac{(V_i - V_{sat})\,t_{on}}{I_p} \qquad \textbf{(17-17)}$$

$$C_{1(min)} = \frac{t_{on}\,I_{o(max)}}{V_r} \qquad \textbf{(17-18)}$$



(a) Circuit of inverting converter

(b) Conditions with Q_1 *on*

(c) Conditions with Q_1 *off*

Figure 17-36
In an inverting converter circuit, the Inductor current I_t flows while Q_1 is on, producing V_t. When Q_1 switches off, V_t reverses and D_1 becomes forward biased. The output voltage is $-(V_t - V_F)$.

Inverting Converter

Figure 17-36(a) shows the circuit of an *inverting converter*, (also termed a *flyback converter*). This circuit produces a negative *dc* output voltage from a positive supply voltage. In this case, L_1 is connected between ground and the emitter terminal of Q_1. (*point A*). Diode D_1 is in series with Q_1 emitter and C_1. Note the polarity of D_1 and output capacitor C_1.

Figure 17-36(b) shows that when Q_1 is *on*, D_1 is reverse biased, and

$$V_A = V_t = V_i - V_{sat}$$

From Fig. 17-36(c), when Q_1 is *off* V_t reverses to keep I_t flowing. Diode D_1 is now forward biased, giving

$$V_o = -(V_t - V_F)$$

The output voltage is negative, and once again the actual output voltage level is set by selection of R_1 and R_2.

The voltage at *point A* in Fig. 17-36 is also the inductor voltage, and it has the pulse waveform shown in Fig. 17-37. During t_{on}, $V_A = (V_i - V_{sat})$; and during t_{off}, $V_A = -(V_o + V_F)$. As in other switching converters, the inductor current increases to I_p during t_{on} and

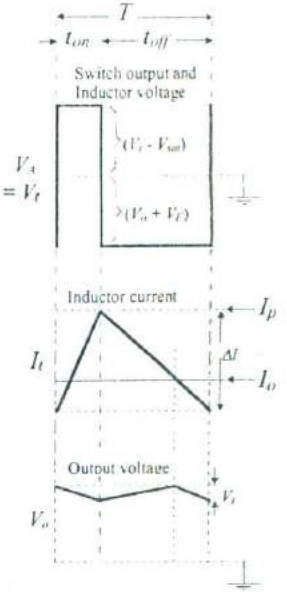


Figure 17-37
Inverting converter circuit waveforms.

decreases during t_{off}, discharging to C_1 and the load. V_o decreases during t_{on} (D_1 reverse biased) as C_1 supplies all of I_o. Then, C_1 is recharged from L_1 during t_{off} (D_1 forward biased), and V_o increases while I_t exceeds I_o, and decreases while I_t is less than I_o.

For the inverting converter,

$$\frac{t_{on}}{t_{off}} = \frac{V_o + V_F}{V_i - V_{sat}} \qquad \textbf{(17-19)}$$

Equations 17-16, 17-17, and 17-18 apply for the inverting converter, as well as for the step-up converter.

Practise Problems

17-7.1 A switching regulator with $V_i = 20$ V and $f = 30$ kHz is to produce a 5 V, 1 A output with a 200 mV ripple. Assuming that $V_{sat} = 0.5$ V and $V_F = 0.7$ V, determine minimum filter component values.

17-7.2 A switching regulator is to have $V_i = 5$ V, $V_o = 9$ V, $I_{o(max)} = 600$ mA, $f = 30$ kHz, and $V_r = 200$ mV. Determine minimum filter component values. Assume that $V_{sat} = 0.5$ V and $V_F = 0.7$ V.

17-8 IC Controller for Switching Regulators

Functional Block Diagram

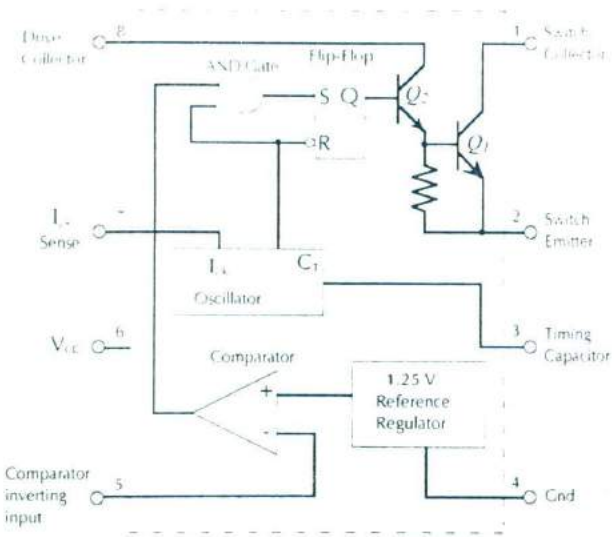


Figure 17-38
Motorola MC34063 switching regulator controller functional block diagram.
(Courtesy of Motorola Inc.)

The functional block diagram of a *MC34063* integrated circuit controller is shown in Fig. 17-38. This *IC* is designed to be used as a variable *off* time switching regulator. The components parts of the diagram in Fig. 17-38 are:

- *Switching transistor* (Q_1) controlled by transistor Q_2.
- *Set-reset flip-flop* with input terminals *S* and *R*, and output *Q*.

- *AND gate* that controls Q_1 and Q_2 by controlling the flip-flop.
- *Oscillator* that generates a square wave output at the desired switching frequency. The oscillator frequency is set by an externally-connected timing capacitor (C_T) at terminal 3.
- *Current limiter* terminal (I_{pk} *sense*). This input to the oscillator permits Q_1 to be turned *off* via the reset terminal of the flip-flop.
- *Comparator* for comparing the output and reference voltages.
- *Reference voltage source* (1.25 V).

Step-Down Converter Using an MC34063

Figure 17-39 shows an *MC34063* connected to function as a step-down converter. The positive terminal of the supply is connected to terminal *6*, and the negative (grounded) terminal is connected to terminal *4*. Note that a 100 µF capacitor (C_2) is connected from terminal *6* to ground (right at the *IC* terminals) to smoothe supply-line pulses that result from fast load current changes.

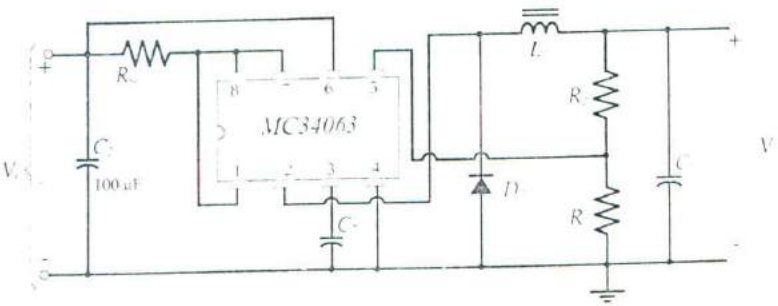


Figure 17-39
Step-down switching converter circuit using an MC34063 controller

The supply voltage (V_i) is connected (via R_{SC}) to the collectors of Q_1 and Q_2 at terminals *8* and *1*, (see Fig. 17-38). Resistor R_{SC} (connected to terminal *7*) senses the peak supply current (I_S) and provides a voltage drop to turn Q_1 *off* when the current exceeds the maximum design level. The equation for the current-limiting resistor is given on the device data sheet as,

$$R_{SC} = \frac{0.33\ \text{V}}{I_P} \qquad \textbf{(17-20)}$$

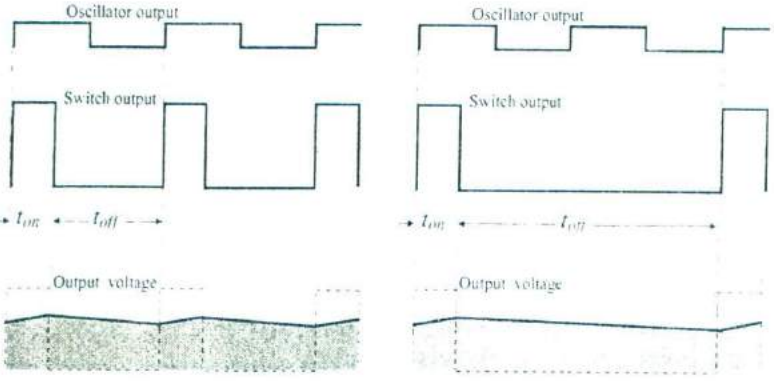
The output voltage (V_o) is divided across resistors R_1 and R_2 and applied to the inverting input of the voltage comparator to compare it to the reference voltage (V_{ref}). The voltage across R_1 must be equal to the V_{ref} when the circuit is operating correctly, and the voltage across ($R_1 + R_2$) equals V_o. As in all voltage divider designs, the resistor current should be much larger than the device input bias current; the comparator input current in this case.

The timing capacitor (C_T), connected from terminal 3 to ground, is selected for the desired *on* time of the switching transistor. An equation for the capacitance of C_T is given on the *IC* data sheet:

$$C_T = 4.8 \times 10^{-5} \times t_{on} \qquad \textbf{(17-21)}$$

Variable Off Time Modulator

Switching converter circuits are designed to supply a particular maximum load current. For a converter circuit using an *MC34063* controller, the circuit waveforms are typically as shown in Fig. 17-40(a) when supplying *full load current*. Transistor Q_1 (in Fig. 17-38) is switched *on* at the start of the each cycle of the oscillator square wave output. Also, t_{on} and t_{off} add up to the time period (T) of the oscillator, as illustrated. When the *load current is low*, capacitor C_1 discharges more slowly than when supplying full load current, [see Fig. 17-40(b)]. So, V_{R1} (in Fig. 17-39) has not dropped below V_{ref} by the beginning of the next cycle of the oscillator square wave. Consequently, Q_1 is *not* switched *on* again at this point, and so the pulse waveform frequency at Q_1 emitter is now lower than the oscillator frequency. A switching converter controller designed to operate in this way is known as a *variable off-time modulator*.



(a) Waveforms for high load current

(b) Waveforms for lower load current

Figure 17-40
Waveforms for high-current and low-current conditions in a variable off-time controller for a switching regulator.

Example 17-13

A *MC34063* controller is to be used with the step-down switching regulator designed in Ex. 17-12, as in Fig. 17-39. Determine suitable component values for R_1, R_2, R_{SC}, and C_T.

Solution

$I_1 >>$ [comparator input bias current (I_B)]

I_B = -400 nA (from the *IC* data sheet)

Select, $I_1 = 1$ mA

$$R_1 = \frac{V_{ref}}{I_1} = \frac{1.25\text{ V}}{1\text{ mA}}$$

$$= 1.25\text{ k}\Omega \text{ (use 1.2 k}\Omega\text{ standard value)}$$

I_1 becomes, $$I_1 = \frac{V_{ref}}{R_1} = \frac{1.25\text{ V}}{1.2\text{ k}\Omega}$$

$= 1.04\ \text{mA}$

$$R_2 = \frac{V_o - V_{ref}}{I_1} = \frac{12 - 1.25\ \text{V}}{1.04\ \text{mA}}$$

$= 10.34\ \text{k}\Omega$ [use (10 kΩ + 330 Ω) standard values]

Eq. 17-20, $$R_{SC} = \frac{0.33\ \text{V}}{I_p} = \frac{0.33\ \text{V}}{1\ \text{A}}$$

$= 0.33\ \Omega$ (special low-value resistor)

Eq. 17-21, $C_1 = 4.8 \times 10^{-5} \times t_{on} = 4.8 \times 10^{-5} \times 8.6\ \mu\text{s}$

$= 413\ \text{pF}$ (use 430 pF standard value)

Catch Diode Selection

The diode power dissipation can be calculated approximately from the output current and the diode voltage drop:

$$P_{D1} \approx I_o \times V_F \qquad \textbf{(17-22)}$$

The reverse recovery time (t_{rr}) of the diode should be less than one tenth of the minimum diode *on* or *off* time, which ever is smaller:

$$t_{rr} < 0.1\ (t_{on(min)}\ \textbf{or}\ t_{off(min)}) \qquad \textbf{(17-23)}$$

Diode Snubber

A *diode snubber* is a series *RC* circuit connected across the catch diode to suppress high frequency *ringing* that can be produced by resonance of the inductance and capacitance of components and connecting leads. (Termed *parasitic* inductance and capacitance.) A diode snubber circuit is shown in Fig. 17-41. The capacitance of C_s is usually selected in the range of four to ten times the diode junction capacitance (C_J), and then the resistance of R_s is calculated from C_s and the ringing frequency (f_r).

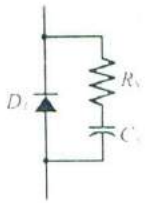


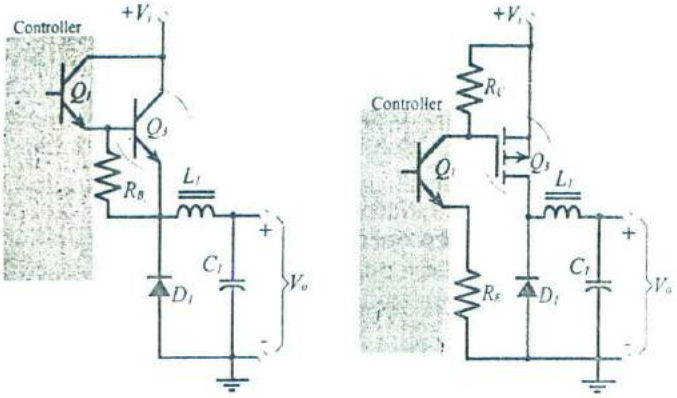
Figure 17-41
A series RC circuit connected in parallel with a diode (a diode snubber circuit) is often used to suppress high frequency ringing.

$$C_s = (4 \text{ to } 10) \times C_D \qquad \textbf{(17-24)}$$

$$R_s C_s = \frac{1}{f_r} \qquad \textbf{(17-25)}$$

High Power Converters

When the load current of a switching regulator is too high for the controller internal transistor, an externally-connected device can be employed. Figure 17-42(a) illustrates how a high-power *BJT* (Q_3) should be connected for use with a step-down converter, and Fig. 17-42(b) shows how an external *FET* should be connected. Resistor R_B at the base of Q_3 in Fig. 17-42(a) ensures that Q_3 is biased *off* when Q_1 switches *off*. For the *p*-channel *MOSFET* (Q_3) In Fig. 17-43(b), resistors R_C and R_E are selected to give a gate-channel voltage (V_{RC}) that will switch Q_3 *on* when Q_1 is *on*.



(a) Use of external *BJT* (b) External *MOSFET* connection

Figure 17-42
When the peak current is too high for an IC switching converter controller, an external power device can be connected to pass higher current levels.

Practise Problems

17-8.1 The step-down switching regulator designed for Problem 17-7.1 is to use an *MC34063* controller. Determine suitable values for the additional components.

17-8.2 The step-up switching regulator designed for Problem 17-7.2 is to use an *MC34063* controller. Determine suitable values for the additional components.

Chapter-17 Review Questions

Section 17-1

17-1 Sketch the circuit of an emitter follower voltage regulator. Explain the operation of the circuit, and discuss the effect of the transistor on the performance of the regulator.

17-2 Sketch the circuit of a series regulator with a one-transistor error amplifier. Explain the operation of the circuit, and discuss the effect of the error amplifier on the performance of the regulator.

Section 17-2

17-3 Show how the regulator circuit in Question 17-2 should be modified to produce an adjustable output voltage. Explain.

17-3 Show how the regulator in Question 17-2 should be modified to handle a large load current. Explain.

17-4 Show how voltage regulator performance may be improved by the use of a preregulator. Explain how the circuit performance is improved.

17-5 Show how a constant-current source may be used instead of a preregulator to improve the performance of a voltage regulator. Explain the operation of the circuit, and discuss

how the performance of the regulator is improved.

17-6 Sketch the complete circuit of a transistor voltage regulator that uses a differential amplifier. Explain the operation of the circuit and discuss its performance.

Section 17-3

17-7 Sketch a simple current limiting circuit for short-circuit protection on a voltage regulator. Explain the operation of the circuit, and sketch the V_o/I_L characteristic for the regulator. Discuss the effects of current limiting on the series-pass transistor.

17-8 Sketch a foldback current limiting circuit for a voltage regulator. Sketch the V_o/I_L characteristic, and explain the operation of the circuit.

17-9 Write equations for power dissipation in the series pass transistor in voltage regulators using (a) simple current limiting, (b) foldback current limiting. Compare the two current limiting methods.

Section 17-4

17-10 Sketch the circuit of a voltage follower regulator using an *IC* operational amplifier. Explain the circuit operation.

17-11 Compare the performance of an *IC* op-amp voltage regulator to the performance of an emitter follower voltage regulator.

17-12 Sketch the circuit of a series regulator that uses an *IC* operational amplifier as an error amplifier. Explain the circuit operation.

17-13 For an *IC* op-amp series regulator, write equations for V_o in terms of V_Z. Briefly discuss the supply voltage requirements.

Section 17-5

17-14 Sketch the basic circuit of a *723 IC* voltage regulator. Briefly explain.

17-15 Sketch a *723 IC* voltage regulator connected to function as a positive voltage regulator with V_o greater than V_{ref}. Write an equation for V_o in terms of V_{ref}. Briefly discuss the required supply voltage.

17-16 Sketch a regulator circuit that uses an *LM317 IC* positive voltage regulator. Briefly explain.

17-17 Sketch a regulator circuit that uses an *LM337 IC* negative voltage regulator. Briefly explain.

17-18 Sketch a regulator circuit that uses an *LM340 IC* fixed voltage regulator. Briefly explain.

Section 17-6

17-19 Draw a basic block diagram and waveforms for a switching regulator. Explain its operation.

17-20 Compare switching regulators and linear regulators.

Section 17-7

17-21 Sketch the basic circuit for a step-down switching regulator. Draw current and voltage waveforms, and explain the circuit operation.

17-22 Repeat Question 17-21 for a step-up switching regulator.

17-23 Repeat Question 17-21 for an inverting switching regulator.

Section 17-8

17-24 Sketch the functional block diagram for an *MC34063* controller for a switching regulator. Briefly discuss each item in the block diagram.

17-25 Sketch the circuit of a step-up switching regulator using an *MC34063* in a similar form to Fig. 17-39.

17-26 Sketch the circuit of an inverting switching regulator using an *MC34063* in a similar form to Fig. 17-39.

17-27 Sketch a diode snubber circuit, and briefly explain.

17-28 Draw circuits to show how an external *BJT* and an external *FET* should be connected for use with step-down converters. Briefly explain.

Chapter-17 Problems

Section 17-1

17-1 Using a 15 V supply and a transistor with $h_{FE(min)} = 50$, design a voltage follower regulator circuit (as in Fig. 17-1) to give a 9 V output with a 100 mA maximum load current.

17-2 Calculate the line regulation, load regulation, and ripple rejection ratio for the circuit designed for Problem 17-1.

17-3 A regulator circuit as in Fig. 17-1 has: $V_Z = 7$ V, $R_1 = 560\ \Omega$, $R_E = 8.2\ k\Omega$, $R_L = 180\ \Omega$. $V_S = 19$ V when $I_L = 0$, and $V_S = 18$ V when $I_L = 35$ mA. The transistor has $h_{FE} = 60$. Calculate the Q_1 emitter current and the Zener diode current when the load is connected and when the load is disconnected.

17-4 Determine the line and load regulations for the regulator in Problem 17-3. Assume that $Z_Z = 5\ \Omega$.

17-5 Measurements on a voltage regulator with $V_S = 25$ V and $V_o = 18$ V give the following results: (when I_L changes from zero to 200 mA, $\Delta V_S = 2$ V, and $\Delta V_o = 10$ mV), (when $\Delta V_S = \pm 2.5$ V, $\Delta V_o = \pm 12.5$ mV). Calculate the source effect, load effect, line regulation, and load regulation.

17-6 Determine the voltage gain of the error amplifier in Problem 17-5, and estimate the output ripple voltage amplitude if there is a 2 V peak-to-peak input ripple.

17-7 A series regulator circuit as in Fig. 17-2 is to have a 15 V output and a 50 mA maximum load current. Select a suitable minimum supply voltage and design the circuit.

17-8 Design a voltage regulator circuit as in Fig. 17-2 to produce a 9 V output with a 30 mA maximum load current.

17-9 For the regulator designed for Problem 17-7, calculate the approximate line regulation, load regulation, and ripple reduction, if V_S drops by 1 V from zero to full load current.

17-10 Determine the approximate line regulation, load regulation, and ripple reduction for the regulator designed for Problem 17-8. Assume that $\Delta V_S = 1$ V when $\Delta I_L =$ full load current.

Section 17-2

17-11 Modify the circuit designed for Problem 17-7 to make the output adjustable from 12 V to 15 V.

17-12 Modify the regulator designed for Problem 17-8 to make the output adjustable from 8 V to 10 V.

17-13 Modify the regulator designed for Problem 17-7 to supply a maximum load current of 210 mA. Assume that all transistors used have $h_{FE} = 30$.

17-14 Modify the regulator designed for Problem 17-8 to supply a maximum load current of 300 mA. Assume that $h_{FE1} = 20$ and $h_{FE3} = 100$.

17-15 Design a series voltage regulator with a one-transistor error amplifier to provide an output adjustable from 15 V to 18 V. The load current is to be 250 mA. Assume that all transistors have $h_{FE} = 50$.

17-16 Calculate the line and load regulations for the modified regulator circuit in Problem 17-14. Assume that $\Delta V_S = 1$ V when $\Delta I_L =$ full load current.

17-17 Design a preregulator for the circuit designed for Problem 17-7 and modified for Problem 17-13.

17-18 Determine the approximate line regulation, load regulation, and ripple reduction for the modified regulator in Problem 17-17. Assume that $\Delta V_S = 1$ V when $\Delta I_L =$ full load current.

17-19 The preregulator in the circuit referred to in Problem 17-17 is to be replaced with a constant-current source. Design the constant-current source.

17-20 Design a differential amplifier as in Fig. 17-12 to use with the regulator designed for Problem 17-15.

Section 17-3

17-21 Design a current limiting circuit as in Fig. 17-13(a), to limit the maximum load current to approximately 220 mA for the regulator in Problem 17-13. Calculate the power dissipation in the series pass transistor at I_{SC}.

17-22 Design a foldback current limiting circuit. as in Fig. 17-14(a). to set $I_{L(max)}$ to approximately 220 mA and I_{SC} to approximately 150 mA for the regulator in Problem 17-13. Calculate the power dissipation in the series-pass transistor at $I_{L(max)}$ and at I_{SC}.

17-23 The current limiting circuit in Fig. 17-14(a) has $R_{10} = 1.6\,\Omega$, $R_{11} = 2.7\,k\Omega$, and $R_{12} = 47\,k\Omega$. If the normal output level is 20 V, calculate $I_{L(max)}$ and I_{SC}.

Section 17-4

17-24 Design an op-amp voltage regulator to have $V_o = 15$ V and $I_{L(max)} = 120$ mA. Use a *741 IC* operational amplifier.

17-25 Design a voltage regulator using a *741 IC* operational amplifier to have V_o adjustable from 9 V to 12 V and to deliver a maximum load current of 60 mA.

17-26 Design an op-amp series voltage regulator to provide an output voltage adjustable from 15 V to 18 V. The load current is to be 300 mA. Use a *741* op-amp, and assume that the transistors all have $h_{FE} = 60$.

17-27 For the regulator designed for Problem 17-25, calculate the approximate line regulation, load regulation, and ripple reduction, if V_S drops by 1 V from zero to full load current.

Section 17-5

17-28 Calculate R_1, R_2, and R_3 for the *723 IC* positive voltage regulator circuit in Fig. 17-21. V_o is to be 25 V, and $I_{L(max)}$ is to be approximately 55 mA. Select a suitable supply voltage.

17-29 A regulator circuit using a *723 IC* is to be designed to provide V_o adjustable from 15 to 20 V. Design the circuit, select a suitable input voltage, and calculate the maximum load current that can be supplied.

17-30 The *LM317* positive voltage regulator in Fig. 17-24(a) is to produce an 8 V output of with $I_{L(max)} = 100$ mA. Calculate suitable resistances for R_1 and R_2, select an appropriate supply voltage, and determine the device power dissipation.

17-31 The *LM317* negative voltage regulator in Fig. 17-24(b) is to produce a 12 V output with $I_{L(max)} = 80$ mA. Calculate suitable resistances for R_1 and R_2, select an appropriate supply voltage, and determine the *IC* power dissipation.

Section 17-6

17-32 Calculate the approximate efficiency of the linear regulator in Problem 17-24. Also calculate the approximate efficiency of a switching regulator with similar supply and load conditions. Assume that the switching transistor has $V_{(sat)} = 0.5$ V, and that the switching diode has $V_F = 0.7$ V.

17-33 Calculate the approximate efficiency of the *IC* series regulator in Problem 17-30. A switching regulator with similar supply and load conditions uses a *FET* with $r_{DS(on)}$ = 10 Ω, and a switching diode with V_F = 0.7 V. Calculate the approximate efficiency of the switching regulator.

Section 17-7

17-34 Determine minimum filter component values for a step-down switching regulator to have: f = 28 kHz, V_i = 30 V, V_o = 15 V, I_o = 300 mA, and V_r = 250 mV. Assume that $V_{(sat)}$ = V_F = 1 V.

17-35 A step-up switching regulator that is to have: f = 28 kHz, V_i = 12 V, V_o = 30 V, I_o = 150 mA, and V_r = 250 mV. Determine suitable minimum filter component values. Assume that $V_{(sat)} = V_F$ = 1 V.

17-36 Determine minimum filter component values for an inverting switching regulator to have: f = 28 kHz, V_i = 30 V, V_o = -12 V, I_o = 300 mA, and V_r = 250 mV. Assume that $V_{(sat)}$ = V_F = 1 V.

Section 17-8

17-37 The step-down switching regulator in Problem 17-34 is to use an *MC34063 IC* controller. Determine suitable values for the additional components.

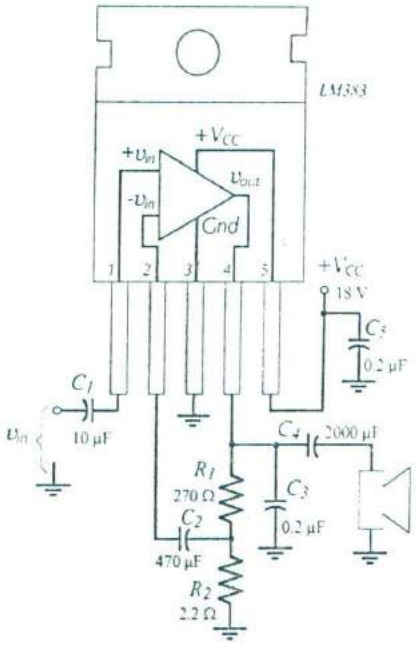
17-38 Calculate values for the additional components for the step-up switching regulator in Problem 17-35 when an *MC34063 IC* controller is used.

17-39 Calculate the additional component values for the inverting switching regulator in Problem 17-36 to use an *MC34063 IC* controller.

Practise Problem Answers

17-1.1 25.7 mV, 14.3 mV, 0.21%, 0.12%
17-1.2 1.5 kΩ, 470 Ω, (3.9 kΩ + 390 Ω), 10 kΩ, *1N758* (25 V, 70 mA, 700 mW)
17-2.1 2.2 kΩ, 5.6 kΩ, 2 kΩ
17-2.2 5.6 kΩ, 270 Ω, 1.8 kΩ, 8.2 kΩ, 22 kΩ, (18 V, 160 mA, 1.28 W)
17-2.3 *1N749*, 3.3 kΩ, 1.5 kΩ
17-3.1 1.25 Ω, (25 V, 400 mA, 10 W)
17-3.2 3.3 Ω, 820 Ω, 15 kΩ
17-4.1 470 Ω, 15 kΩ, 4.7 kΩ, 8.2 kΩ, 2 kΩ, *1N758*
17-4.2 2.5 Ω, 220 Ω, (12 kΩ + 1.8 kΩ), 2.2 kΩ
17-5.1 10 kΩ, 6.8 kΩ, 2.5 Ω, 23 V, (200 mA, 23 V, 4.6 W)
17-5.2 270 Ω, 1.5 kΩ, 12 V, 0.45 W
17-6.1 71%, 93%
17-7.1 60 μH, 47 μF
17-7.2 30 μH, 60 μF
17-8.1 1.2 kΩ, (3.3 kΩ + 470 Ω), 0.165 Ω, 360 pF
17-8.2 1.2 kΩ, (6.8 kΩ + 1 kΩ), 0.18 Ω, 560 pF

Chapter 18
Audio Power Amplifiers



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Objectives

You will be able to:

1. *Sketch and explain Class-A, Class-B, and Class-AB transformer-coupled power amplifier circuits.*
2. *Design and analyze transformer-coupled power amplifiers, and draw the circuit dc and ac load lines.*
3. *Sketch and explain the basic circuits of Class-AB capacitor-coupled and direct-coupled power amplifiers.*
4. *Show how capacitor-coupled and direct-coupled power amplifiers should be modified for: high load currents, output current limiting, the use of overall negative feedback.*
5. *Explain: complementary and quasi-complementary emitter followers, V_{BE} multiplier, and supply decoupling.*
6. *Draw and explain complete circuits for direct- and capacitor-coupled power amplifiers using: BJT driver stages, op-amp drivers, BJT output stages, and MOSFET output stages.*
7. *Design and analyze the types of circuit listed in item 6 above.*
8. *Draw and explain complementary common-source power amplifiers, and design and analyze such circuits.*
9. *Explain the applications of various integrated circuit power amplifiers.*

Introduction

A *power amplifier*, or *large-signal amplifier*, develops relatively large output voltages across low impedance loads. Audio amplifiers are large-signal amplifiers that supply *ac* output power to speakers. Power amplifiers may be categorized as *Class-A* circuits in which the output transistor is biased to the center of its load line, or as *Class-B* or *Class-AB* amplifiers in which two output transistors are biased at or close to cutoff. The amplifier load may be transformer-coupled, capacitor-coupled, or direct-coupled. Direct coupling usually gives the best performance, but plus-and-minus supply voltages are required. The output stage of the amplifier may use power *BJTs* or power *MOSFETs*. *IC* operational amplifiers may also be used in power amplifiers, and complete power amplifiers are available as integrated circuits.

18-1 Transformer-Coupled Class-A Amplifier

Class A Circuit

Instead of capacitor coupling, a transformer may be used to *ac* couple amplifier stages while providing *dc* isolation between stages. The resistance of the transformer windings is normally very small, so that there is no effect on the transistor bias conditions.

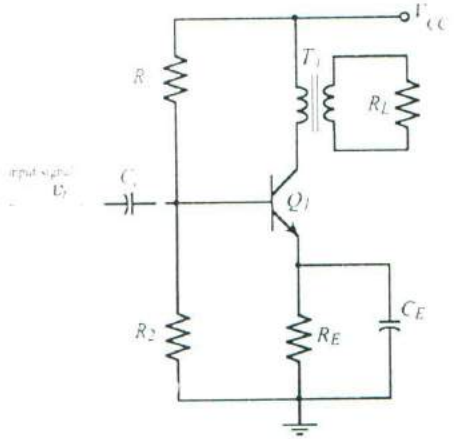


Figure 18-1
Transformer-coupled Class-A circuit using emitter current bias. Q_1 is biased to produce maximum equal positive and negative V_{CE} changes. The transistor ac load depends on R_L and the square of the transformer turn ratio.

Figure 18-1 shows a load resistance (R_L) transformer-coupled to a transistor collector. The low resistance of the transformer primary winding allows any desired level of (*dc*) collector current to flow, while the transformer core couples all variations in I_C to R_L via the secondary winding. This circuit is an emitter current bias circuit with voltage divider resistors R_1 and R_2 determining the transistor base voltage (V_B), and resistor R_E setting the emitter current level.

The circuit in Fig. 18-1 is referred to as a *class-A amplifier*, which is defined as one that has the *Q*-point (bias point) approximately at the center of the *ac* load line. This enables the circuit to produce maximum equal positive and negative changes in V_{CE}.

DC and AC Loads

The total *dc* load for transistor Q_1 in the circuit in Fig. 18-1 is the sum of the emitter resistor (R_E) and the transformer primary winding resistance (R_{PY}).

$$R_{L(dc)} = R_E + R_{PY} \qquad \textbf{(18-1)}$$

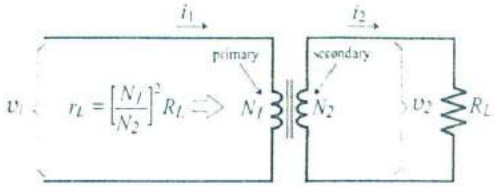


Figure 18-2
The load (R_L) at the secondary terminals of a transformer is reflected into the primary as $R_L(N_1/N_2)^2$.

Consider the transformer illustrated in Fig. 18-2. N_1 is the number of turns on the primary winding, and N_2 is the number of secondary turns. The primary *ac* voltage and current are v_1 and i_1, and the secondary quantities are v_2 and i_2. The (secondary) load resistance can be calculated as,

$$R_L = \frac{v_2}{i_2}$$

The *ac* load resistance measured at the transformer primary terminals (r_L) is calculated as,

$$r_L = \frac{v_1}{i_1}$$

From basic transformer theory,

$$\frac{v_1}{v_2} = \frac{N_1}{N_2} \quad \text{and} \quad \frac{i_1}{i_2} = \frac{N_2}{N_1}$$

These equations give,

$$v_1 = \frac{N_1}{N_2} v_2 \quad \text{and} \quad i_1 = \frac{N_2}{N_1} i_2$$

Substituting for v_1 and i_1 in the equation for r_L,

$$r_L = \left[\frac{N_1}{N_2}\right]^2 R_L \qquad \textbf{(18-2)}$$

The load resistance calculated in this way is termed the *reflected load*, or the *referred load;* meaning that R_L is reflected or referred from the transformer secondary to the primary as r_L. The total *ac* load at the transistor collector is the sum of the referred load and the transformer primary winding resistance,

$$r_{L(ac)} = r_L + R_{PY} \qquad \textbf{(18-3)}$$

Example 18-1

Draw the *dc* and *ac* load lines for the circuit in Fig. 18-3 on the transistor common emitter characteristics in Fig. 18-4. The transformer has $R_{(T)} = 40\ \Omega$, $N_1 = 74$, and $N_2 = 14$.

Solution

Q point:

$$V_B = V_{CC} \times \frac{R_2}{R_1 + R_2} = 13\ \text{V} \times \frac{3.7\ \text{k}\Omega}{4.7\ \text{k}\Omega + 3.7\ \text{k}\Omega}$$

$$\approx 5.7\ \text{V}$$

$$I_C \approx I_E = \frac{V_B - V_{BE}}{R_E} = \frac{5.7\ \text{V} - 0.7\ \text{V}}{1\ \text{k}\Omega}$$

$$\approx 5\ \text{mA}$$

$$V_{CE} = V_{CC} - I_C (R_{(T)} + R_E) = 13\ \text{V} - 5\ \text{mA}\ (40\ \Omega + 1\ \text{k}\Omega)$$

$$\approx 8\ \text{V}$$

Plot the Q-point on the characteristics at $I_C = 5$ mA and $V_{CE} = 8$ V.

dc load line:

$$V_{CE} = V_{CC} - I_C (R_{(T)} + R_E)$$

When $I_C = 0$, $\quad V_{CE} = V_{CC} = 13\ \text{V}$

Plot point *A* on the characteristics at $I_C = 0$ and $V_{CE} = 13$ V.

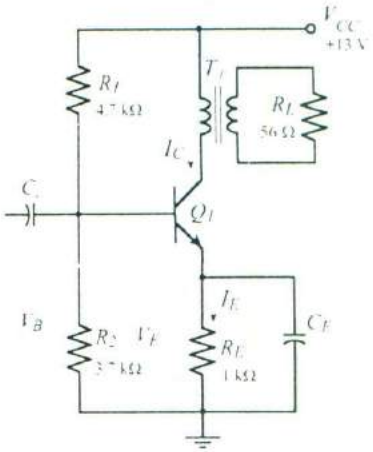


Figure 18-3
Transformer-coupled Class-A amplifier for Example 18-1.

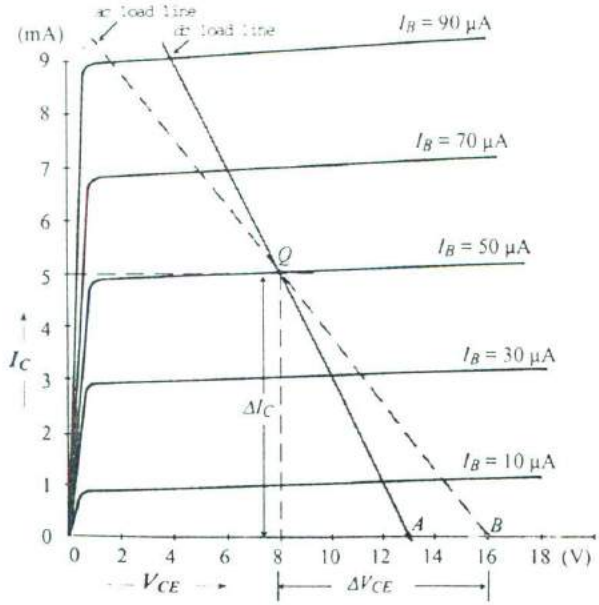


Figure 18-4
The dc load line for a transformer-coupled amplifier is drawn through the Q-point at a slope of $-1/R_{(dc)}$. The ac load line is drawn through the Q-point at a slope of $-1/r_{(ac)}$.

Draw the *dc* load through point *A* and point *Q*.

ac load line:

Eq. 18-2, $$r_l = \left[\frac{N_1}{N_2}\right]^2 R_l = \left[\frac{74}{14}\right]^2 \times 56\ \Omega$$
$$= 1565\ \Omega$$

Eq. 18-3, $$r_{l(ac)} = r_l + R_{PS} = 1565\ \Omega + 40\ \Omega$$
$$\approx 1.6\ \text{k}\Omega$$

When I_C changes by $\Delta I_C = 5$ mA,

$$\Delta V_{CI} = \Delta I_C \times r_{l(ac)} = 5\ \text{mA} \times 1.6\ \text{k}\Omega$$
$$= 8\ \text{V}$$

Measure ΔI_C and ΔV_{CI} from the *Q*-point on the characteristics to give point *B* at $V_{CI} = 16$ V and $I_C = 0$. Draw the *ac* load line through points *Q* and *B*.

Collector Voltage Swing

The *ac* load line drawn in Ex. 18-1 is reproduced in Fig. 18-5 to show the effect of an input signal. When the input causes I_B to increase from 50 μA (at I_{BQ}) to 90 μA, the current and voltage become $I_C \approx 9$ mA and $V_{CE} \approx 1.6$ V. (point *C* on the *ac* load line). The changes are: $\Delta I_C = +4$ mA, and $\Delta V_{CE} = -6.4$ V. When the input causes I_B to decrease (from I_{BQ}) to 10 μA, I_C changes from 5 mA to 1 mA, and the V_{CE} changes from 8 V to 14.4 V. (point *D*). The current and voltages changes are now: $\Delta I_C = -4$ mA and $\Delta V_{CE} = +6.4$ V.

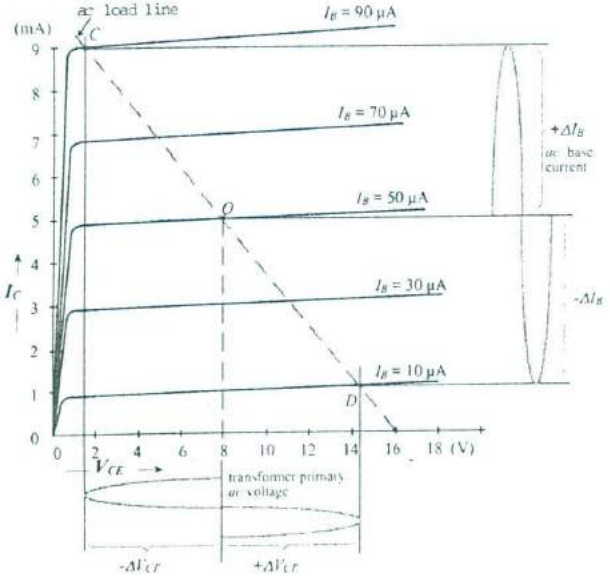


Figure 18-5
A transformer-coupled Class-A amplifier has its Q-point at the center of the ac load line. The ac voltage applied to the transformer primary is $\pm\Delta V_{CT}$, which is produced by $\pm\Delta I_B$.

It is seen that an I_B change of ±40 μA produces a ±4 mA I_C change and a ±6.4 V change in V_{CE}. The V_{CE} variation appears at the primary winding of transformer T_1 (Fig. 18-3), and the I_C variation flows in the primary winding.

Note that, although V_{CC} = 13 V, the transistor V_{CE} can actually go to 16 V. This is due to the inductive effect of the transformer primary winding. The transistor used in this type of circuit should have a minimum breakdown voltage approximately equal to 2 V_{CC}.

Efficiency of a Class A Amplifier

Power is delivered to an amplifier from the *dc* power supply. The amplifier converts the *dc* power into *ac* power delivered in the load, (see Fig. 18-6). Some of the input power is dissipated in the transistor or in other components. This is wasted power. The efficiency (η) of a power amplifier is a measure of how good the amplifier is at converting the *dc* input (supply) power (P_i) into *ac* output power (P_o) dissipated in the load.

$$\eta = \frac{P_o}{P_i} \times 100\% \qquad \textbf{(18-4)}$$

The *dc* supply power is,

$$P_i = V_{CC} \times I_{ave}$$

In the case of a class A amplifier, $I_{ave} = I_{CQ}$.

So, $$P_i = V_{CC} \times I_{CQ}$$

Refer again to the class A circuit in Fig. 18-6, and assume that $V_E << V_{CC}$. In this case, V_{CEQ} is approximately equal to V_{CC}, and the peak voltage developed across the transformer primary approaches $\pm V_{CC}$ if the transistor is driven to cutoff and saturation. Also, the peak current developed in the transformer windings approaches $\pm I_{CQ}$. Thus, the maximum *ac* power delivered to the transformer primary can be calculated as,

$$P_o' = V_{rms} \times I_{rms} = (V_p/\sqrt{2}) \times (I_p/\sqrt{2})$$

giving, $$\mathbf{P_o' = 0.5\ V_p I_p} \qquad \textbf{(18-5)}$$

Using the highest possible current and voltage levels, and assuming that the transformer is 100% efficient,

$$P_o = 0.5\ V_{CC} I_{CQ}$$

The maximum theoretical efficiency for a Class-*A* transformer-coupled power amplifier can now be determined as,

Eq. 18-4, $$\eta = \frac{P_o}{P_i} \times 100\% = \frac{0.5\ V_{CC} I_{CQ}}{V_{CC} I_{CQ}} \times 100\%$$

$$= 50\%$$

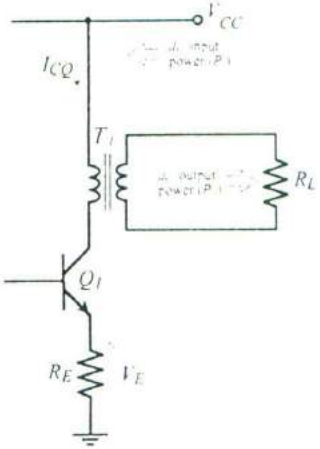


Figure 18-6
A power amplifier converts dc input (supply) power into ac output power.

In a practical Class-*A* transformer-coupled power amplifier circuit, 50% efficiency is never approached. Any practical calculation of power amplifier efficiency must take the output transformer efficiency (η_t) into account.

$$\eta_t = \frac{P_o}{P_o'} \times 100\% \qquad \textbf{(18-6)}$$

A typical transformer efficiency might be 80%. There is also power dissipation in the transistor emitter resistor and in the bias circuit. The practical maximum efficiency for a Class-*A* power amplifier is usually around 25%. This means, for example, that 4 W of *dc* supply power must be provided to deliver 1 W of *ac* output power to the load.

Example 18-2

Calculate the maximum efficiency of the Class-A amplifier circuit in Ex. 18-1, (reproduced in Fig. 18-7). Assuming that the transformer has an 80% efficiency.

Solution

$$P_i = V_{CC} \times I_{CQ} = 13\text{ V} \times 5\text{ mA}$$
$$= 65\text{ mW}$$

$$V_p \approx V_{CEQ} = 8\text{ V}$$

$$I_p \approx I_{CQ} = 5\text{ mA}$$

Eq. 18-5, $$P_o' = 0.5\, V_p I_p = 0.5 \times 8\text{ V} \times 5\text{ mA}$$
$$= 20\text{ mW}$$

Eq. 18-6, $$P_o = \eta_t P_o' = 0.8 \times 20\text{ mW}$$
$$= 16\text{ mW}$$

Eq. 18-4, $$\eta = \frac{P_o}{P_i} \times 100\% = \frac{16\text{ mW}}{65\text{ mW}} \times 100\%$$
$$= 24.6\%$$

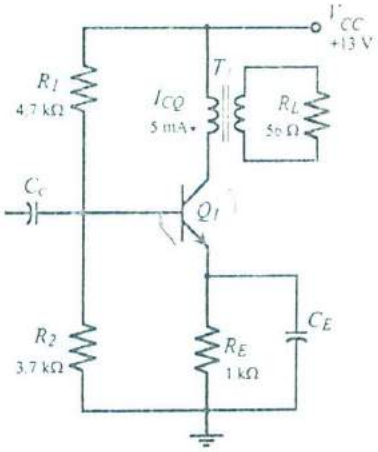


Figure 18-7
Class-A power amplifier for Example 18-2.

Practise Problems

18-1.1 The circuit in Ex. 18-1 has the quantities changed to: $V_{CC} = 15$ V, $R_1 = 3.9\text{ k}\Omega$, $R_2 = 2.2\text{ k}\Omega$, $R_E = 1.5\text{ k}\Omega$, $R_{PY} = 33\,\Omega$, $R_L = 100\,\Omega$, $N_1 = 118$, $N_2 = 20$. Draw the new *dc* and ac load lines on Fig. 18-4.

18-1.2 Determine the maximum efficiency for the amplifier in Problem 18-1.1. Assume that the transformer efficiency is 75%.

18-2 Transformer-Coupled Class-B and Class-AB Amplifiers

Class B Amplifier

The inefficiency of Class-*A* amplifiers is largely due to the transistor bias conditions. In a Class-*B* amplifier, the transistors are biased to cutoff, so that there is no transistor power dissipation when there is no input signal. This gives the Class-*B* amplifier a much greater efficiency than the Class-*A* circuit.

The output stage of a Class-*B* transformer-coupled amplifier is shown in Fig. 18-8. Transformer T_2 couples load resistor R_L to the collector circuits of transistors Q_2 and Q_3. Note that the supply is connected to the center-tap of the transformer primary, and that Q_2 and Q_3 have grounded emitters. The transistor bases are grounded via resistors R_1 and R_2, so that both are biased *off*.

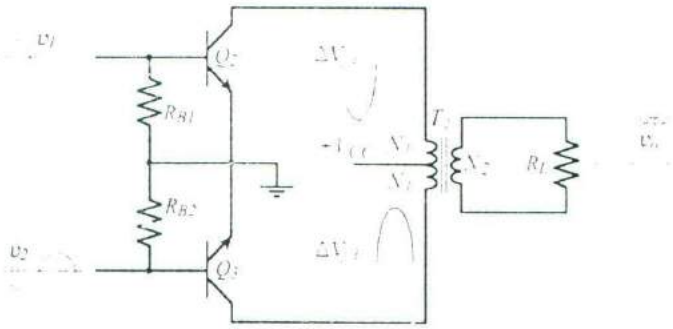


Figure 18-8
In a Class-B power amplifier, two transistors operate in push-pull. When the input signal turns Q_2 on, Q_3 is turned off, and vice versa.

The input signals applied to the transistor bases consist of two separate sine waves which are identical, except that they are in antiphase. When v_1 is going positive, v_2 is going negative, so that Q_3 is being biased further *off* as Q_2 is being biased *on*. As the collector current in Q_2 increases from zero, it produces a half sine wave of voltage across the upper half of the transformer primary, as illustrated. When the positive half-cycle of input signal to Q_2 base begins to go negative, the signal at Q_3 base is commencing to go positive. Thus, as Q_2 becomes biased *off* again, Q_3 is biased *on*, and a half-cycle of voltage waveform is generated across the lower half of the transformer primary.

The two half-cycles in the separate sections of the transformer primary produce a magnetic flux in the transformer core that flows first in one direction and then in the opposite direction. This flux links with the secondary winding and generates a complete sine wave output which is passed to the load.

In the Class-*B* circuit, the two output transistors are said to be operating in *push-pull*. The push-pull action is best illustrated by drawing the *ac* load line on the *composite characteristics* for Q_2 and Q_3. The composite characteristics are created by drawing the Q_2

characteristics in the normal way, and presenting the Q_3 characteristics upside down. This is illustrated in Fig. 18-9.

Example 18-3

Draw the ac load lines for the circuit in Fig. 18-8 on the transistor composite characteristics in Fig. 18-9. The transformer has $R_{PY} = 40\ \Omega$, $N_1 = 74$, and $N_2 = 14$, and the supply voltage is $V_{CC} = 16$ V.

Solution

Q-point : $V_B = 0$ V and $I_C = 0$ mA

$$V_{CE} = V_{CC} - I_C(R_{PY} + R_E) = 16\text{ V} - 0$$
$$= 16\text{ V}$$

Plot the Q-point on the characteristics at $I_C = 0$ mA and $V_{CE} = 16$ V.

ac load line:

Eq. 18-2, $$r_L = \left[\frac{N_1}{N_2}\right]^2 R_L = \left[\frac{74}{14}\right]^2 \times 56\ \Omega$$
$$= 1565\ \Omega$$

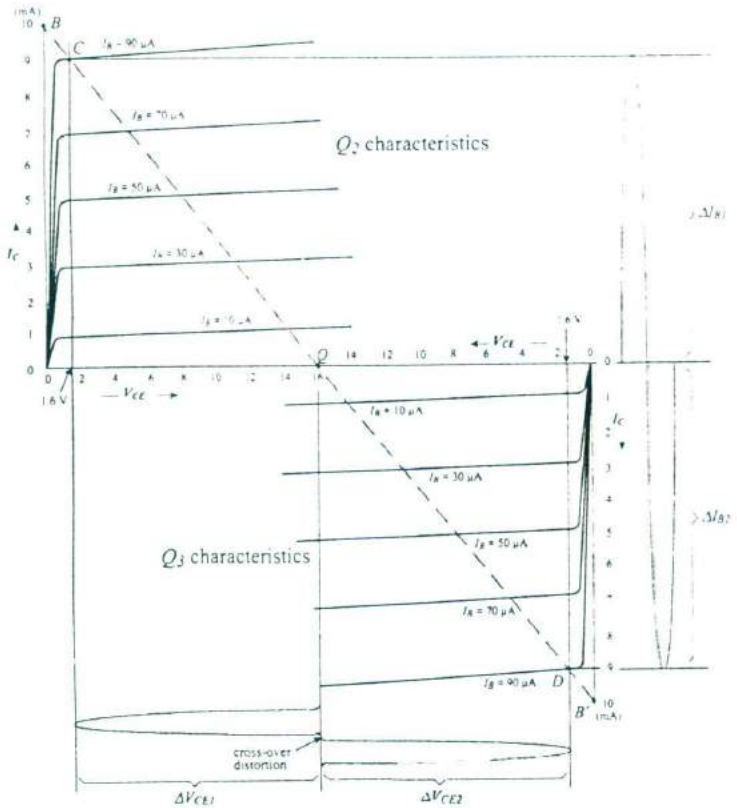


Figure 18-9
AC load line for a Class-B amplifier drawn on the BJT composite characteristics. Also, showing the effect of I_B changes on V_{CE}.

Eq. 18-3, $r_{(ac)} = r_l + R_{p'} = 1565\ \Omega + 40\ \Omega$
$\approx 1.6\ k\Omega$

When I_C changes by $\Delta I_C = 10$ mA,

$$V_{CE} = \Delta I_C \times r_{(ac)} = 10\ mA \times 1.6\ k\Omega$$
$$= 16\ V$$

Measure ΔI_C and V_{CE} from the Q-point to give points B and B' at $V_{CE} = 16$ V and $I_C = 0$. Draw the ac load line through points Q, B, and B'.

Now consider the effect of a signal applied to the bases of Q_2 and Q_3 in the circuit in Fig. 18-8. When I_{B1} is increased from zero to 90 μA, Q_3 remains *off* and V_{CE1} falls to 1.6 V, (point C on the composite characteristics in Fig. 18-9). At this point the voltage across the upper half of the transformer primary in is,

$$V_{pu} = V_{CC} - V_{CE} = 16\ V - 1.6\ V$$
$$= 14.4\ V$$

When I_{B2} is increased from 0 to 90 μA, Q_2 is *off*, and the Q_3 current and voltage conditions move to point D on the ac load line. This produces 14.4 V across the lower half of the transformer primary. Thus, a full sine wave is developed at the transformer output. When no signal is present, both transistors remain *off* and dissipate zero power. Power is dissipated only while each device is conducting. The wasted power is considerably less with the Class-B amplifier than with a Class-A circuit.

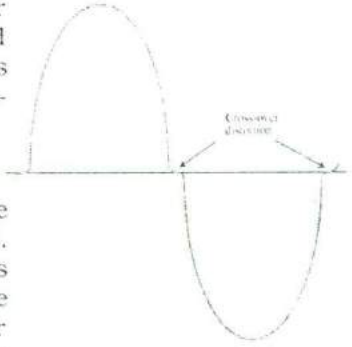


Figure 18-10
Cross-over distortion occurs in Class-B amplifiers because the transistors are biased off.

Cross-Over Distortion

The waveform delivered to the transformer primary and the resultant output are not perfectly sinusoidal in the Class-B circuit. *Cross-over distortion* is produced in the output waveform, as illustrated in Fig. 18-9 and 18-10, due to the fact that the transistors do not begin to turn on until the input base-emitter voltage is about 0.5 V for a silicon device, or 0.15 V for a germanium transistor. To eliminate this effect, the transistors are partially biased *on* instead of being biased *off*. With this modification, the Class-B amplifier becomes a *Class-AB amplifier*.

Class AB Amplifier

Figure 18-11 shows a Class-AB transformer-coupled output stage with a Class-A transformer-coupled *driver stage*. The output transformer (T_2) has a center-tapped primary winding, with each half of the winding constituting a load for one of the output transistors (Q_2 and Q_3). Resistors R_4 and R_5 bias Q_2 and Q_3 partially *on*, and resistors R_6 and R_7 limit the emitter (and collector) currents to the desired bias levels. Transformer T_1 together with transistor Q_2 and the associated components comprise a Class-A stage. The secondary of T_1 is center-tapped to provide the necessary antiphase signals to Q_2 and Q_3.

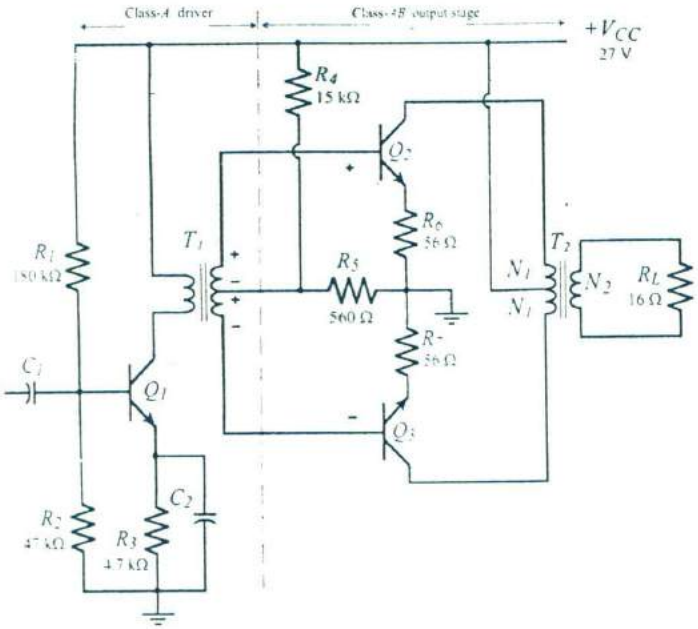


Figure 18-11
Class-AB transformer-coupled output stage with a Class-A driver stage. Transistors Q_2 and Q_3 are biased to a low I_C level.

When the instantaneous polarity of T_1 output is positive at the top, Q_2 base voltage is positive and Q_3 base voltage is negative, as illustrated. At this time Q_2 is *on* and Q_3 is *off*. When the polarity reverses at T_1 output, the base of Q_3 becomes positive and that of Q_2 becomes negative. The output stage functions exactly as for a Class-*B* circuit, except that each device commences to conduct just before the signal to its base becomes positive. This eliminates the transistor turn-on delay that creates crossover distortion in a Class-*B* amplifier.

The Class-*A* portion of the circuit in Fig. 18-11 is referred to as a *driver stage*, simply because it provides the input signals to drive the Class-*AB* output stage. The input power handled by the driver stage is very much smaller than the circuit output power, so that the inefficiency of the Class-*A* stage is unimportant.

Efficiency of Class-B and Class-AB Amplifiers

For a Class-*B* amplifier, the *dc* supply power (see Fig. 18-12) is calculated as,

$$P_{i(dc)} = V_{CC} \times I_{ave}$$

or,
$$\mathbf{P_{i(dc)} = V_{CC} \times 0.636\ I_p} \qquad \textbf{(18-7)}$$

The *ac* power input to the transformer primary is given by Eq. 18-5,

$$P_o' = 0.5\ V_p I_p \approx 0.5\ V_{CC} I_p$$

Assuming a 100% efficiency for the output transformer,

$$P_o = P_o' \approx 0.5\ V_{CC} I_p$$

So, the maximum theoretical efficiency for a Class-*B* transformer-coupled power amplifier is,

Eq. 18-4.
$$\eta = \frac{P_o}{P_i} \times 100\% = \frac{0.5\, V_{CC}\, I_p}{0.636\, V_{CC}\, I_p} \times 100\%$$
$$= 78.6\%$$

Once again, the efficiency of a practical amplifier is lower than the theoretical efficiency. Some power is wasted in the transistors and emitter resistors, and the transformer is never 100% efficient.

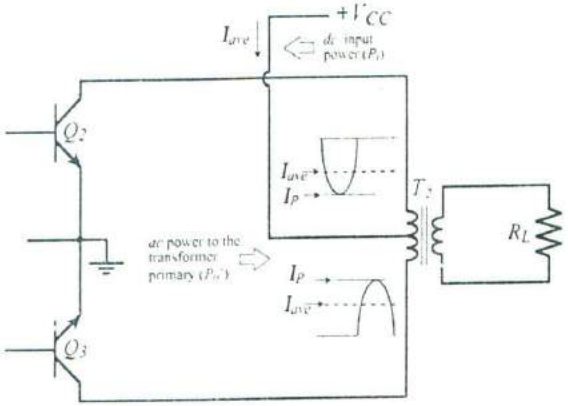


Figure 18-12
The dc input power to a Class-B amplifier is $P_i = (V_{CC} \times I_{ave})$, and the ac power to the transformer primary is $P_o' = (0.5\, V_{CC}\, I_p)$.

The efficiency of a Class-*AB* power amplifier is typically a little less than that of a Class-*B* circuit, because of the additional small amount of power wasted in keeping the output transistors biased in a low-current *on* state. Class-*B* and Class-*AB* power amplifiers are employed more often than Class-*A* circuits, because of their greater efficiency.

Example 18-4

Calculate the power delivered to the load in the Class-*AB* amplifier Fig. 18-13, (reproduced from Fig. 18-11). Assume that T_2 has a 79% efficiency, and that there is a 0.5 V drop across Q_2 and across Q_3 at peak output voltage. Also, assume that $N_1 = 60$, $N_2 = 10$, and that the primary winding resistance is small enough to neglect.

Solution

Referred load:

Eq. 18-2,
$$r_l = \left[\frac{N_1}{N_2}\right]^2 \times R_L = \left[\frac{60}{10}\right]^2 \times 16\ \Omega$$
$$= 576\ \Omega$$

Total ac load in series with each of Q_2 and Q_3:

$$R_L' = r_l + R_6 + R_{PY} = 576\ \Omega + 56\ \Omega + 0$$
$$= 632\ \Omega$$

Peak primary current:

$$I_p = \frac{V_{CC} - V_{CE}}{R_L'} = \frac{27\text{ V} - 0.5\text{ V}}{632\ \Omega}$$
$$= 41.9\text{ mA}$$

Peak primary voltage:

$$V_p = V_{CC} - V_{CE} - (I_p R_6)$$
$$= 27\text{ V} - 0.5\text{ V} - (41.9\text{ mA} \times 56\ \Omega)$$
$$= 24.15\text{ V}$$

Power delivered to primary:

Eq. 18-5, $P_o' = 0.5\, V_p I_p$
$= 0.5 \times 24.15\text{ V} \times 41.9\text{ mA}$
$= 506\text{ mW}$

Power delivered to the load:

P_o = (P_o' × transformer efficiency)
$= 506\text{ mW} \times 0.79$
$= 400\text{ mW}$

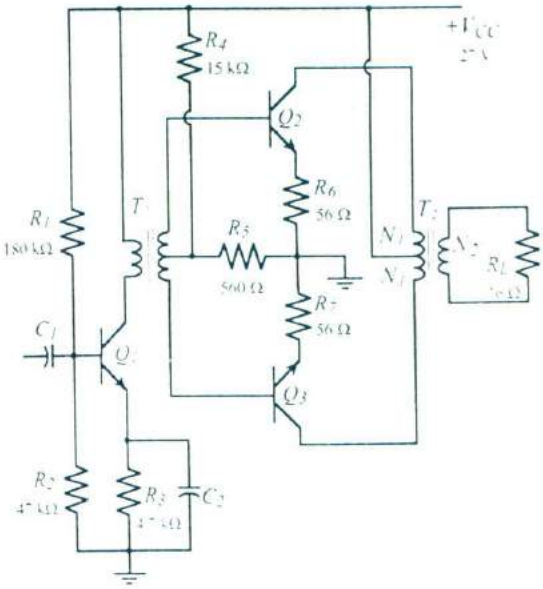


Figure 18-13
Class-AB transformer-coupled amplifier for Example 18-4

Practise Problems

18-2.1 Calculate the bias currents in the circuit in Fig. 18-13, and using the results from Ex. 18-4 estimate the overall efficiency of the amplifier.

18-2.2 Draw the *dc* and *ac* load lines for the output stage in the circuit in Fig. 18-13 on blank composite characteristics.

18-3 Transformer-Coupled Amplifier Design

Design of a transformer-coupled amplifier commences with the load resistance and output power specification. A signal voltage amplitude may also be stated, as well as the upper and lower cutoff frequencies for the amplifier. If a supply voltage is given, then the design must determine a specification for the transformer. Where an available transformer is to be employed, the supply voltage is calculated to suit the transformer. The maximum levels of V_{CE}, I_C, and P_D must be calculated for each transistor.

The power delivered to the transformer primary is determined from the Eq. 18-6.

$$P_o' = \frac{P_o}{\eta_t}$$

The power delivered to the primary can also be expressed as,

$$P_o' = \frac{(V_{rms})^2}{r_L}$$

where V_{rms} is the *rms* primary voltage, and r_L is the *ac* resistance offered by the transformer primary (the referred resistance). Using peak voltages, the equation becomes,

$$P_o' = \frac{(V_p/\sqrt{2})^2}{r_L} = \frac{V_p^2}{2\,r_L}$$

This gives the equation for r_L:

$$r_L = \frac{V_p^2}{2\,P_o'} \qquad \textbf{(18-8)}$$

Using Eq. 18-2, r_L can be calculated in terms of the load resistance and the transformer turn ratio:

$$r_L = \left[\frac{N_1}{N_2}\right]^2 R_L$$

The resistance seen when "looking into" the whole winding of a transformer with a center-tapped primary (see Fig. 18-14) is,

$$r_L' = \left[\frac{2\,N_1}{N_2}\right]^2 R_L = 4\left[\frac{N_1}{N_2}\right]^2 R_L$$

or,

$$r_L' = 4\,r_L \qquad \textbf{(18-9)}$$

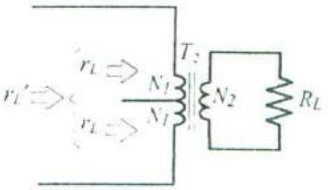


Figure 18-14
The input resistance at each half of the center-tapped primary winding of an output transformer is r_L, and the input resistance to the whole primary is $r_L' = 4\,r_L$.

The transformer can now be specified in terms of the output power (P_o), the load resistance (R_L), and the referred resistance (r_L').

Referring to Fig. 18-15, note that when Q_2 is *off* and Q_3 is *on* a voltage with a peak value of approximately $+V_{CC}$ is induced in the half of the transformer primary connected to Q_2. The induced voltage occurs because the other half of the primary has $+V_{CC}$ applied to it via Q_3, and because both windings are on the same magnetic core. The induced voltage is superimposed upon the supply, so that the voltage that appears at the collector of Q_2 is,

$$V_{CE(max)} = 2\,V_{CC} \qquad \textbf{(18-10)}$$

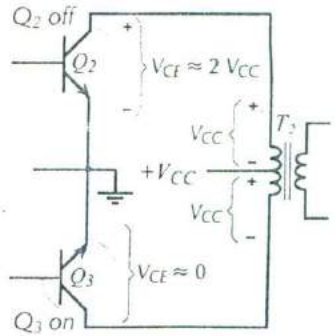


Figure 18-15
With Q_1 off and Q_2 on, the voltage across Q_1 collector-emitter is approximately $2\,V_{CC}$.

To determine the peak transistor current, the equation for power delivered to the transformer primary is rewritten. From Eq. 18-5,

$$I_p = \frac{2\,P_o'}{V_p} \qquad \textbf{(18-11)}$$

The power dissipated in the two output transistors is the difference between the *dc* supply power to the amplifier and the *ac* power delivered to the transformer primary:

$$2\,P_T = P_{i(dc)} - P_o'$$

Each transistor is *on* for half of each cycle of the input signal, so the power dissipated in each transistor is half of 2 P_T.

$$P_T = 0.5\,(P_{i(dc)} - P_o') \qquad \textbf{(18-12)}$$

The transistors are specified in terms of the device power dissipation (P_T), the peak current (I_p), and the maximum collector-emitter voltage ($V_{CE(max)}$). The transistors must also be operated below the maximum power dissipation curve. (see Section 8-7).

Example 18-5

The Class-B circuit in Fig. 18-16 is to dissipate 4 W in the 16 Ω load. Specify the output transformer and transistors. Assume an 80% transformer efficiency.

Solution

Eq. 18-6. $$P_o' = \frac{P_o}{\eta_t} = \frac{4\text{ W}}{0.8}$$
$$= 5\text{ W}$$

$$V_p \approx V_{CC} = 30\text{ V}$$

Eq. 18-8. $$r_L' = \frac{V_p^2}{2\,P_o'} = \frac{(30\text{ V})^2}{2 \times 5\text{ W}}$$
$$= 90\ \Omega$$

$$r_L' = 4\,r_L = 4 \times 90\ \Omega$$
$$= 360\ \Omega$$

Transformer specification:

$$P_o = 4\text{ W},\ R_L = 16\ \Omega,\ r_L' = 360\ \Omega \text{ center-tapped}$$

Eq. 18-10. $$V_{CE(max)} = 2\,V_{CC} = 2 \times 30\text{ V}$$
$$= 60\text{ V}$$

Eq. 18-11. $$I_p = \frac{2\,P_o'}{V_p} = \frac{2 \times 5\text{ W}}{30\text{ V}}$$
$$= 333\text{ mA}$$

Eq. 18-7. $$P_{i(dc)} = V_{CC} \times 0.636\,I_p = 30\text{ V} \times 0.636 \times 333\text{ mA}$$
$$= 6.35\text{ W}$$

Eq. 18-12. $$P_T = 0.5\,(P_{i(dc)} - P_o') = 0.5\,(6.35\text{ W} - 5\text{ W})$$
$$= 0.68\text{ W}$$

Transistor specification:

$$P_T = 0.68\text{ W},\ V_{CE(max)} = 60\text{ V},\ I_p = 333\text{ mA}$$

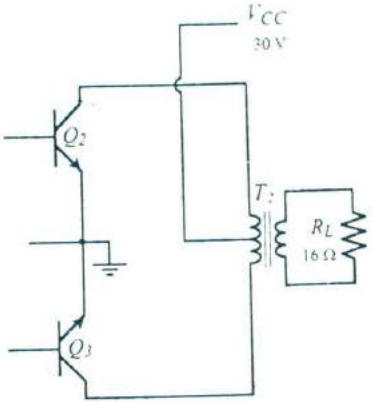


Figure 18-16
Class-B power amplifier output stage for Ex. 18-5.

Poor frequency response is one disadvantage of transformer-coupled amplifiers, both at the low and high ends of the audio frequency range. This can be improved by the use of overall negative feedback. However, substantial improvement in frequency response can be achieved by eliminating transformers from the circuit. The alternatives are capacitor-coupling and direct-coupling of the amplifier load.

Practise Problems

18-3.1 A Class-*A* transformer-coupled amplifier is to produce a peak current of 15 mA in a 200 Ω load. The available transformer has R_L = 200 Ω, r_l = 320 Ω, and efficiency = 90%. Determine a suitable supply voltage and specify the transistor.

18-3.2 A Class-*B* transformer-coupled amplifier with V_{CC} = 25 V is to supply 6 W to a 12 Ω load. Assuming a 75% transformer efficiency, specify the transistors and transformer.

18-4 Capacitor-Coupled and Direct-Coupled Output Stages

Complementary Emitter Follower

Two *BJTs* connected to function as emitter followers are shown in Fig. 18-17. Although one is *npn* and the other is *pnp*, the devices are selected to have similar parameters, so they are *complementary transistors*. The circuit is termed a *complementary emitter follower*.

A single-transistor emitter follower is essentially a small-signal circuit, because large signals can reverse bias the transistor base-emitter junction when the input polarity is opposite to the transistor V_{BE} polarity. An *npn* emitter follower might not correctly reproduce the negative-going portion of a large signal, while a *pnp* emitter follower might not reproduce the positive-going portion. Complementary emitter followers have similar signals applied simultaneously to both device bases, as illustrated. Transistor Q_1 conducts during the positive half-cycle of the signal, and it *pulls* the output voltage up to follow the input. During this time, Q_2 base-emitter junction is reverse biased. For the duration of the negative half-cycle of the input, Q_1 base-emitter junction is reversed and Q_2 conducts, pulling the output down to follow the input. Thus, the complementary emitter follower is a large-signal circuit with the low output impedance typical of emitter followers.

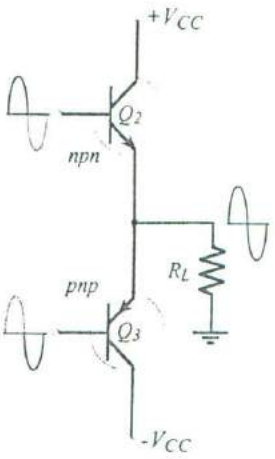


Figure 18-17
A complementary emitter follower uses an npn transistor and a pnp transistor that have similar characteristics.

Capacitor-Coupled Class-AB Output Stage

The basic circuit of a Class-*AB* amplifier using a complementary emitter follower output stage and a capacitor-coupled load is shown in Fig. 18-18. The circuit is termed a *complementary symmetry amplifier*. Transistor Q_1 and resistors R_1, R_2, R_C, and R_{E1} comprise a common emitter amplifier stage that produces all of the circuit voltage gain. The output of Q_1 is developed across R_C and

applied to the bases of Q_2 and Q_3. Capacitor C_o *ac* couples R_L, and *dc* isolates R_L to keep it from affecting the circuit bias conditions.

The total voltage drop (V_B) across diodes D_1 and D_2 and resistor R_B forward biases the base-emitter junctions of Q_2 and Q_3 to avoid cross-over distortion. Emitter resistors R_{E2} and R_{E3} help limit the quiescent current through Q_2 and Q_3. Adjustment of the bias voltage (V_B) is provided by variable resistor R_B. The diodes have voltage drops (V_D) that approximately match the output transistor V_{BE} levels. Also, V_D does not change significantly when the diode current changes, so, the diodes behave like bypassed resistors. The diodes and output transistors can be *thermally-coupled* by mounting D_1 and Q_2 on a single heat sink, and D_2 and Q_3 on a single heat sink. In this case, V_D follows the V_{BE} level changes with temperature, thus stabilizing the transistor bias conditions over a wide temperature range. The junction of R_{E2} and R_{E3} must be biased to $V_{CC}/2$, so that the output voltage to C_o can swing by equal amounts in positive- and negative-going directions.

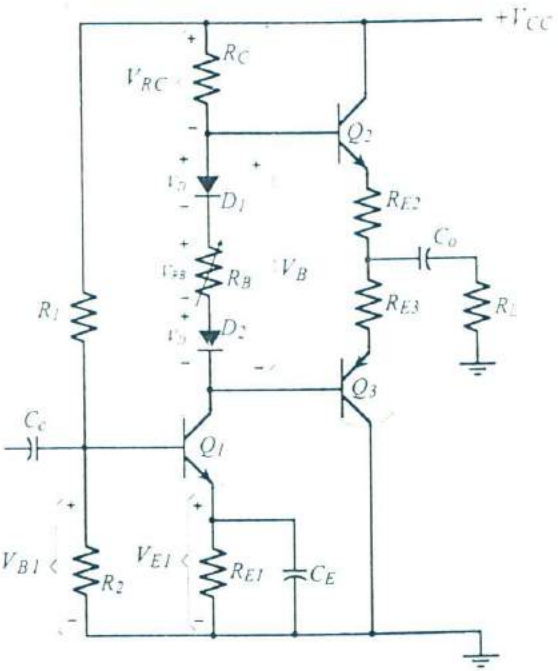


Figure 18-18
A Class-AB capaci power amplifier th complementary emitt as the output stage is complementary amplifier.

Class-AB Capacitor-Coupled Amplifier Design

Design of the type of circuit shown in Fig. 18-18 is largely a matter of selecting appropriate resistor voltage drops and current levels, and then applying Ohm's law to calculate the resistor values. The peak output voltage (V_P) and peak output current (I_P) can be determined from Eqs. 18-8 and 18-11, respectively. Those equations were developed for the power delivered to a transformer primary, but they apply equally to power delivered to any load resistor.

The voltage drops across R_{E2} and R_{E3} when the peak output current is flowing are typically selected as 5% to 10% of the peak

output voltage. This is illustrated in Fig. 18-19(a) and (b) where the output capacitor is represented as an *ac* short-circuit. So,

$$R_{E2} = R_{E3} \approx 0.05\ R_L \text{ to } 0.1\ R_L \qquad \textbf{(18-13)}$$

It should be remembered that R_{E2} and R_{E3} are included to help stabilize the transistor quiescent currents at a level that eliminates cross-over distortion in the output waveform. For the type of amplifier circuit in Fig. 18-18, without overall negative feedback, it is best to select the emitter resistors as large as possible. Smaller emitter resistors can be used in circuits with *dc* and *ac* negative feedback, (see Sections 18-5 and 18-6).

When the output is at its negative-going peak, V_{CE1} should be 1 V minimum, to ensure that Q_1 does not go into saturation. Also, V_{E1} should typically be 3 V, (see Section 5-7). So, the minimum level of V_{C1} is typically 4 V, [Fig. 18-19(b)]. Similarly, when the output is at its positive-going peak, there must be an appropriate minimum voltage drop across resistor R_C, [Fig. 18-19(a)]. It is not acceptable to set a 1 V minimum for V_{RC}, because the current through R_C would be too small for the required peak base current to Q_2. So, it is best to select,

$$V_{RC(min)} = V_{C1(min)} = 4\ \text{V} \qquad \textbf{(18-14)}$$

The minimum current through R_C ($I_{RC(min)}$) should typically be selected 1 mA larger than the peak base current for the output transistors. R_C is calculated from $V_{RC(min)}$ and $I_{RC(min)}$.

Referring to Fig. 18-19(a), the supply required to produce the positive output peak voltage is,

$$V_+ = V_P + V_{RE2} + V_{BE2} + V_{RC(min)}$$

Also, from Fig. 18-19(b), the negative output peak requires,

$$V_- = V_P + V_{RE3} + V_{BE3} + V_{C1(min)}$$

and, $$V_+ = V_-$$

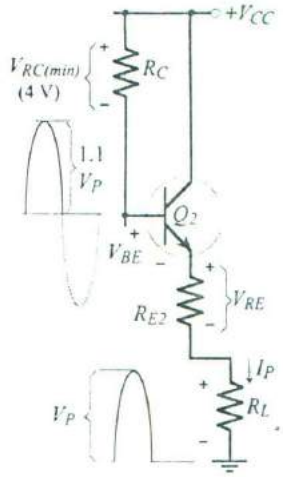
So, the total supply voltage is,

$$V_{CC} = 2(V_P + V_{RE2} + V_{BE2} + V_{RC(min)}) \qquad \textbf{(18-15)}$$

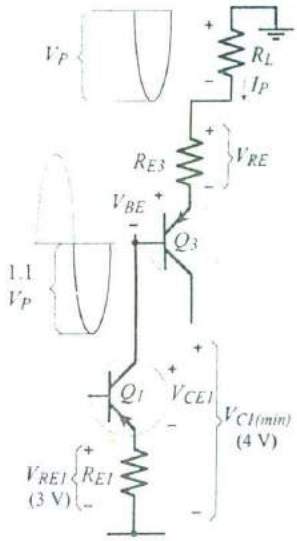
The voltage drop across the diodes and R_B should just bias Q_2 and Q_3 on for Class-*AB* operation, (see Fig. 18-20). The current through R_B is the Q_1 quiescent current (I_{CQ1}), and this is calculated from R_C and the *dc* voltage drop across R_C. $V_{RC(dc)}$ equals $V_{C1(dc)}$, and the sum of them equals (V_{CC} - V_B), (see Fig. 18-20). So,

$$V_{RC(dc)} = V_{C1(dc)} = 0.5(V_{CC} - V_B) \qquad \textbf{(18-16)}$$

The resistance of R_B is now calculated from $V_{RC(dc)}$ and I_{CQ1}. Resistors R_1, R_2, and R_{E1} are determined in the usual manner for an emitter current bias circuit.



(a) Positive output peak



(a) Negative output peak

Figure 18-19
Supply voltage determination for a Class-AB capacitor-coupled output stage.

The output transistors should be specified in terms of their maximum voltage, current, and power dissipation. The maximum V_{CE} for Q_2 and Q_3 (in Fig. 18-18) is the total supply voltage (V_{CC}). Maximum current for Q_2 and Q_3 is the peak load current plus the selected quiescent current (I_{Q23}). This normally 1.1 I_P. Transistor power dissipation is calculated by determining the *dc* power delivered to the output stage from the power supply, and then subtracting the *ac* load power. The remainder is halved to find the power dissipated in each transistor. Equation 18-12 applies: $P_T = 0.5\ (P_i - P_o)$. Recall that the transistors must be operated within the safe operating area of the characteristics. (see Section 8-7).

With a capacitor-coupled load, current is drawn from the power supply during the positive half-cycle of the output, but not during the negative half cycle. The capacitor acts as an energy reservoir to supply load current when the output is negative-going. Consequently, the supply current has a half-wave rectified waveform (see Fig. 18-21), and so,

$$I_{ave} = 0.5 \times 0.636\ 1.1\ I_p$$
$$= 0.35\ I_p$$

The *dc* supply power to the output stage is,

$$P_i = V_{CC} \times I_{ave}$$

or,

$$\boldsymbol{P_i = 0.35\ V_{CC}\ I_p} \qquad \textbf{(18-17)}$$

As always, with the exception of the capacitor selected to set the circuit low 3 dB frequency (f_l), each capacitor impedance is selected as one tenth of the impedance in series with the capacitor. Where there is no overall negative feedback, the capacitor with the lowest-value series-connected impedance is normally selected to set f_l. For the circuit shown in Fig. 18-18, the impedance looking into the emitter of Q_1 is h_{ib1}, and this is in series with C_E. If h_{ib1} is smaller than R_L, then at f_l:

$$X_{CE} \approx h_{ib1},\ X_{CC} \approx 0.1\ Z_i,\ X_{CO} \approx 0.1\ R_L$$

Most power amplifiers typically have $R_L = 8\ \Omega$ or $16\ \Omega$. So, the load-coupling capacitor normally sets the circuit low 3 dB frequency.

$$\boldsymbol{X_{CO} = R_L \text{ at } f_1} \qquad \textbf{(18-18)}$$

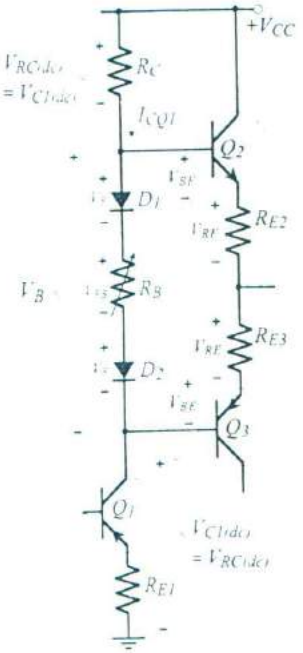


Figure 18-20
The voltage drops across D_1, D_2, and R_B bias Q_2 and Q_3 on for Class-AB operation.

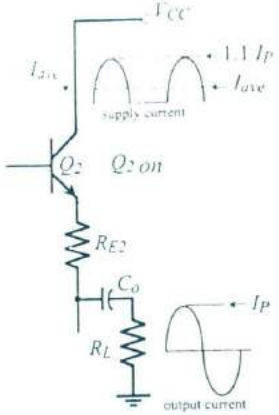


Figure 18-21
The supply current for the output stage of a capacitor-coupled Class-AB power amplifier has a half-wave rectified waveform.

Example 18-6

The Class-AB amplifier in Fig. 18-22 (reproduced from Fig. 18-18) is to deliver 1 W to a 50 Ω load. Determine the required supply voltage, and calculate resistor values for R_C, R_B, R_{f2}, and R_{f3}. Assume $h_{FE(min)} = 50$ for Q_2 and Q_3.

Solution

from Eq. 18-8, $V_p = \sqrt{(2\ R_L\ P_o)} = \sqrt{(2 \times 50\ \Omega \times 1\ W)}$
$= 10\ V$

$$I_p = \frac{V_p}{R_L} = \frac{10\text{ V}}{50\ \Omega}$$
$$= 200\text{ mA}$$

Eq. 18-13, $R_{E2} = R_{E3} = 0.1\,R_L = 0.1 \times 50\ \Omega$
$= 5\ \Omega$ (use 4.7 Ω standard value)

select, $I_{CQ2} = 0.1\,I_p = 0.1 \times 200\text{ mA}$
$= 20\text{ mA}$

$$V_B = V_{BE2} + I_{CQ2}(R_{E2} + R_{E3}) + V_{BE3}$$
$$= 0.7\text{ V} + 20\text{ mA}(4.7\ \Omega + 4.7\ \Omega) + 0.7\text{ V}$$
$$= 1.6\text{ V}$$

Eq. 18-14, $V_{C1(min)} = V_{RC(min)} = 4\text{ V}$

$$I_{B2(max)} = \frac{I_p}{h_{FE2(min)}} = \frac{200\text{ mA}}{50}$$
$$= 4\text{ mA}$$

select, $I_{RC(min)} = I_{B2(max)} + 1\text{ mA} = 4\text{ mA} + 1\text{ mA}$
$= 5\text{ mA}$

$$R_C = \frac{V_{RC(min)}}{I_{RC(min)}} = \frac{4\text{ V}}{5\text{ mA}}$$
$$= 800\ \Omega \text{ (use 680 } \Omega \text{ standard value)}$$

Eq. 18-15, $V_{CC} = 2\,(V_p + V_{RE2} + V_{BE2} + V_{RC(min)})$
$= 2\,[10\text{ V} + 1\text{ V} + 0.7\text{ V} + 4\text{ V}]$
$= 31.4\text{ V}$ (use 32 V)

Eq. 18-16, $V_{RC(dc)} = 0.5\,(V_{CC} - V_B) = 0.5\,(32\text{ V} - 1.6\text{ V})$
$= 15.2\text{ V}$

$$I_{C1(dc)} = \frac{V_{RC(dc)}}{R_{C1}} = \frac{15.2\text{ V}}{680\ \Omega}$$
$$= 22.4\text{ mA}$$

$$R_B = \frac{V_B - V_{D1} - V_{D2}}{I_{C1(dc)}} = \frac{1.6\text{ V} - 0.7\text{ V} - 0.7\text{ V}}{22.4\text{ mA}}$$
$= 8.9\ \Omega$ (use 20 Ω standard value variable resistor to allow for ± adjustment)

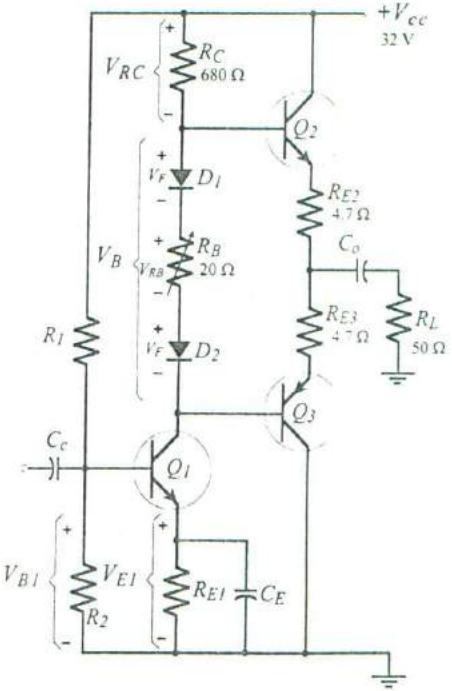


Figure 18-22
Capacitor-coupled Class-AB power amplifier for Example 18-6.

Example 18-7

Specify the output transistors for the circuit in Example 18-6.

Solution

$$V_{CE(max)} = V_{CC} = 32\ V$$

$$I_{C(max)} = 1.1\ I_p = 1.1 \times 200\ mA$$
$$= 220\ mA$$

Eq. 18-17, $$P_{i(dc)} = 0.35\ V_{CC} I_p = 0.35 \times 32\ V \times 200\ mA$$
$$= 2.24\ W$$

from Eq. 18-12, $$P_t = 0.5\ (P_{i(dc)} - P_o) = 0.5\ (2.24\ W - 1\ W)$$
$$= 0.62\ W$$

Example 18-8

Calculate capacitor values for C_i and C_o for the circuit in Example 18-6 if the lower cutoff frequency is to be 50 Hz. Assume $h_{ib1} = 20\ \Omega$.

Solution

Because $h_{ib1} < R_L$, C_i sets f_c:

$$C_i \approx \frac{1}{2\pi f_c h_{ib1}} = \frac{1}{2 \times \pi \times 50\ Hz \times 20\ \Omega}$$
$$= 159\ \mu F \text{ (use } 180\ \mu F \text{ standard value)}$$

$$C_o \approx \frac{1}{2\pi f_c\ 0.1\ R_L} = \frac{1}{2 \times \pi \times 50\ Hz \times 0.1 \times 50\ \Omega}$$
$$= 637\ \mu F \text{ (use } 680\ \mu F \text{ standard value)}$$

Direct-Coupled Class-AB Output Stage

The output capacitor in a capacitor-coupled power amplifier is a large expensive component that should be eliminated if possible. Figure 18-23 shows a Class-*AB* amplifier circuit with a direct-coupled load. In this case, the supply voltages must be positive and negative quantities, $+V_{CC}$ and $-V_{EE}$ as shown, so that the *dc* voltage at the output is zero. This is necessary to avoid a power-wasting direct current through the load. Apart from the positive/negative supply, the direct-coupled circuit operates in the same way as the capacitor-coupled amplifier.

With a few exceptions, the design procedure for a direct-coupled circuit is essentially the same as for a capacitor coupled circuit. Equation 18-15 gives the total supply voltage, and this must be halved to give $+V_{CC}$ and $-V_{EE}$ for the direct-coupled amplifier. The total supply voltage must be used to calculate P_t in Eq. 18-17. Also, the transistor maximum V_{CE} is the total supply voltage.

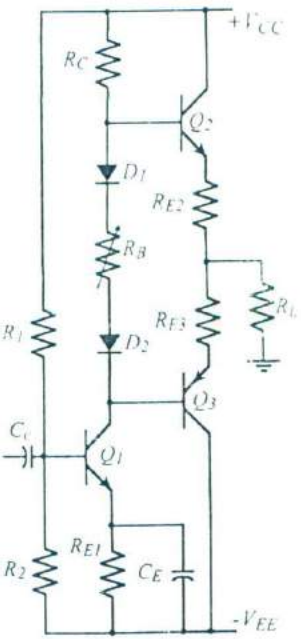


Figure 18-23
A direct-coupled Class-AB power amplifier must use plus-minus supply voltages.

Practise Problems

18-4.1 A Class-*AB* power amplifier, as in Fig. 18-23, is to dissipate 200 mW in a 60 Ω load. Calculate V_{CC}, and specify the output transistors.

18-4.2 Determine R_C and R_B for the amplifier in Problem 18-4.1.

18-5 Modifications to Improve Power Amplifier Performance

Darlington-Connected Output Transistors

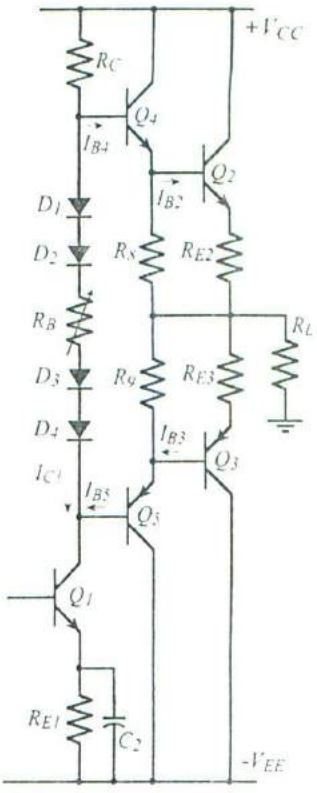
High-power transistors usually have low current gains, so relatively large base currents must flow into Q_2 and Q_3 in the circuits in Figs. 18-22 and 18-23 to supply a high load current. This means that the quiescent current through Q_1 must be large, and consequently resistor R_C is small. The small value of R_C keeps the amplifier voltage gain low. To improve on this situation, *Darlington-connected* output transistors may be used, as illustrated in Fig. 18-24(a). Transistors Q_4 and Q_5 in Fig. 18-24(a) are low-power devices that supply base current to output transistors Q_2 and Q_3, respectively. Note the four biasing diodes in Fig. 18-24(a) to bias the four transistor base-emitter junctions.

When peak load current (I_L) flows, the peak base current to Q_4 and Q_5 is,

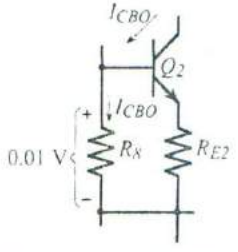
$$I_B = \frac{I_P}{h_{fe2} \times h_{fe4}}$$

This reduced base current allows $I_{RC(min)}$ to be smaller, giving a larger resistance for R_C, and resulting in a larger voltage gain.

Resistors R_8 and R_9 in Fig. 18-24(a) are included to bias Q_2 and Q_3 *off* when Q_4 and Q_5 are in cutoff. The largest possible resistance values should normally be selected for R_8 and R_9. When Q_2 and Q_3 are *off*, the collector-base leakage current I_{CBO} flows in R_8 and R_9 [see Fig. 18-24(b)]. The voltage drop across the resistors ($I_{CBO}R_8$) should be much smaller than the normal transistor base-emitter voltage. Selecting $I_{CBO}R_8$ equal to 0.01 V normally gives satisfactory resistor values. R_8 and R_9 are not required when power Darlingtons are used, as illustrated in Fig. 18-25.



(a) Darlington-connected output stage



(b) R_8 biases Q_2 *off*

Figure 18-24
Darlington-connected output transistors reduce the current to be supplied by R_C and Q_1, and allow R_C to be increased for a larger voltage gain.

Example 18-9

The Class-AB amplifier in Example 18-6 is to be redesigned to use power Darlingtons, as in Fig. 18-25. Assuming that the power Darlingtons have $h_{FE(min)} = 2000$, and $V_{EE} = 1.4$ V. Determine new values for: V_{CC}, R_C, and R_B.

Solution

from Ex. 18-6, $V_P = 10$ V, $I_P = 200$ mA, $I_{CQ2} = 20$ mA, $R_{E1} = R_{E2} = 4.7\ \Omega$, $V_{E1} = 3$ V, $V_{C1(dc)} = V_{RC(dc)} = 15.2$ V, $V_{RC(min)} = 4$ V

$$V_B = V_{BE2} + I_{CQ2}(R_{E2} + R_{E3}) + V_{BE3}$$
$$= 1.4\text{ V} + 20\text{ mA}(4.7\ \Omega + 4.7\ \Omega) + 1.4\text{ V}$$
$$= 3\text{ V}$$

$$V_{CC} = V_{RC(dc)} + V_{C1(dc)} + V_B = 15.2\text{ V} + 15.2\text{ V} + 3\text{ V}$$
$$= 33.4\text{ V}$$

use, $V_{CC}/V_{EE} = \pm 17$ V

$$I_{B2(max)} = \frac{I_P}{h_{FE2(min)}} = \frac{200\text{ mA}}{2000}$$
$$= 100\,\mu\text{A}$$

select, $I_{RC(min)} = 1\text{ mA}$

$$R_C = \frac{V_{RC(min)}}{I_{RC(min)}} = \frac{4\text{ V}}{1\text{ mA}}$$
$$= 4\text{ k}\Omega \text{ (use 3.9 k}\Omega\text{ standard value)}$$

$$I_{C1(dc)} = \frac{V_{RC(dc)}}{R_{C1}} = \frac{15.2\text{ V}}{3.9\text{ k}\Omega}$$
$$= 3.9\text{ mA}$$

$$R_B = \frac{V_B - (4 \times V_D)}{I_{C1(dc)}} = \frac{3\text{ V} - (4 \times 0.7\text{ V})}{3.9\text{ mA}}$$
$$\approx 51\,\Omega \text{ (use a 100 }\Omega\text{ variable resistor for adjustment)}$$

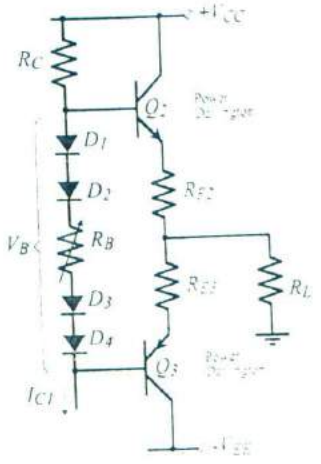


Figure 18-25
Class-AB output stage using power Darlingtons.

Quasi-Complementary Output Stage

The *quasi-complementary* circuit was originally developed because complementary high-power transistors were not readily available. Despite the fact that such transistors are now available, the quasi-complementary circuit is still widely used.

Consider the arrangement in Fig. 18-26. Q_3 is a high-power *npn* transistor, and Q_5 is a low-power *pnp* device. When Q_5 base current (I_{B5}) flows, the collector current of Q_5 behaves (largely) as base current (I_{B3}) for transistor Q_3. This produces a Q_3 collector current flow (I_{C3}), which combines with I_{E5} to constitute a current flow in the load. Because $I_{C3} >> I_{E5}$, the output current can be taken to be approximately I_{C3}:

$$I_{C3} = h_{FE3} \times I_{B3}$$

or,

$$I_{C3} = h_{FE3} \times h_{FE5} \times I_{B5}$$

This is the same as the current gain with Darlington-connected transistors.

Now note that when a negative-going input voltage is applied to the base of Q_5 a negative-going output occurs, because the emitter of Q_5 (and the collector of Q_3) follow the input voltage. Thus, the combination of transistors Q_3 and Q_5 in Fig. 18-26 behave as a high-power *pnp* emitter follower, just like Darlington-connected transistors Q_3 and Q_5 in Fig. 18-24(a). Because transistors Q_2 and Q_3 in Fig. 18-26 are both *npn* devices, they can be the same type of transistor. This eliminates any problem with finding suitable complementary high-power transistors. Resistor R_9 in Fig. 18-26 ensures that Q_3 is biased off when Q_5 goes into cutoff.

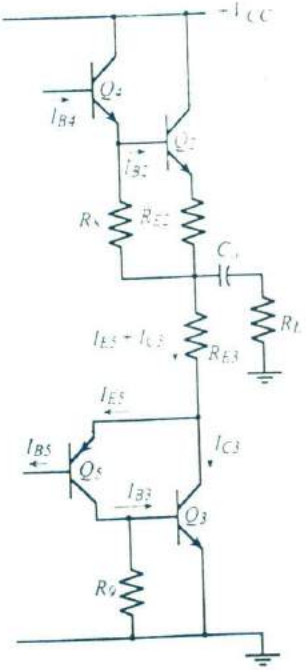


Figure 18-26
A quasi-complementary output stage allows output transistors to be the same type; Q_2 and Q_3 are both npn transistors.

Output Current Limiting

Because the output transistors can be destroyed by excessive current flow, output current limiting circuits are often included in a power amplifier. Figure 18-27 shows the typical arrangement for a current limiting circuit. Emitter resistors R_{E2} and R_{E3} are each made up of two components (R_A and R_B), as illustrated. The current limiting transistors (Q_4 and Q_5) are connected as shown, so that the voltage drop across R_{B2} and R_{B3} (produced by I_L) can turn Q_4 and Q_5 *on*. This occurs only when I_L is at the selected $I_{L(max)}$ level. When Q_4 turns *on*, it pulls the base of Q_2 *down*, so that Q_2 cannot supply current in excess of $I_{L(max)}$. Similarly, turning Q_5 *on* causes the base of Q_3 to be pulled *up* toward its emitter, thus again limiting the output current to $I_{L(max)}$.

As already discussed for voltage regulator current limiting circuits, Q_4 and Q_5 typically turn *on* when $V_{BE} \approx 0.5$ V, (see Section 17-3). The component values shown in Fig. 18-27 limit the peak output current to approximately 1 A. *Catch diodes* D_3 and D_4 in Fig. 18-27 are usually included with current limiting, to protect the output transistors from the excessive voltage levels generated in an inductive load when the current growth is limited. The diodes prevent the load voltage from exceeding the supply voltage level.

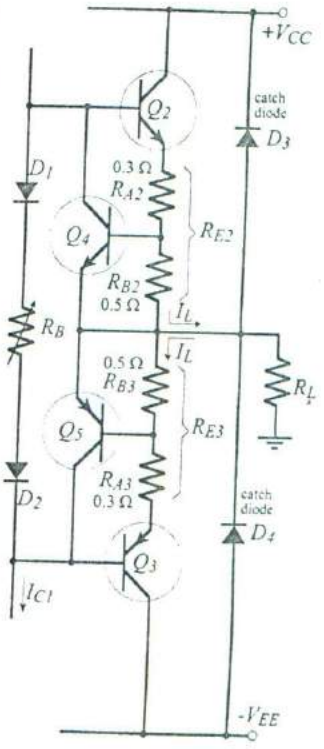


Figure 18-27
Current limiting transistors (Q_4 and Q_5) turn on when the load current is at the selected maximum. This stops further current increase in Q_2 and Q_3.

V_{BE} Multiplier

Figure 18-28 shows an alternative to diode biasing for the output stage transistors in a Class-*AB* amplifier. This circuit is known as a V_{BE} *multiplier* because it produces a bias voltage ($V_B = V_{CE6}$) which is a multiple of the V_{BE} of transistor Q_6. Referring to the circuit, note that I_{10} is the current through the the voltage divider (R_{10}, R_{11}, and R_{12}) that biases Q_6. Because I_{10} is much smaller than I_{C6}, the Q_1 collector current (I_{C1}) approximately equals I_{C6}.

$$I_{10} = \frac{V_{BE6}}{R_{11} + R_{12}}$$

$$V_B = I_{10}(R_{10} + R_{11} + R_{12})$$

or,

$$\boldsymbol{V_B = \frac{V_{BE6}(R_{10} + R_{11} + R_{12})}{R_{11} + R_{12}}} \qquad \textbf{(18-19)}$$

It is seen that the base bias voltage for the output stage transistors can be set by suitable selection of the V_{BE} multiplier resistors. The bias voltage remains constant when I_{C1} changes. Also, it can also be shown that the changes produced in V_B by temperature variations closely match the total V_{BE} temperature changes in the four output stage transistors.

Example 18-10

Design the V_{BE} multiplier in Fig. 18-28 to have $V_B = 3.2$ V adjustable by ± 0.5 V when $I_{C1} = 5$ mA.

Solution

$$V_{B(min)} = 3.2\text{ V} - 0.5\text{ V} = 2.7\text{ V}$$
$$V_{B(max)} = 3.2\text{ V} + 0.5\text{ V} = 3.7\text{ V}$$

select $I_{10} \approx 0.1\, I_{C1} = 0.1 \times 5\text{ mA}$
$\approx 500\,\mu\text{A}$

for $V_{CE} = 3.2$ V,
$$R_{10} = \frac{V_{CE} - V_{BE}}{I_{10}} = \frac{3.2\text{ V} - 0.7\text{ V}}{500\,\mu\text{A}}$$
$= 5\text{ k}\Omega$ (use 4.7 kΩ standard value)

for $V_{CE} = 3.7$ V,
$$I_{10(max)} = \frac{V_{CE(max)} - V_{BE}}{R_{10}} = \frac{3.7\text{ V} - 0.7\text{ V}}{4.7\text{ k}\Omega}$$
$= 638\,\mu\text{A}$

for $V_{CE} = 2.7$ V,
$$I_{10(min)} = \frac{V_{CE(min)} - V_{BE}}{R_{10}} = \frac{2.7\text{ V} - 0.7\text{ V}}{4.7\text{ k}\Omega}$$
$= 426\,\mu\text{A}$

$$R_{11} + R_{12} = \frac{V_{BE}}{I_{10(min)}} = \frac{0.7\text{ V}}{426\,\mu\text{A}}$$
$= 1.6\text{ k}\Omega$

$$R_{11} = \frac{V_{BE}}{I_{10(max)}} = \frac{0.7\text{ V}}{638\,\mu\text{A}}$$
$= 1.1\text{ k}\Omega$ (use 1 kΩ standard value)

$$R_{12} = (R_{11} + R_{12}) - R_{11} = 1.6\text{ k}\Omega - 1\text{ k}\Omega$$
$= 600\ \Omega$ (use a 750 Ω standard value potentiometer)

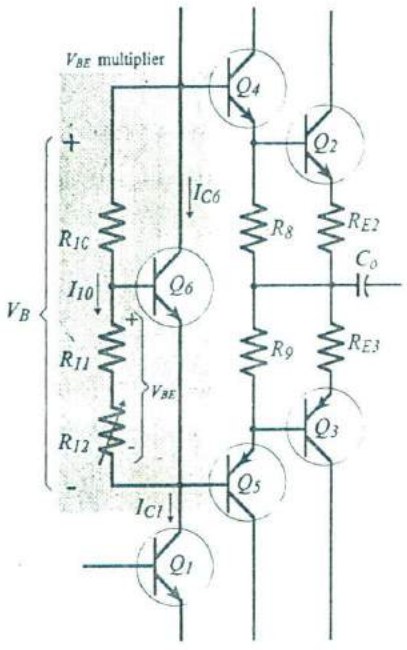
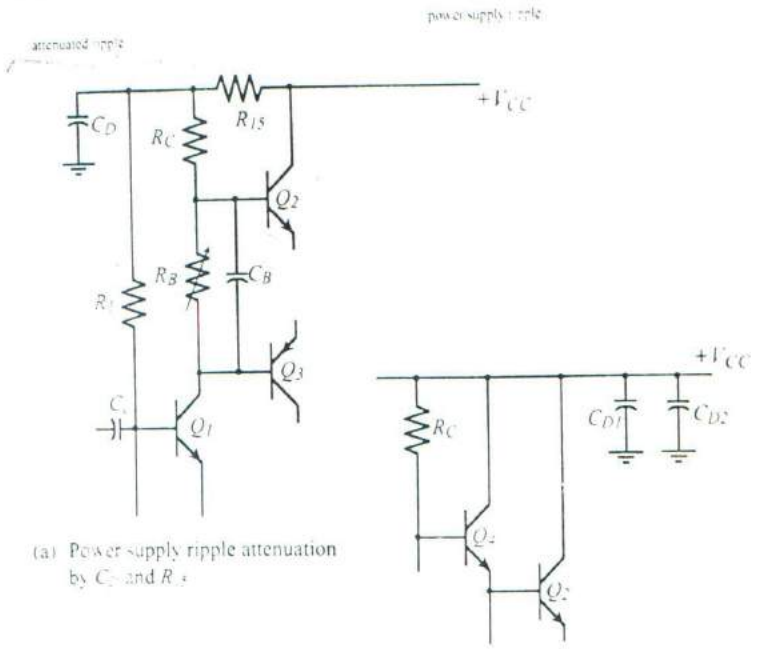


Figure 18-28
A V_{BE} multiplier is an alternative to diode biasing for the output transistors.

Power Supply Decoupling

High-power amplifiers require high supply current levels, so unregulated power supplies are often employed to avoid the power wasted in a series regulator. The high ripple voltage that occurs with unregulated supplies can be amplified to appear at speaker outputs as very unpleasant *power supply hum*. Supply *decoupling* components C_D and R_{15} are employed as shown in Fig. 18-29(a) to combat hum. Capacitive impedance X_{CD} forms an *ac* voltage divider with resistor R_{15}, so that the ripple amplitude is attenuated, as illustrated. The resistance of R_{15} is usually selected approximately equal to emitter resistor R_{E1}, and X_{CD} is made very much smaller than R_{15} at the ripple frequency (f_r). If $X_{CD} = R_{15}/100$ at f_r, the ripple voltage will be attenuated approximately by a factor of 100. The *dc* voltage drop across R_{15} must be taken into account when calculating V_{CC}.



(a) Power supply ripple attenuation by C_D and R_C

(b) Power supply decoupling by C_{D1} and C_{D2}

Figure 18-29
Decoupling capacitors are used to minimize power supply ripple voltage and supply line transients.

Figure 18-29(b) shows power supply decoupling capacitors (C_{D1} and C_{D2}) without any series connected resistors. These are often used even when the supply voltages are regulated and hum is not a problem. When a sudden high output current is switched *on* or *off*, the current change can produce short-lived (spike-type) voltage drops (*transient*) on the supply lines. These transients may be amplified to produce output distortion if they are allowed to appear at the supply lines for the first or second stages of a circuit. Capacitor C_{D1} is a relatively high-capacitance component that might normally be expected to perform the necessary decoupling. However, such capacitors usually offer a relatively high impedance to high-frequency variations or fast transients. Consequently, the high-frequency low-capacitance component C_{D2} is required to ensure satisfactory decoupling. *It is very important that decoupling capacitors be located right on circuit boards, as close as possible to the terminals of the circuit to be decoupled.*

Increased Voltage Gain and Negative Feedback

The Q_1 collector resistor (R_C) in the circuits discussed so far has its resistance limited by the need to supply base current to the *npn* output transistor. The resistance of R_C also dictates the Q_1 collector current level. This is shown by the $I_{C1(dc)}$ calculation in Ex. 18-6. A larger resistance for R_C would give a greater voltage gain, which is desirable for negative feedback. In Section 13-7 it is shown that negative feedback reduces distortion and increases circuit bandwidth, so its use is necessary in all power amplifiers.

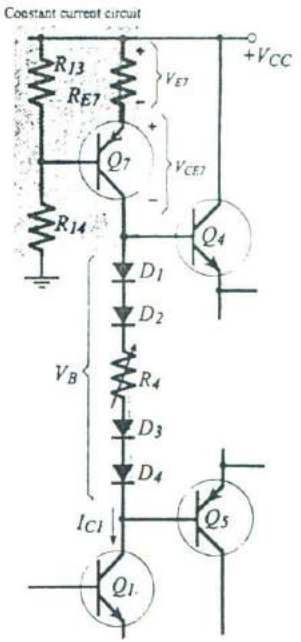


Figure 18-30
A constant-current circuit used as a load for Q_1 will increase the overall amplifier overall gain.

In Fig. 18-30 R_C is replaced by a constant current circuit (see Section 17-2) constituted by transistor Q_7 together with emitter resistor R_{E7}, and base bias resistors R_{13} and R_{14}. The minimum level of V_{CE7} and the R_{E7} voltage drop are selected to equal the Q_1 levels. This allows the voltage to the output stage to swing positively by the same amount as it can go negatively. The constant current circuit offers a high *ac* load resistance ($1/h_{oe7}$) for the Q_1 stage, to give the highest possible voltage gain.

Load Compensation

All design and analysis calculations for power amplifiers assume a resistive load with a given resistance value (R_L). For audio amplifiers, the load is usually the coil of a speaker which, as illustrated in Fig. 18-31, combines coil inductance L_c and winding resistance R_C. The load impedance is, $Z_L = R_c + j\,(2\pi f L_c)$, and clearly Z_L increases (from a low of R_c at *dc*) as the signal frequency increases. An 8 Ω speaker might offer an impedance of 8 Ω only at a frequency around 400 Hz. The fact that the load is inductive means that the load current lags the load voltage, and typically the phase angle could be as high as 60°. Similarly, when capacitive loads are involved the load current can lead the load voltage. The phase difference between load current and voltage can put stress on the output transistors, so output compensating components are often included to minimize the phase difference.

Figure 18-32 shows the typical arrangement of the compensating components. Inductor L_x and its parallel-connected resistor R_x are usually recommended by device and *IC* manufacturers for isolating a capacitive load. Capacitor C_o and series-connected resistor R_o help to correct the lagging phase angle of an inductive load.

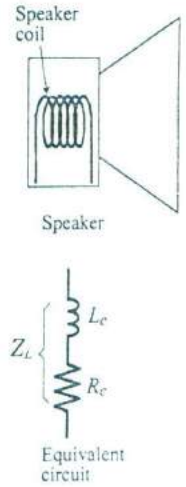


Figure 18-31
A speaker coil has resistance and inductance, so its impedance varies with signal frequency.

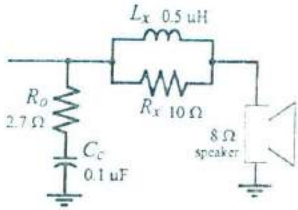


Figure 18-32
Typical arrangement of components to compensate for inductive and capacitive loads.

Practise Problems

18-5.1 A direct-coupled Class-*AB* power amplifier output stage, as in Fig. 18-24(a) is to deliver 5 W to a 8 Ω load. The output transistors are power Darlingtons with h_{FE} = 3000 and V_{BE} = 1.5 V. Calculate the required V_{CC} and the resistance values for R_C and R_B.

18-5.2 Design a V_{BE} multiplier to provide a (4 ± 0.7) V bias for a Class-*AB* output stage. The bias current (I_{C1}) is 2 mA.

18-5.3 The constant current circuit in Fig. 18-30 has V_{CC} = 25 V and I_{C1} = 3 mA. Determine suitable resistance values for R_{13}, R_{14}, and R_{E7}. Also, calculate the resistance for R_4 to give V_B = 3.5 V ± 0.4 V.

18-6 BJT Power Amplifier with Differential Input Stage

Amplifier Circuit

The direct-coupled amplifier in Fig. 18-33 has a differential-amplifier input stage constituted by transistors Q_1 and Q_2, (see Section 12-8). It also has an intermediate stage (Q_3) with a

constant current load (Q_4). Both pairs of output stage transistors (Q_5 and Q_7) and (Q_6 and Q_8) are in quasi-complementary configuration, instead of the usual complementary form. This arrangement helps to minimize the required supply voltage by removing the V_{BE} of the power transistors from the V_{CC} equation.

$$V_{CC} = V_P + V_{R14} + V_{BE5} + V_{CE3(min)} + V_{R9} \qquad \textbf{(18-20)}$$

$$V_{EE} = -(V_P + V_{R15} + V_{BE6} + V_{CE4(min)} + V_{R11})$$
$$= -V_{CC}$$

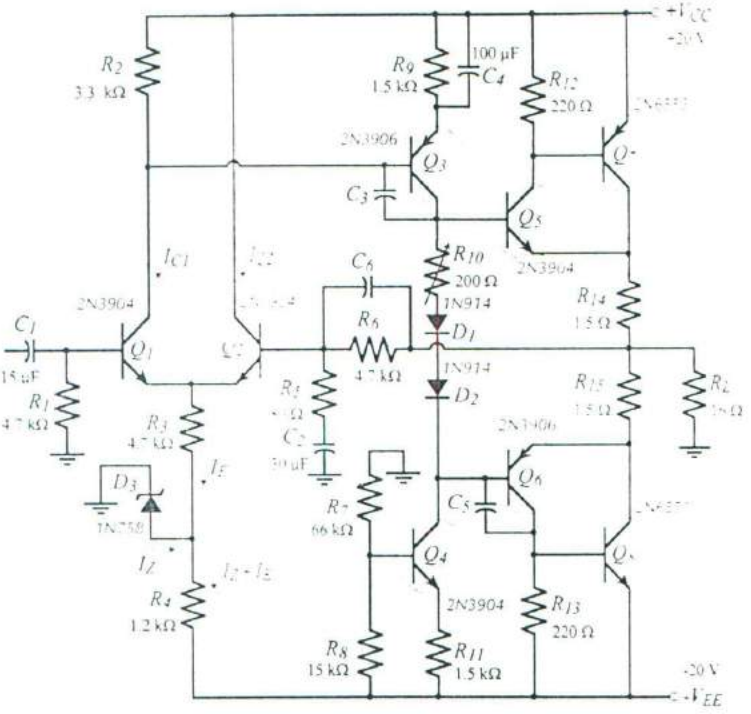


Figure 18-33
Complementary-symmetry Class-AB power amplifier with a quasi-complementary output stage, a differential input stage, and overall negative feedback. The closed-loop gain is $A_{CL} = (R_5 + R_6)/R_5$.

The differential input stage facilitates negative feedback (*NFB*), and the whole circuit functions like an operation amplifier. Q_1 base is the noninverting input, Q_2 base is the inverting input, and the junction of R_{14} and R_{15} is the output terminal. There is 100% *dc NFB* provided from the output via R_6 to Q_2 base. This keeps the output *dc* voltage at the same level as Q_1 base, (at ground). With C_2 behaving as an *ac* short-circuit, the *ac NFB* is divided by R_5 and R_6 to give a closed loop gain: $A_{CL} = (R_5 + R_6)/R_5$.

Zener diode D_3 and resistor R_4 decouple the power supply ripple on the negative supply line. The dynamic impedance of D_1 combined with R_4 functions as an *ac* voltage divider to attenuate the ripple at the emitters of Q_1 and Q_2. Ripple at this point is amplified just like an input signal. Capacitors C_3 and C_5 are frequency-compensating components, (see Section 15-2).

Amplifier Design

The design procedure for the output and intermediate stages of the circuit in Fig. 18-33 is similar to procedures already discussed. Design of the differential stages is very simple. The *dc* collector currents for Q_1 and Q_2 should be larger than the peak base current for Q_3, and the voltage drop across R_2 is $(V_{E3} + V_{BE3})$. Zener voltage V_{Z3} is any convenient level, usually around 0.5 V_{EE}. Resistor R_3 is calculated to pass $I_E = (I_{C1} + I_{C2})$, and R_4 must pass $(I_Z + I_E)$.

Q_1 bias resistor R_1 is determined from Eq. 5-17, R_6 is selected equal to R_1, and R_5 is calculated in terms of R_6 to give the desired closed-loop gain. The impedance of C_2 is made equal to R_5 at the desired lower cutoff frequency (f_1), so that C_2 sets f_1. Capacitors C_1 and C_4 are determined in the usual way for capacitors that are not to affect f_1. An additional capacitor (C_6) might be included to set the upper cutoff frequency (f_2): $(X_{C6} = R_6$ at $f_2)$.

Example 18-11

The amplifier circuit in Fig. 18-33 is to deliver 6 W to a 16 Ω load. Determine the required supply voltage and specify the output transistors.

Solution

from Eq. 18-8, $V_p = \sqrt{(2\ R_L\ P_o)} = \sqrt{(2 \times 16\ \Omega \times 6\ W)}$

$= 13.9\ V$

$V_{R14} = V_{R15} = 0.1\ V_P$

$\approx 1.4\ V$

$R_{14} = R_{16} = 0.1\ R_L$

$= 1.6\ \Omega$ (use 1.5 Ω standard value)

select, $V_{CE3(min)} = V_{CE4(min)} = 1\ V$

and, $V_{R9} = V_{R10} = 3\ V$

refer to Fig. 18-34,

$V_{CC} = \pm(V_P + V_{R14} + V_{BE5} + V_{CE3(min)} + V_{R9})$

$= \pm(13.9 + 1.4\ V + 0.7\ V + 1\ V + 3\ V)$

$= \pm 20\ V$

$I_P = \dfrac{V_P}{R_L} = \dfrac{13.9\ V}{16\ \Omega}$

$= 869\ mA$

dc power input from each supply line,

Eq. 18-17, $P_{i(dc)} = [V_{CC} - (V_{EE})] \times 0.35\ I_p$

$= [20\ V + 20\ V] \times 0.35 \times 869\ mA$

$\approx 12\ W$

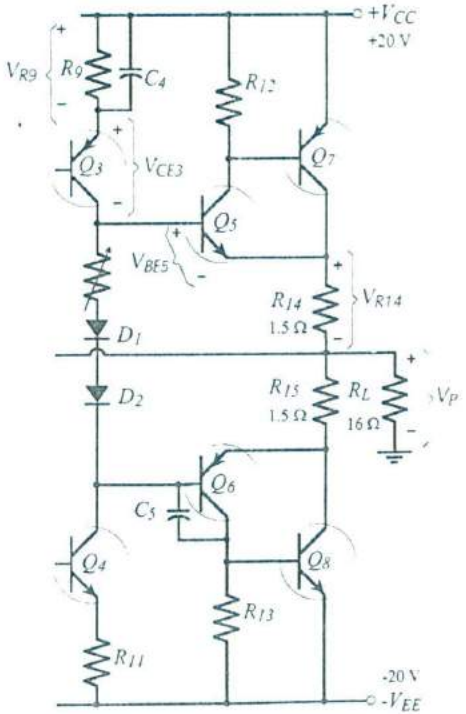


Figure 18-34
Output stage voltage drops for the circuit in Fig. 18-33.

Output transistor specification;

from Eq. 18-12, $P_T = 0.5\,(P_{a(dc)} - P_o) = 0.5\,(12\text{ W} - 6\text{ W})$

$= 3\text{ W}$

$V_{CE(max)} = 2\,V_{CC} = 2 \times 20\text{ V}$

$= 40\text{ V}$

$I_{C(max)} \approx 1.1\,I_p = 1.1 \times 869\text{ mA}$

$\approx 956\text{ mA}$

Example 18-12

Determine suitable resistor values for the output and intermediate stages of the circuit in Example 18-11. Assume that Q_7 and Q_8 have $h_{fl} = 20$ and $I_{CBO(max)} = 50\,\mu\text{A}$. Also, assume that Q_3 and Q_4 have $h_{fl} = 70$.

Solution

Refer to Fig. 18-35.

$$R_{12} = R_{13} = \frac{0.01\text{ V}}{I_{CBO}} = \frac{0.01\text{ V}}{50\,\mu\text{A}}$$

$= 200\ \Omega$ (use 220 Ω standard value)

$$I_{B7(peak)} = \frac{I_p}{h_{fl7} \times h_{fl5}} = \frac{869\text{ mA}}{20 \times 70}$$

$\approx 0.62\text{ mA}$

$I_{C3} > I_{B7(peak)}$

select $I_{C3} = 2\text{ mA}$

$$R_9 = R_{11} = \frac{V_{R9}}{I_{C3}} = \frac{3\text{ V}}{2\text{ mA}}$$

$= 1.5\text{ k}\Omega$ (standard value)

$I_{Q78} \approx Q_7, Q_8$ quiescent current

select $I_{Q78} \approx 0.1\,I_p = 0.1 \times 869\text{ mA}$

$\approx 86.9\text{ mA}$

$V_{R14(dc)} = V_{R15(dc)} = I_{Q78} \times R_{15}$

$= 86.9\text{ mA} \times 1.5\ \Omega$

$\approx 0.13\text{ V}$

$V_{R10(max)} = (V_{R14(dc)} + V_{R15(dc)}) + 50\%$

$= (0.13\text{ V} + 0.13\text{ V}) + 50\%$

$= 0.39\text{ V}$

$$R_{10} = \frac{V_{R10}}{I_{C3}} = \frac{0.39\text{ V}}{2\text{ mA}}$$

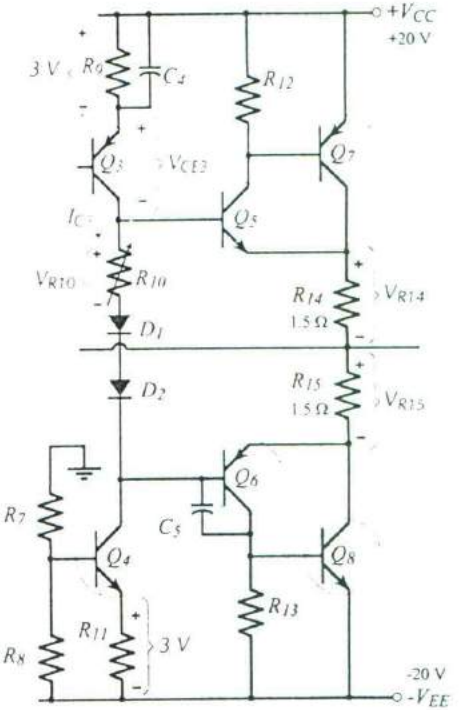


Figure 18-35
Intermediate and output stage dc voltage drops for the circuit in Fig. 18-33.

$= 195\ \Omega$ (use 200 Ω variable resistor)

select $R_8 = 10\,R_{11} = 15\ \text{k}\Omega$ (standard value)

$$I_{R8} = \frac{V_{R11} + V_{BI}}{R_8} = \frac{3\ \text{V} + 0.7\ \text{V}}{15\ \text{k}\Omega}$$

$$= 247\ \mu\text{A}$$

$$R_7 = \frac{V_{EE} - (V_{R11} + V_{BI})}{I_{R8}} = \frac{20\ \text{V} - (3\ \text{V} + 0.7\ \text{V})}{247\ \mu\text{A}}$$

$= 66\ \text{k}\Omega$ (use 56 kΩ + 10 kΩ)

Practise Problems

18-6.1 Design the input stage and feedback network for the circuit in Examples 18-11 and 18-12. The signal amplitude is ± 0.5 V, and the lower cutoff frequency is to be 30 Hz. Assume that transistors Q_1 through Q_4 have $h_{fe(min)} = 60$.

18-7 Complementary MOSFET Common-Source Power Amplifier

Advantages of MOSFETs

Power *MOSFETs* (described in Section 9-5) have several advantages over power *BJTs* for large signal amplifier applications. One of the most important differences is that *MOSFET* transfer characteristics (I_D/V_{GS}) are more linear than I_C/V_{BE} characteristics for *BJTs*. This helps to minimize distortion in the output waveform. Thermal runaway does not occur with power *MOSFETs*, so the emitter resistors in the *BJT* output stage (R_{14} and R_{15} in Fig. 18-33) are not needed in a *MOSFET* amplifier. Thus, the wasted power dissipation in the emitter resistors is eliminated.

Power *MOSFETs* can be operated in parallel to reduce the total channel resistance and increase the output current level. Unlike *BJTs* operated in parallel, there is no need for resistors to equalize current distribution between parallel-connected *MOSFETs*. For Class-*AB* operation, the *MOSFET* gate-source should be biased to the *threshold voltage* (V_{TH}) for the device, to ensure that it is conducting at a low level when no signal is present.

Power Amplifier with MOSFET Output Stage

The four output transistors in the amplifier circuit in Fig. 18-33 could be replaced with two power *MOSFETs* operating as source followers. However, the *FET* gate-source voltage must be included when calculating the supply voltage, so that a larger supply voltage would be required than with a *BJT* amplifier. In the power amplifier in Fig. 18-36 the complementary *MOSFETs* output devices operate as common source-amplifiers. As will be seen, this permits the peak output voltage to approach the supply voltage level.

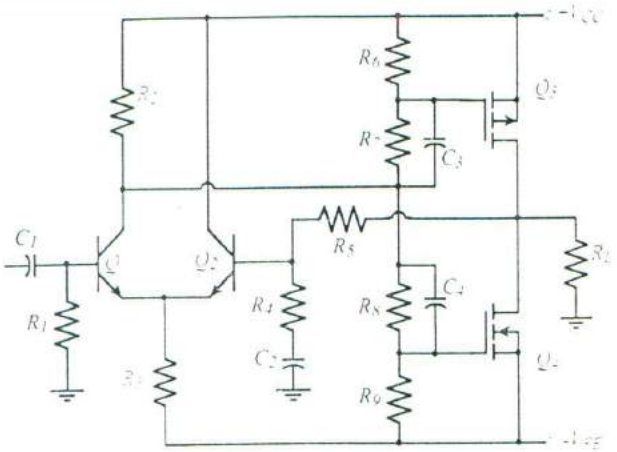


Figure 18-36
Class-AB power amplifier using a MOSFET output stage. Power MOSFETs Q_3 and Q_4 operate as common source amplifiers.

As in the case of the *BJT* circuit in Fig. 18-33, the differential amplifier input stage in Fig. 18-36 allows the use of *dc* negative feedback (via R_2) to stabilize the *dc* output voltage level, and *ac* negative feedback (via R_4 and R_5) to set the closed-loop voltage gain. Output transistors Q_3 and Q_4 are complementary *MOSFETs* and both are operated as common-source amplifiers. Resistors R_6 through R_9 provide bias voltage to set the gate-source voltage of Q_3 and Q_4 to the threshold level (V_{TH}) for the *MOSFETs*, (see Fig. 18-37). Resistors R_{10} can be included, as shown, to facilitate bias voltage adjustment. Capacitors C_3 and C_4 short-circuit R_7 and R_8 at signal frequencies, so that all of the *ac* voltage from the first stage is applied to the *MOSFET* gate terminals.

A positive-going voltage at Q_1 collector increases V_{GS4} and decreases V_{GS3}. Thus, Q_4 drain current is increased and Q_3 is turned *off*. (see Fig. 18-38). I_{D4} flows through R_L producing a negative-going load voltage. When the voltage at Q_{1C} is negative-going, V_{GS4} is decreased and V_{GS3} is increased. This causes I_{D4} to increased and Q_4 to be turned *off*. Load current now flows via Q_3 to produce a positive-going load voltage.

MOSFET Power Amplifier Design

In a Class-*AB MOSFET* power amplifier, the *FET* gate-source voltages should be biased to the minimum specified threshold voltage for the devices. The peak output voltage and current are calculated in the usual way, and the minimum supply voltage is,

$$V_{CC} = -[V_P + I_{DS}\, R_{D(on)}] \qquad \textbf{(18-21)}$$

where $R_{D(on)}$ is the *FET* channel resistance, (see Section 9-3).

The required gate-source voltage swing (ΔV_{GS}) is determined from I_P/g_{FS}. The input stage must provide for $\pm\Delta V_{GS}$ at Q_1 collector (Fig. 18-38). Power dissipation in Q_3 and Q_4 is determined in the same way as for a *BJT* stage. The selected *MOSFETs* must survive the total supply voltage and pass a drain current approximately equal to 1.1 I_P. Capacitor values are determined in the usual way.

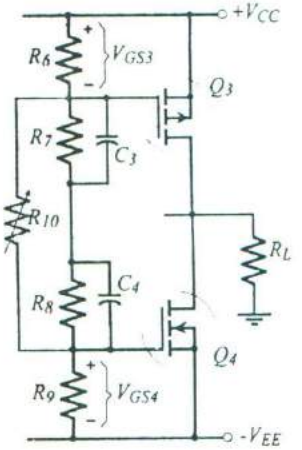


Figure 18-37
MOSFET gate-source bias voltage is provided by resistors R_6 through R_9.

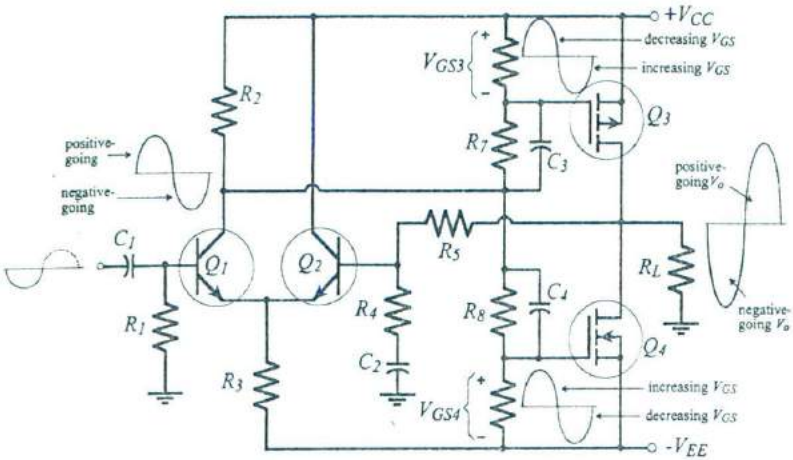


Figure 18-38
A positive-going voltage at Q_1 collector is applied to the gate-source terminals of Q_4 to produces a negative-going load voltage.

Example 18-13

The amplifier in Fig. 18-36 is to deliver 2.5 W to a 20 Ω load. The output MOSFETs have g_{FS} = 250 mA/V, V_{TH} = 1 V, and $R_{D(on)}$ = 4 Ω. Calculate the required supply voltage, and determine suitable *dc* voltage drops across R_2, R_3, and R_6 through R_9.

Solution

from Eq. 18-8, $V_p = \sqrt{(2\, R_L\, P_o)} = \sqrt{(2 \times 20\ \Omega \times 2.5\ W)}$

$= 10\ V$

$$I_p = \frac{V_p}{R_L} = \frac{10\ V}{20\ \Omega}$$

$= 500\ mA$

Eq. 18-21, $V_{CC} = \pm(V_P + I_p\, R_{D(on)}) = \pm[10\ V + (500\ mA \times 4\ \Omega)]$

$= \pm 12\ V$

$V_{R6} = V_{R9} = V_{TH} = 1\ V$

$$\Delta V_{R6} = \Delta V_{R9} = \frac{I_P}{g_{FS}} = \frac{500\ mA}{250\ mA/V}$$

$= 2\ V$

$V_{R2(min)} = V_{CE1(min)} = \Delta V_{R6} + 1\ V = 2\ V + 1\ V$

$= 3\ V$

select, $V_{CE1(dc)} = 3\ V$

then, $V_{R2(dc)} \approx V_{CC} - V_{CE1(dc)} = 12\ V - 3\ V$

$= 9\ V$

$V_{R3} = V_{EE} - V_{BE} = 12\ V - 0.7\ V$

$= 11.3\ V$

$$V_{R7} = V_{R2} - V_{R6} = 9\text{ V} - 1\text{ V}$$
$$= 8\text{ V}$$

$$V_{R8} = [V_{CC} - (-V_{EE})] - V_{R6} - V_{R7} - V_{R9}$$
$$= 12\text{ V} + 12\text{ V} - 1\text{ V} - 8\text{ V} - 1\text{ V}$$
$$= 14\text{ V}$$

Example 18-14

Determine resistor values for the MOSFET amplifier circuit in Example 18-13. The input signal is to be ±800 mV.

Solution

$$R_6 = R_3 < 1\text{ M}\Omega$$

select, $R_6 = R_4 = 100\text{ k}\Omega$

$$I_6 = \frac{V_{R6}}{R_6} = \frac{1\text{ V}}{100\text{ k}\Omega}$$
$$= 10\,\mu\text{A}$$

$$R_5 = \frac{V_{R5}}{I_6} = \frac{8\text{ V}}{10\,\mu\text{A}}$$
$$= 800\text{ k}\Omega\text{ (use 820 k}\Omega\text{ standard value)}$$

$$R_8 = \frac{V_{R8}}{I_6} = \frac{14\text{ V}}{10\,\mu\text{A}}$$
$$= 1.4\text{ M}\Omega\text{ (use 1.5 M}\Omega\text{ standard value)}$$

select, $I_{C1} = I_{C2} = 1\text{ mA}$

$$R_2 = \frac{V_{R2}}{I_{C1}} = \frac{9\text{ V}}{1\text{ mA}}$$
$$= 9\text{ k}\Omega\text{ (use 8.2 k}\Omega\text{ standard value)}$$

$$R_3 = \frac{V_{R3}}{I_{C1} + I_{C2}} = \frac{11.3\text{ V}}{1\text{ mA} + 1\text{ mA}}$$
$$= 5.65\text{ k}\Omega\text{ (use 5.6 k}\Omega\text{ standard value)}$$

Select, $R_1 = 4.7\text{ k}\Omega$ (from Eq. 5-17)

$R_5 = R_1 = 4.7\text{ k}\Omega$

$$A_{CL} = \frac{V_{p(out)}}{V_{p(in)}} = \frac{10\text{ V}}{800\text{ mV}}$$
$$= 12.5$$

$$R_4 = \frac{R_5}{A_{CL} - 1} = \frac{4.7\text{ k}\Omega}{12.5 - 1}$$
$$= 408\ \Omega\text{ (use 390 }\Omega\text{ standard value)}$$

Practise Problems

18-7.1 Calculate suitable capacitor values for the circuit in Examples 18-13 and 18-14 if the lower cutoff frequency is to be 20 Hz.

18-7.2 A *MOSFET* Class-*AB* amplifier as in Fig. 18-36 is to deliver 1 W to a 100 Ω load. The output devices have g_{fs} = 100 mS, V_{TH} = 1.3 V, and $R_{D(on)}$ = 6 Ω. Determine the supply voltage, and the *dc* voltage drops for the resistors.

18-7.3 Determine resistor and capacitor values for the circuit in Problem 18-7.2. The signal amplitude is ±0.4 V and the lower cutoff frequency is to be 40 Hz.

18-8 BJT Power Amplifier with Op-Amp Driver

Circuit Operation

The Class-*AB* power shown in Fig. 18-39 uses an operational amplifier (A_1) for the input stage. Resistors R_4 and R_5 together with the two diodes provide bias for the complementary emitter-follower *BJT* output stage. There is 100% *dc* negative feedback via R_3 to keep the *dc* output at the same level as the op-amp noninverting input, which is grounded via R_1. Overall *ac* negative feedback via R_2 and R_3 controls the amplifier *ac* voltage gain.

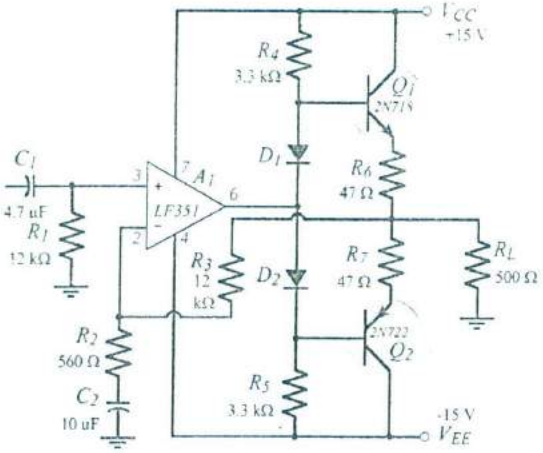
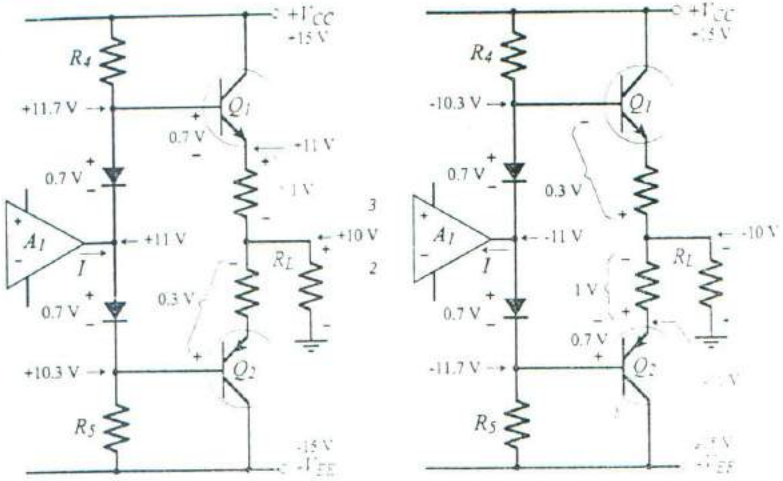


Figure 18-39
Complementary-symmetry Class-AB power amplifier using an operational amplifier and overall negative feedback.

No amplification is produced by the intermediate (output biasing) stage. Instead resistors R_4 and R_5 provide *active pull up* for transistors Q_1 and Q_2. When the op-amp output at the junction of D_1 and D_2 is increased in a positive direction, A_1 supplies current through D_2 and R_5. So, the voltage drop across R_4 is reduced, allowing it to pull the Q_1 base up to the required level while supplying increased base current to Q_1. This is illustrated by the example voltage levels shown in Fig. 18-40(a). Note that Q_2 is biased *off* when the output voltage is at its positive peak.



(a) Voltage levels when $V_o = -10$ V

(b) Voltage levels when $V_o = -10$ V

Figure 18-40
Output stage voltage levels for peak output voltages of ±10 V.

Figure 18-40(b) illustrates the situation when the op-amp output moves in a negative direction. A_1 pulls current through R_4 and D_1, leaving R_5 to pull the base of Q_2 down to the required voltage level while supplying the increased base current. Transistor Q_1 is biased *off* at this time, as indicated by the example voltage levels.

The circuit in Fig. 18-39 has no provision for adjusting the bias current in the output transistors. However, the diode voltage drops do bias Q_1 and Q_2 at least into a low-current *on* state. Although this might not seem enough to completely eliminate cross-over distortion, it should be recalled (from Eq. 13-28) that overall negative feedback (*NFB*) reduces distortion by a factor of $(1 + A_v B)$, where A_v is the circuit open-loop gain and B is the feedback factor. Thus, the high open-loop gain of the op-amp severely attenuates the cross-over distortion that would be present without *NFB*.

Use of Bootstrapping Capacitors

The resistance of (equal resistors) R_4 and R_5 (in Fig. 18-39) is limited by the need to supply base current to the output transistors. The calculation of R_C in Ex. 18-9 shows the process for determining R_4 and R_5. Also, there is a need for minimum voltage drop across R_4 and R_5 to produce the base current. Here again, this is shown in Ex. 18-9 where $V_{RC(min)}$ is the minimum voltage drop across R_C. This minimum resistor voltage requirement keeps the amplifier maximum peak output voltage well below the supply voltage level, and thus limits the amplifier efficiency.

The situation can be substantially improved by the use of the bootstrapping capacitors (C_3 and C_4) shown in Fig. 18-41. Resistors R_4 and R_5 are divided into two equal-value resistors (R_8 R_9 and R_{10} R_{11}), as illustrated, and the capacitors couple the output voltage back to the junctions of these components.

Consider the example supply voltage and *dc* bias levels shown in Fig. 18-42(a), where the Q_1 emitter resistor is left out for simplicity.

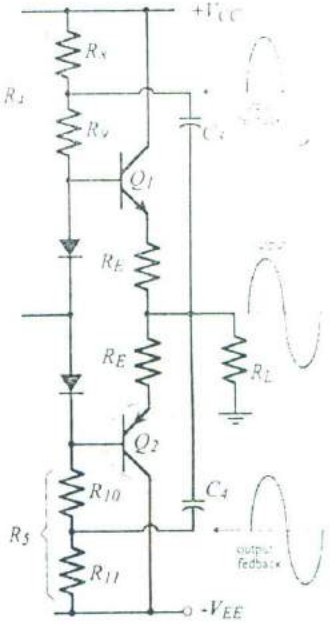


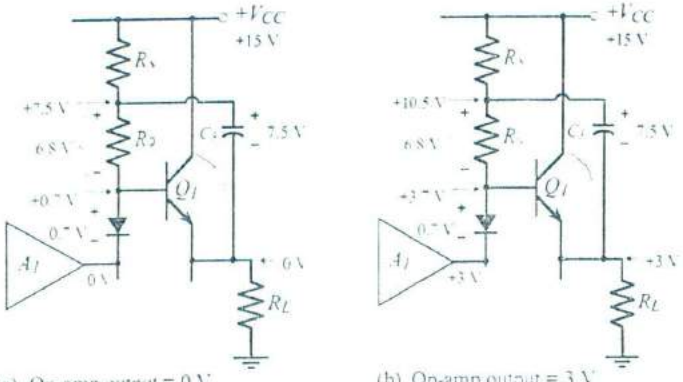
Figure 18-41
Bootstrapping capacitors used with a complementary emitter follower output stage can drive the output transistors close to saturation.

The output of A_1 is at 0 V. Q_1 base is at +0.7 V, and the load voltage is 0 V. The supply voltage is +15 V, the voltage at the junction of R_8 and R_9 is +7.5 V, and the voltage across C_3 is 7.5 V. Note that the voltage drop across R_9 is 6.8 V.

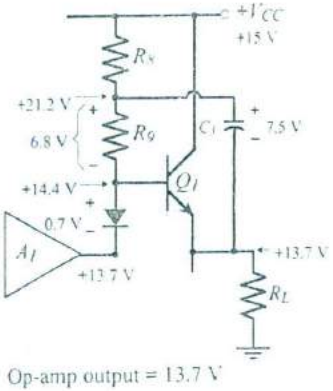
The new voltage levels that occur when the op-amp output increases by 3 V are shown in Fig. 18-42(b). Q_1 base is at +3.7 V, and the load voltage (V_o) is +3 V. Because C_3 is a large capacitor, its terminal voltage remains substantially constant at 7.5 V, so the junction of R_8 and R_9 is pushed up to:

$$V_o + V_{C3} = 3\text{ V} + 7.5\text{ V} = 10.5\text{ V}$$

With 10.5 V at one end of R_9 and 3.7 V at the other end, the voltage across R_9 is 6.8 V. This is the same level of V_{R9} that occurs when the op-amp output is zero. Thus, C_3 keeps V_{R9} constant. Recall that, without the bootstrapping capacitor, V_{R9} decreases when the op-amp output rises.



(a) Op-amp output = 0 V (b) Op-amp output = 3 V



(c) Op-amp output = 13.7 V

Figure 18-42
Output stage voltage levels for various levels of op-amp output voltage. The voltage on the bootstrapping capacitor remains constant.

Now consider the voltage levels shown in Fig. 18-42(c), where the op-amp output is +13.7 V. Q_1 base voltage is 14.4 V, V_o = +13.7, and the voltage at the R_8 R_9 junction is,

$$V_o + V_{C3} = 13.7\text{ V} + 7.5\text{ V} = 21.2\text{ V}$$

Once again, V_{R9} remains constant, however, note that the bootstrapping capacitor has actually driven the R_8 R_9 junction to a level higher than the supply voltage. This allows the output transistors to be driven into saturation, and the voltage drop across (R_8 + R_9) is no longer involved in the supply voltage calculation. In this case, the required supply voltage is,

$$V_{CC} = \pm[V_P + (I_P R_E) + V_{CE3(sat)}] \qquad \textbf{(18-22)}$$

The peak output voltage can also be limited by the output voltage range of the op-amp. For most op-amps the output voltage range is 1 V to 1.5 V less than the positive and negative supply levels. However, *rail-to-rail* op-amps are available with an output that ranges from $+V_{CC}$ to $-V_{EE}$.

Example 18-15

Analyze the amplifier circuit in Fig. 18-43 to determine the bootstrap capacitor terminal voltage (V_{C2}), peak output voltage (V_p), and the peak output power (P_o). The transistors have $V_{CE(sat)}$ = 1.5 V.

Solution

When V_i = 0 V:

$$I_2 = \frac{V_{CC} - V_{D1}}{R_8 + R_9} = \frac{17\text{ V} - 0.7\text{ V}}{1.5\text{ k}\Omega + 1.5\text{ k}\Omega}$$

$$= 5.4\text{ mA}$$

$$V_{C2} = V_{CC} - (I_2 R_8)$$

$$= 17\text{ V} - (5.4\text{ mA} \times 1.5\text{ k}\Omega)$$

$$= 8.9\text{ V}$$

$$V_p + V_{R6} = V_{CC} - V_{CE(sat)} = 17\text{ V} - 1.5\text{ V}$$

$$= 15.5\text{ V}$$

$$I_P = \frac{V_P + V_{R6}}{R_L + R_6} = \frac{15.5\text{ V}}{100\ \Omega + 8.2\ \Omega}$$

$$= 143\text{ mA}$$

$$V_p = I_P R_L = 143\text{ mA} \times 100\ \Omega$$

$$= 14.3\text{ V}$$

$$P_o = \frac{V_p^2}{2 R_L} = \frac{(14.3\text{ V})^2}{2 \times 100\ \Omega}$$

$$= 1\text{ W}$$

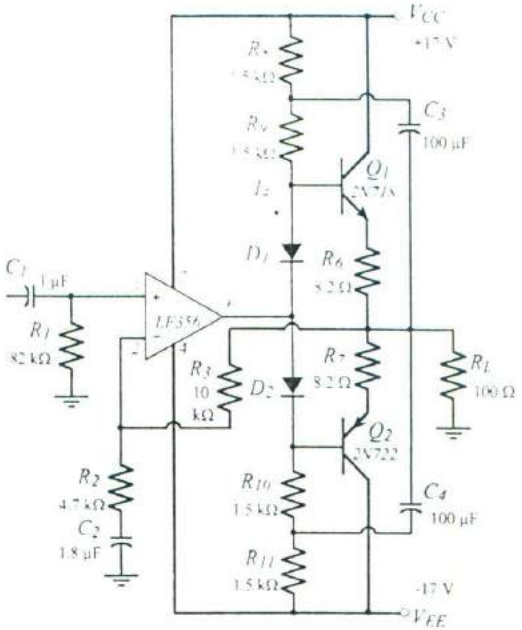


Figure 18-43
Power amplifier circuit for Examples 18-15.

Design Procedure

The amplifier in Fig. 18-44 uses four diodes to forward bias the base-emitter junctions of the Darlington output transistors. Otherwise, the circuit is exactly the same as in Fig. 18-43.

As always, the peak output voltage and current are calculated from the specified output power and load resistance. The supply voltage is determined using Eq. 18-22, and the emitter resistors for the output stage are typically selected as 0.1 R_L. The bias network current (I_4) should be larger than the peak base current for Q_1 and Q_2. The resistance of R_4 (which equals $R_8 + R_9$) is calculated from I_4 and the circuit *dc* voltage drops. R_8 should typically be selected as 0.5 R_4, and then R_9, R_{10}, and R_{11} are all equal to R_8.

R_1 and R_3 are equal-value resistors that bias the op-amp input terminals. R_2 is calculated from R_3 to give the required voltage gain. C_2 is selected to have its impedance equal to R_2 at the desired lower cutoff frequency (f_1). The bootstrapping capacitors are calculated in terms of the resistance in series with them; $R_8 \| R_9$. The op-amp must have a suitable full power bandwidth (see Section 15-3) to produce the peak output voltage at the desired upper cutoff frequency for the amplifier.

Example 18-16

The circuit in Fig. 18-44 uses a *BIFET* op-amp. $R_L = 8\ \Omega$, P_o is to be 6 W, and $v_s = \pm 0.1$ V. Q_1 and Q_2 are Darlingtons with $h_{FE(min)} = 1000$ and $V_{CE(sat)} = 2$ V. Determine a suitable supply voltage and resistor values. Also, calculate the minimum op-amp slew rate to give $f_2 = 50$ kHz.

Solution

from Eq. 18-8, $V_p = \sqrt{(2 R_L P_o)} = \sqrt{(2 \times 8\ \Omega \times 6\ \text{W})}$

$= 9.8$ V

$$I_p = \frac{V_p}{R_L} = \frac{9.8\ \text{V}}{8\ \Omega}$$

$= 1.2$ A

select, $R_6 = R_7 \approx 0.1\ R_L = 0.1 \times 8\ \Omega$

$\approx 0.8\ \Omega$

Eq. 18-22, $V_{CC} = \pm[V_p + I_p R_6 + V_{CE3(sat)}]$

$= \pm[9.8\ \text{V} + (1.2\ \text{A} \times 0.8\ \Omega) + 2\ \text{V}]$

$\approx \pm 12.8$ V (use ± 13 V)

$$I_{B1(peak)} = \frac{I_p}{h_{FE1}} = \frac{1.2\ \text{A}}{1000}$$

$= 1.2$ mA

$I_4 > I_{B3(peak)}$

select, $I_4 = 2$ mA

$$R_4 = \frac{V_{CC} - V_{D1} - V_{D2}}{I_4} = \frac{13\ \text{V} - 0.7\ \text{V} - 0.7\ \text{V}}{2\ \text{mA}}$$

$= 5.8$ kΩ

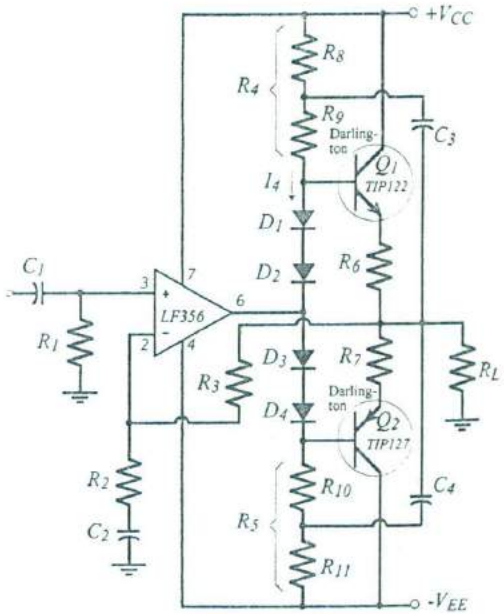


Figure 18-44
Power amplifier circuit for Examples 18-16 and 18-17.

$$R_B = R_{B1} = R_{B2} = R_{11} = 0.5\,R_1$$
$$= 0.5 \times 5.8\ \text{k}\Omega$$
$$= 2.9\ \text{k}\Omega \text{ (use 2.7 k}\Omega \text{ standard value)}$$

$$A_{CL} = \frac{V_o}{V_{in}} = \frac{9\ \text{V}}{0.1\ \text{V}}$$
$$= 90$$

select, $R_1 = R = 100\ \text{k}\Omega$ (see *BIFET* in Section 14-2

$$R_2 = \frac{R_1}{A_{CL} - 1} = \frac{100\ \text{k}\Omega}{90 - 1}$$
$$= 1.12\ \text{k}\Omega \text{ (use 1 k}\Omega)$$

Eq. 15-3, $SR = 2\pi f_2 V_o = 2\pi \times 50\ \text{kHz} \times 9\ \text{V}$
$= 2.8\ \text{V}/\mu\text{s}$

Example 18-17

Calculate capacitor values for the circuit in Ex. 18-16. The lower cutoff frequency is to be 50 Hz.

Solution

$X_{C1} = 0.1\,R_1$ at f_1

$$C_1 = \frac{1}{2\pi f_1 \times 0.1\,R_1} = \frac{1}{2\pi \times 50\ \text{Hz} \times 0.1 \times 100\ \text{k}\Omega}$$
$$= 0.18\ \mu\text{F} \text{ (use 0.33 }\mu\text{F)}$$

$X_{C2} = R_2$ at f_1

$$C_2 = \frac{1}{2\pi f_1 R_2} = \frac{1}{2\pi \times 50\ \text{Hz} \times 1\ \text{k}\Omega}$$
$$= 3.18\ \mu\text{F} \text{ (use 3.3 }\mu\text{F)}$$

$X_{C3} = X_{C4} = 0.1(R_B \| R_9)$ at $f_1 = 0.1\,(2.7\ \text{k}\Omega \| 2.7\ \text{k}\Omega$
$= 135\ \Omega$

$$C_3 = C_4 = \frac{1}{2\pi f_1 X_{C3}} = \frac{1}{2\pi \times 50\ \text{Hz} \times 135\ \Omega}$$
$$= 23.6\ \mu\text{F} \text{ (use 25 }\mu\text{F)}$$

Practise Problems

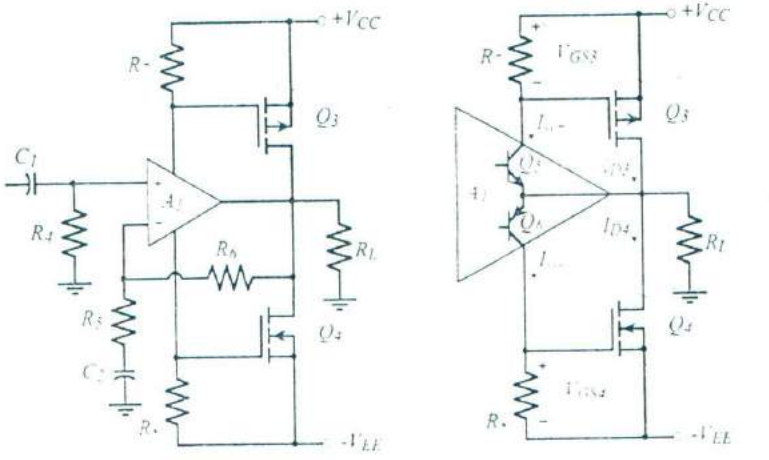
18-8.1 Calculate $V_{p(out)}$ and P_o for the circuit in Fig. 18-39 when $V_{in} = \pm 0.54$ V. Also, determine f_2 when a *741* op-amp is used.

18-8.2 Calculate the supply voltage for an amplifier as in Fig. 18-44 to deliver 3 W to a 12 Ω load. Assume $h_{FE(min)} = 1500$ and $V_{CE(sat)} = 2$ V for Q_1 and Q_2. Also, determine the op-amp minimum slew rate to give $f_2 = 65$ kHz.

18-9 MOSFET Power Amplifier with OP-Amp Driver Stage

Basic Circuit Operation

The Class-*AB* power amplifier circuit in Fig. 18-45(a) consists of an operational amplifier (A_1), two *MOSFETs* (Q_3 and Q_4), and several resistors. The op-amp together with resistors R_4, R_5, and R_6, and capacitor C_2 constitutes a non-inverting amplifier. The two *MOSFETs* are a complementary common-source output stage, like the output stage for the circuit discussed in Section 18-7.



(a) Basic circuit of common-source amplifier

(b) Op-amp output stage controls V_{GS3} and V_{GS4}

Figure 18-45
Complementary common-source power amplifier using an op-amp driver stage and a MOSFET output stage.

The gate-source bias voltages for Q_3 and Q_4 are provided by the voltage drops across resistors R_7 and R_8, which are in series with the op-amp supply terminals. So, the op-amp supply currents ($I_{S(+)}$ and $I_{S(-)}$) determine the levels of V_{GS3} and V_{GS4}:

$$V_{GS3} = I_{S(+)} \times R_7 \qquad \textbf{(18-23)}$$

and,

$$V_{GS4} = I_{S(-)} \times R_8 \qquad \textbf{(18-24)}$$

Suitable gate-source *threshold voltages* ($V_{GS(th)}$) to bias the output transistors for Class-*AB* operation, and typical op-amp supply currents (I_S) can be determined from the device data sheets.

Figure 18-45(b) shows that the op-amp supply currents are largely the collector currents in the op-amp output stage *BJTs* (Q_5 and Q_6). Thus, R_7 and R_8 are collector resistors for Q_5 and Q_6. When the base voltage for Q_5 and Q_6 is increased in a positive direction, Q_5 collector current ($I_{S(+)}$) increases, causing V_{GS3} to increase, and thus increasing the *MOSFET* drain current I_{D3}. At the same time, the Q_6 collector current ($I_{S(-)}$) decreases, reducing V_{GS4} and drain current I_{D4}. The result I_{D3} flows through R_L producing a positive output voltage swing ($+V_o$). Note that the op-amp output voltage is also positive at this time.

When the base voltage at Q_5 and Q_6 is negative-going, $I_{S(-)}$ increases, causing an increase in V_{GS4} and an increased level of I_{D4}. During this time, $I_{S(+)}$ decreases, reducing V_{GS3} and I_{D3}. Thus, I_{D4} flows through R_L producing a negative output voltage swing ($-V_o$). The op-amp output voltage is also going negative during the time that Q_4 is creating the negative output voltage across R_L.

It is seen that *BJTs* Q_5 and Q_6 operate as common-emitter amplifier stages, and that *MOSFETs* Q_3 and Q_4 function as common-source circuits. Both stages produce voltage gain which should be multiplied with the op-amp open-loop gain to determine the total open-loop gain for the circuit. Using typical quantities, the overall open-loop gain can be shown to be around 4×10^6.

Returning to Fig. 18-45(a), the complete (basic) circuit operates as a non-inverting amplifier with a closed-loop voltage gain:

$$A_{CL} = \frac{R_5 + R_6}{R_5} \qquad \textbf{(18-25)}$$

As explained, the power *MOSFETs* produce the high output current required by the amplifier load. An op-amp operating alone could not supply the load current.

Example 18-18

Determine the *MOSFET* gate-source bias voltages for the complementary common-source power amplifier in Fig. 18-46. Also, calculate the peak output voltage, peak output current, and output power if the *ac* input is ±100 mV.

Solution

From the *LF351* op-amp data sheet:

supply current, $I_S = 1.8$ mA to 3.4 mA

$$V_{GS3} = V_{GS4} = I_S \times R_7$$

$$V_{GS(min)} = I_{S(min)} \times R_7 = 1.8 \text{ mA} \times 820\ \Omega \approx 1.5 \text{ V}$$

$$V_{GS(max)} = I_{S(max)} \times R_7 = 3.4 \text{ mA} \times 820\ \Omega \approx 2.9 \text{ V}$$

Eq. 18-25,
$$A_{CL} = \frac{R_5 + R_6}{R_5} = \frac{390\ \Omega + 18\ \text{k}\Omega}{390\ \Omega} \approx 47.2$$

$$V_p = A_{CL} \times V_i = 47.2 \times 100 \text{ mV} = 4.72 \text{ V}$$

$$I_p = \frac{V_p}{R_L} = \frac{4.72 \text{ V}}{10\ \Omega} = 472 \text{ mA}$$

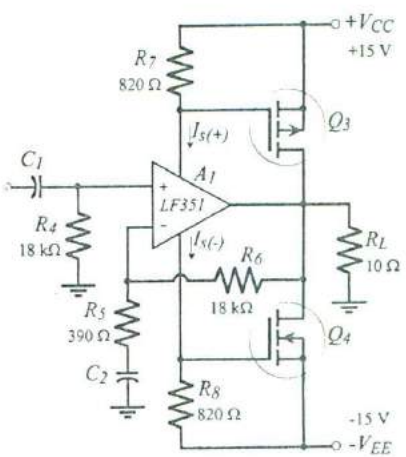
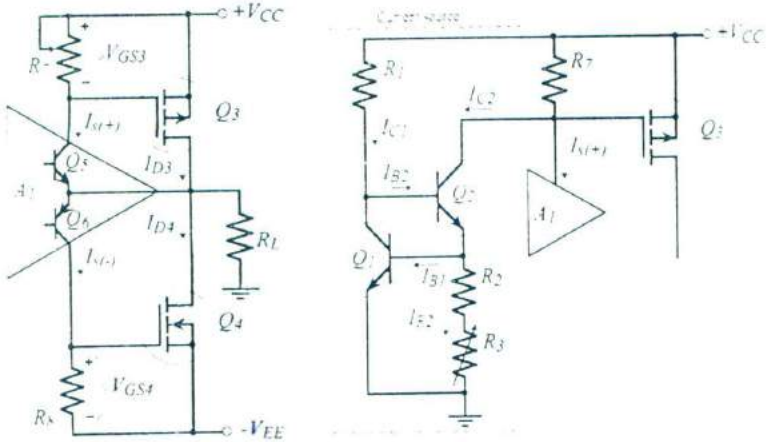


Figure 18-46
Power amplifier circuit for Example 18-18.

$$P_o = \frac{V_p I_p}{2} = \frac{4.72\text{ V} \times 472\text{ mA}}{2}$$
$$= 1.11\text{ W}$$

Bias Control

As previously discussed, the bias current in the output transistors of a power amplifier should be adjustable. Control over the bias current flowing in transistor Q_3 in Fig. 18-47(a) might be achieved by using a variable resistor for R_7, as illustrated. This allows I_{D3} to be adjusted by varying V_{GS3}. When I_{D3} is increased, and the additional drain current flows through R_L, the *dc* feedback (via R_6 in Fig. 18-46) keeps the V_o equal to zero. The feedback produces the necessary change in V_{GS4} to make I_{D4} closely follow I_{D3}. Thus, adjustment of resistor R_7 controls the level of I_{D4} as well as I_{D3}.



(a) R_7 adjustment alters V_{GS3} and V_{GS4}

(b) Current source for adjustment of Q_3 and Q_4 bias

Figure 18-47
The gate-source bias voltage for the two output MOSFETs can be adjusted by making R_7 adjustable, or by the use of a current source.

A disadvantage of using R_7 to adjust the bias current is that the voltage gains produced by Q_5 and Q_6 become unequal when R_7 and R_8 have different resistance values. This can be overcome by the negative feedback, however, the bias resistors can be kept equal by using the variable current source shown in Fig. 18-47(b).

In the variable current source, transistor Q_1 is biased from the emitter of Q_2, and the Q_2 base is connected to the collector of Q_1. The collector-emitter voltage of Q_1 is,

$$V_{CE1} = V_{BE1} + V_{BE2} = 2V_{BE}$$

Assuming that $I_{B2} << I_{C1}$, the Q_1 collector current is,

$$\boldsymbol{I_{C1} = \frac{V_{CC} - 2V_{BE}}{R_1}} \qquad \textbf{(18-26)}$$

With $I_{B1} << I_{E2}$, the Q_2 collector current is approximately,

$$I_{C2} = \frac{V_{BE}}{R_2 + R_3} \qquad (18\text{-}27)$$

Variable resistor R_3 controls the level of I_{C2}. Also,

$$V_{GS3} = (I_{S(+)} + I_{C2})\, R_7 \qquad (18\text{-}28)$$

As explained, the *dc* negative feedback causes V_{GS4} to always be equal to V_{GS3}. So, R_3 controls the *MOSFET* gate-source voltages, and thus controls the quiescent drain current. The *ac* load offered to the collector of Q_5 [see Fig. 18-45(b)] is R_7, regardless of the Q_2 current. Consequently, the Q_5 and Q_6 stage gains are equal.

Example 18-19

Calculate the $V_{GS3(max)}$ and $V_{GS3(min)}$ obtainable by adjusting R_3 for the current source circuit in Fig. 18-48.

Solution

Eq. 18-27. $I_{C2} = \dfrac{V_{BE}}{R_2 + R_3}$

$$I_{C2(max)} = \frac{V_{BE}}{R_2} = \frac{0.7\text{ V}}{560\ \Omega}$$

$$= 1.25\text{ mA}$$

$$I_{C2(min)} = \frac{V_{BE}}{R_2 + R_3} = \frac{0.7\text{ V}}{560\ \Omega + 1\text{ k}\Omega}$$

$$= 449\ \mu\text{A}$$

Eq. 18-28. $V_{GS3} = (I_{S(+)} + I_{C2})\, R_7$

$$V_{GS3(min)} = (2\text{ mA} + 449\ \mu\text{A}) \times 820\ \Omega$$
$$= 2\text{ V}$$

$$V_{GS3(max)} = (2\text{ mA} + 1.25\text{ mA}) \times 820\ \Omega$$
$$\approx 2.7\text{ V}$$

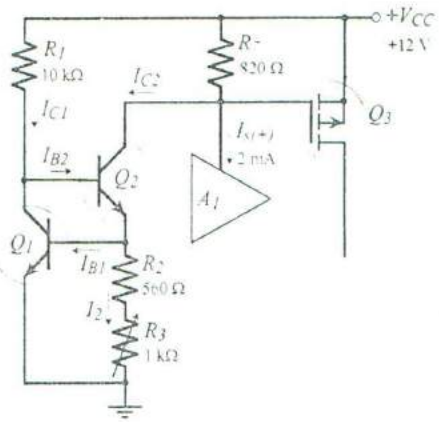


Figure 18-48
Current source circuit for Example 18-19.

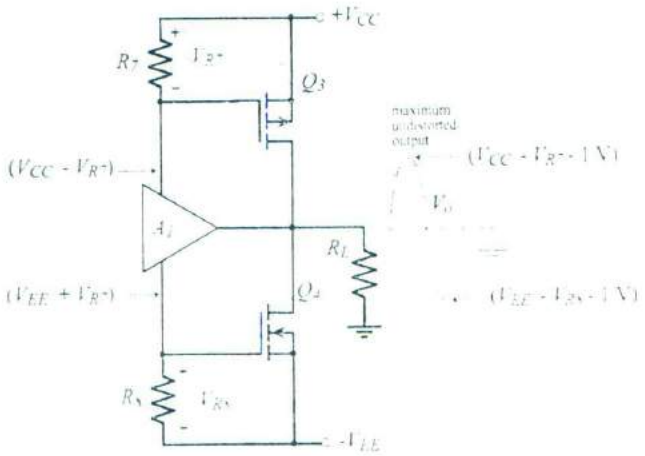
Output Voltage Swing

One problem with the basic circuit in Fig. 18-45 is that the output voltage swing is limited by the voltage levels at the op-amp supply terminals. As illustrated in Fig. 18-49(a), the positive supply voltage to the op-amp is $(V_{CC} - V_{R7})$, and the negative supply voltage is $-(V_{EE} - V_{R8})$. Also, recall that V_{R7} must be increased by ΔV_{GS3} in order to drive the output in a positive direction, and V_{R8} must be increased by ΔV_{GS4} to drive V_o negative.

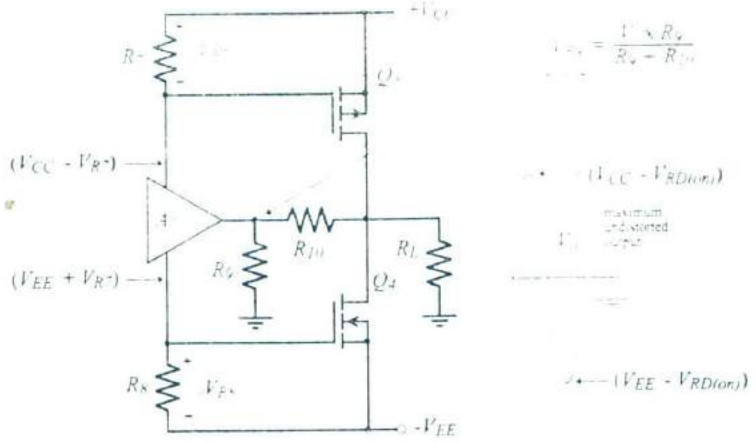
$$\Delta V_{GS} = \frac{I_p}{g_{fs}} \qquad (18\text{-}29)$$

In Eq. 18-29, I_p is the peak output voltage delivered to R_L, and g_{fs} is the *MOSFET* forward transconductance. Thus, the minimum supply voltage levels at the op-amp terminals are.

$$V_S = \pm(V_{CC} - V_{R7} - \Delta V_{GS}) \qquad \textbf{(18-30)}$$



(a) The output voltage swing is limited to approximately $\pm(V_{CC} - V_{R7} - 1\text{ V})$



(b) Voltage divider R_9 and R_{10} allows the output swing to go to $\pm(V_{CC} - V_{RD(on)})$

Figure 18-49
The common source amplifier circuit can be modified to produce an output swing larger than the op-amp maximum output.

The op-amp peak output voltage is normally limited to approximately 1 V below the voltages at the supply terminals, (although, as previously noted, *rail-to-rail* op-amp are available). Consequently, the output voltage swing from the circuit is likely to be less than $\pm(V_{CC} - 4\text{ V})$, [see fig. 18-49(a)]. For greatest efficiency, it is necessary to drive the output as closely as possible to $\pm V_{CC}$. This can be achieved by the circuit modification shown in Fig. 18-49(b).

Resistors R_9 and R_{10} in Fig. 18-49(b) divide V_o, so that the op-amp output can be substantially lower than the peak output

voltage developed across R_L. This means that the voltage levels at the op-amp supply terminals no longer limits the amplifier output voltage swing. Now, the largest peak output voltage that can be achieved is limited only by the supply voltage and $R_{D(on)}$.

$$V_p = \frac{V_{CC} \times R_L}{R_{D(on)} + R_L} \qquad \textbf{(18-31)}$$

R_9 and R_{10} also provide negative feedback that controls the gain of the stage made up of the op-amp output *BJTs* and the common-source *MOSFETs*. This is illustrated in Fig. 18-50. A further function of R_9 and R_{10} is that they can be selected to limit the op-amp output current in the event of R_L becoming short-circuited.

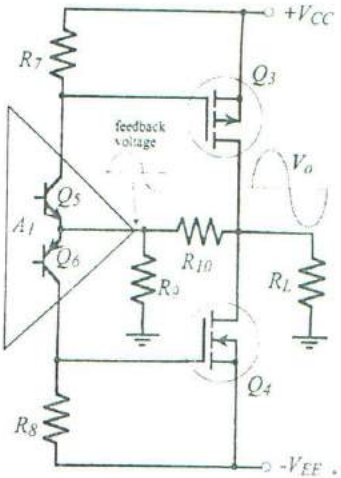


Figure 18-50
Negative feedback to the emitters of Q_5 and Q_6 controls the gain of the $(Q_5$-$Q_6)$—$(Q_3$-$Q_4)$ stage.

Example 18-20

The circuit in Fig. 18-51 has *MOSFETs* with g_{fs} = 2.5 S, and $R_{D(on)}$ = 0.5 Ω. Determine the maximum peak output voltage, the minimum supply voltage at op-amp terminals, and the op-amp peak output voltage when the circuit is producing maximum output power.

Solution

Eq. 18-31,
$$V_p = \frac{V_{CC} \times R_L}{R_{D(on)} + R_L} = \frac{12\text{ V} \times 10\ \Omega}{0.5\ \Omega + 10\ \Omega}$$
$$= 11.43\text{ V}$$

$$I_p = \frac{V_p}{R_L} = \frac{11.43\text{ V}}{10\ \Omega}$$
$$= 1.14\text{ A}$$

Eq. 18-29,
$$\Delta V_{GS} = \frac{I_p}{g_{fs}} = \frac{1.14\text{ A}}{2.5\text{ S}}$$
$$= 0.46\text{ V}$$

$$V_{R7(dc)} = I_S \times R_7 = 2\text{ mA} \times 820\ \Omega$$
$$= 1.64\text{ V}$$

Eq. 18-30,
$$V_{S(min)} = \pm(V_{CC} - V_{R7(dc)} - \Delta V_{GS}) = \pm(12\text{ V} - 1.64\text{ V} - 0.46\text{ V})$$
$$= \pm 9.9\text{ V}$$

The op-amp peak output voltage is,

$$V_{R9} = \frac{V_p \times R_9}{R_9 + R_{10}} = \frac{11.43\text{ V} \times 1\text{ k}\Omega}{1\text{ k}\Omega + 1\text{ k}\Omega}$$
$$= 5.72\text{ V}$$

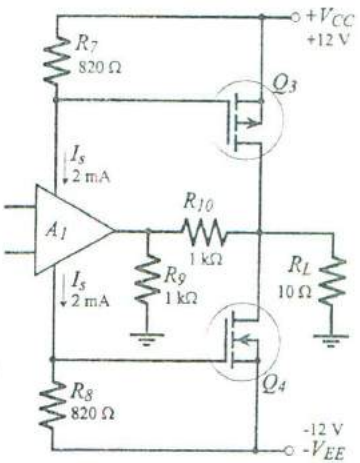


Figure 18-51
Circuit for Example 18-20.

Complete Amplifier Circuit

The complete circuit of the common-source power amplifier is shown in Fig. 18-52. Note the inclusion of resistors R_{11} and R_{12}.

and capacitors C_3 and C_4. Resistors R_{11} and R_{12} are typically 100 Ω. They have no effect on the circuit *dc* conditions, but they help to reduce the possibility of oscillations in the output stage. The additional stage of voltage gain constituted by the *MOSFETs* and the op-amp (common-emitter) output transistors increases the possibility of circuit instability. Capacitor C_3 helps to ensure frequency stability by acting with resistor R_9 to introduce a phase lead in the output stage feedback loop. (see Section 15-2). The phase lead cancels some of the phase lag in the overall circuit.

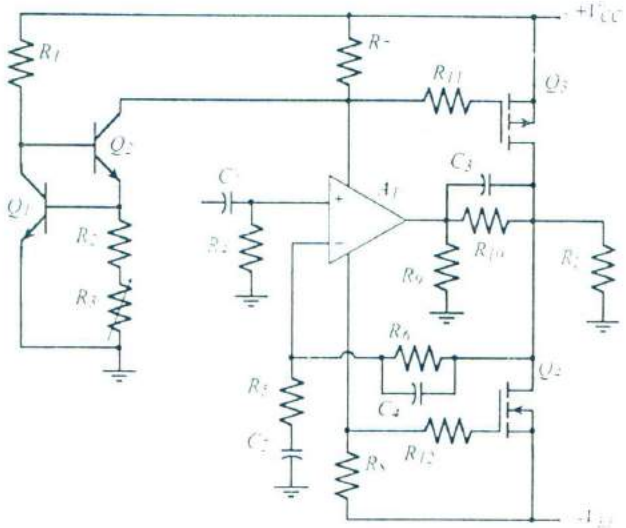


Figure 18-52
Complete circuit of Class-AB common-source power amplifier.

The additional stage of amplification extends the high cut-off frequency of the amplifier above the cut-off frequency of the op-amp operating alone. If the op-amp (full power) upper cutoff frequency for an overall voltage gain of 20 (or 26 dB) is 200 kHz, and the additional stage has a gain of 2 (or 6 dB), the circuit cut-off frequency is 400 kHz. For audio applications, it is normal to include capacitor C_4 (see Fig. 18-52) which is usually selected to set the amplifier upper cutoff frequency around 50 kHz, or lower.

Example 18-21

Analyse the circuit in Fig. 18-53 to determine the op-amp minimum supply voltage ($V_{Sdc(min)}$), and the *MOSFET* maximum gate-source voltage ($V_{GS(on)}$). The op-amp supply current is 0.5 mA.

Solution

$$V_{L_1} = 2\,V_{BE} = 2 \times 0.7\ \text{V}$$
$$= 1.4\ \text{V}$$

From Eq. 18-27, $I_{C2(max)} = \dfrac{V_{BE}}{R_2} = \dfrac{0.7\ \text{V}}{470\ \Omega}$

≈ 1.5 mA

$$I_{C2(min)} = \frac{V_{BE}}{R_2 + R_3} = \frac{0.7\text{ V}}{470\ \Omega + 1\ \text{k}\Omega}$$
$$= 476\ \mu\text{A}$$

Eq. 18-28, $$V_{CS(max)} = [I_{S(max)} + I_{C2(max)}]\, R_7 = (0.5\text{ mA} + 1.5\text{ mA}) \times 1.5\ \text{k}\Omega$$
$$= 3\text{ V}$$

$$V_{S(dc)(min)} = \pm(V_{CC} - V_R) = \pm(15\text{ V} - 3\text{ V})$$
$$= \pm 12\text{ V}$$

Example 18-22

Analyse the circuit in Fig. 18-53 to determine: $P_{o(max)}$, A_{CL}, f_1, f_2. The op-amp supply current is 0.5 mA, and the MOSFETs have $R_{D(on)} = 0.3\ \Omega$.

Solution

Power output:

Eq. 18-31, $$V_p = \frac{V_{CC} \times R_L}{R_{D(on)} + R_L}$$
$$= \frac{15\text{ V} \times 15\ \Omega}{0.3\ \Omega + 15\ \Omega}$$
$$= 14.7\text{ V}$$

$$I_p = \frac{V_p}{R_L} = \frac{14.7\text{ V}}{15\ \Omega}$$
$$= 980\text{ mA}$$

$$P_{o(max)} = \frac{V_p I_p}{2} = \frac{14.7\text{ V} \times 980\text{ mA}}{2}$$
$$= 7.2\text{ W}$$

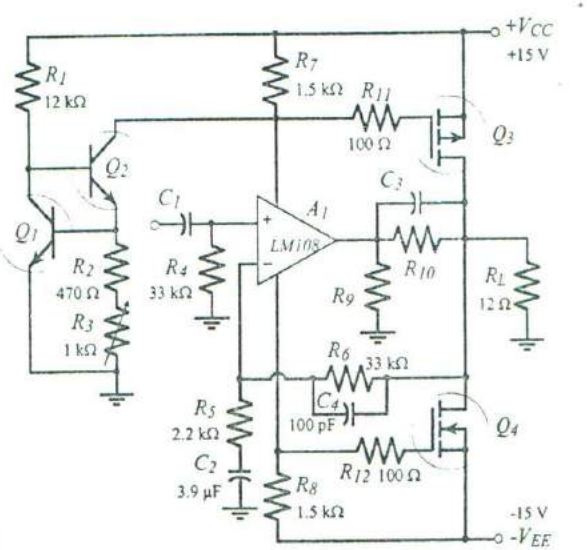


Figure 18-53
Common-source power amplifier circuit for Examples 18-21 and 18-22.

Voltage gain:

$$A_v = \frac{R_5 + R_6}{R_5} = \frac{2.2\ \text{k}\Omega + 33\ \text{k}\Omega}{2.2\ \text{k}\Omega}$$
$$= 16$$

Cut-off frequencies:

$$f_1 = \frac{1}{2\pi C_2 R_5} = \frac{1}{2\pi \times 3.9\ \mu\text{F} \times 2.2\ \text{k}\Omega}$$
$$= 18.5\text{ Hz}$$

$$f_2 = \frac{1}{2\pi C_4 R_6} = \frac{1}{2\pi \times 100\text{ pF} \times 33\ \text{k}\Omega}$$
$$= 48.2\text{ kHz}$$

Practise Problems

18-9.1 A complementary common-source power amplifier is to deliver 5 W to a 12 Ω load. The available *MOSFETs* have $R_{D(on)} = 0.6\,\Omega$, $V_{TH} = 1.2$ V, and $g_{fs} = 3$ S. The op-amp to be used has 1 mA supply currents and maximum output of 20 mA. Design the output stage of the circuit as shown in Fig. 18-51.

18-9.2 Design a *BJT* current source bias control circuit for the amplifier in Problem 18-9.1 to adjust the V_{GS} of Q_3 and Q_4 by ±20%.

18-9.3 The amplifier in Problem 18-9.1 is to have $f_1 = 20$ Hz and $f_2 = 40$ kHz. If the ac input is ±600 mV, determine suitable values for: R_4, R_5, R_6, C_1, C_2, C_4, (see Fig. 18-52). Use a *BIFET* op-amp.

18-10 Integrated Circuit Power Amplifiers

IC Power Amplifier Driver

The *LM391* integrated circuit audio power driver contains amplification and driver stages for controlling an externally-connected Class-AB output stage delivering 10 W to 100 W. The voltage gain and bandwidth are set by additional components. Internal circuitry is included for overload and thermal protection, and for protection of the (externally-connected) amplifier output transistors. The circuit is designed for very low distortion, so that it can be used for high-fidelity amplifiers. Figure 18-54 illustrates the use of the device in an audio amplifier.

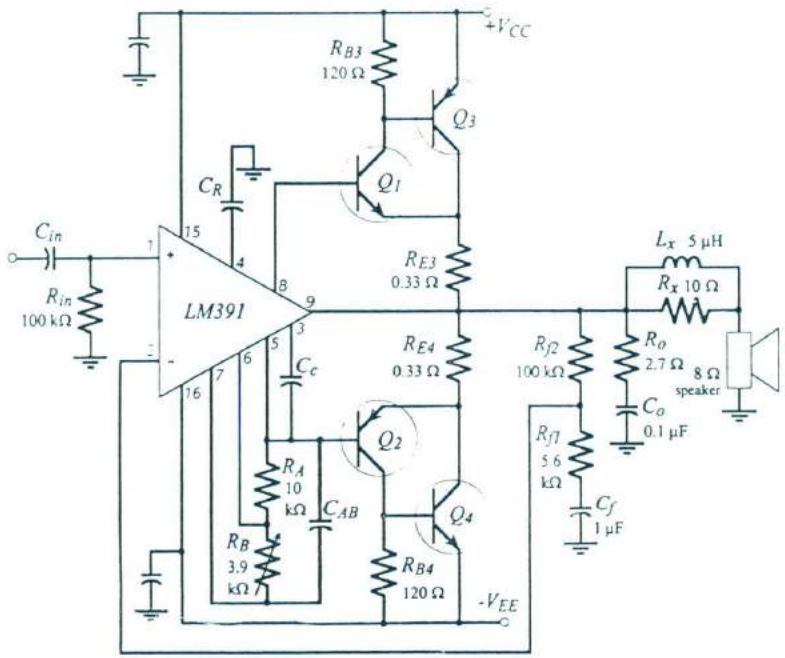
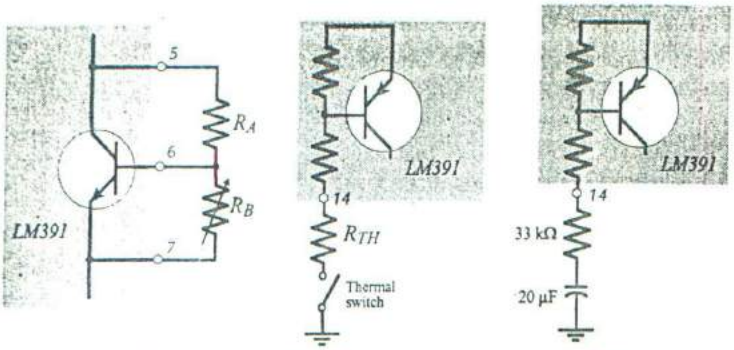


Figure 18-54
Audio power amplifier using an LM391 IC amplifier driver.



(a) V_{BE} multiplier (b) Thermal shut-down (c) Soft turn-on

Figure 18-55
Bias control and shut-down circuits for the LM391.

The output stage in Fig. 18-54 is seen to be a complementary emitter follower with the low power and high power transistor pairs connected in quasi-complementary form. The *IC* output at terminal 9 is connected to the amplifier output, and the output stage transistors are controlled from *current source* terminal 8 and *current sink* terminal 5. The circuit uses a plus-minus supply, and the noninverting input terminal of the *IC* is biased to ground. The inverting input terminal receives feedback from the output, so that the complete circuit operates as a non-inverting amplifier.

Resistors R_A and R_B are connected to an internal transistor (via terminals 5, 6, and 7) to constitute a V_{BE} multiplier for controlling the bias voltage to the amplifier output stage, [see Fig. 18-55(a)]. Capacitor C_{AB} by-passes the V_{BE} multiplier circuit to improve the amplifier high frequency response. Capacitor C_R helps to reject power supply ripple, and C_C is a compensation capacitor for frequency stability. Components R_o, C_o, L_x and R_X are included for load compensation, (see Section 18-5).

The *LM391* has an internal transistor which can shut the circuit down when turned *on* by a thermal switch, [Fig. 18-55(b)]. This allows the device to be protected from overheating that might occur with an excessive load current demand. This same transistor can be employed for *soft turn-on* of the circuit, [Fig. 18-55(c)]. If the amplifier supply voltage is switched *on* at the instant that a peak input signal is applied, a high level output is passed to the speaker, causing a sharp unpleasant noise. Soft turn-*on* causes the output to increase slowly, thus eliminating the speaker noise. The circuit in Fig. 18-55(c) holds the amplifier in a shut-down condition until the capacitor charges.

Overload protection transistors are included in the *LM391*, as shown in Fig. 18-56. These transistors turn *on* when excessive voltage drops occur across the emitter resistors (R_{E3} and R_{E4}) in the output stage, (see Section 18-5).

The output stage components in Fig. 18-54 are selected in the same way as for other direct-coupled Class-*AB* amplifiers. The minimum levels of supply voltage are calculated by adding 5 V to the peak output voltage.

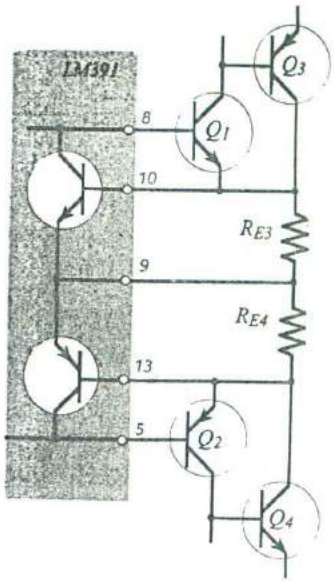


Figure 18-56
Overload protection for the LM391.

$$V_{CC} = \pm(V_P + 5\ V) \qquad (18\text{-}32)$$

The input resistance at terminal 1 of the *LM391* is extremely high, so the circuit input resistance is set by resistor R_{i1}, which is typically selected as 100 kΩ. Feedback resistors R_{f1} and R_{f2} set the amplifier closed-loop voltage gain. The feedback network components are determined in exactly the same way as for other feedback amplifiers. R_{f2} is made equal to R_{i1} to minimize output offset, and R_{f1} is calculated from R_{f2} to give the desired voltage gain. Capacitor C_f is determined in terms of R_{f1} to set low cut-off frequency.

Example 18-23

Determine the maximum output power, the voltage gain, and the low cutoff frequency for the circuit shown in Fig. 18-54.

Solution

from Eq. 18-32, $V_p = V_{CC} - 5\ V = 23\ V - 5\ V$

$= 18\ V$

$$P_o = \frac{V_p^2}{2\,R_L} = \frac{(18\ V)^2}{2 \times 8\ \Omega}$$

$\approx 20\ W$

$$A_{CL} = \frac{R_{f1} + R_{i1}}{R_{f1}} = \frac{100\ k\Omega + 5.6\ k\Omega}{5.6\ k\Omega}$$

$= 18.9$

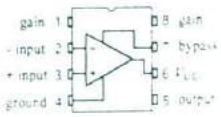
$$f_1 = \frac{1}{2\,\pi\,C_f\,R_{i1}} = \frac{1}{2 \times \pi \times 1\ \mu F \times 5.6\ k\Omega}$$

$= 28\ Hz$

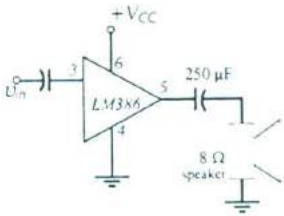
250 mW IC Power Amplifier

The *LM386* is a complete power amplifier circuit capable of delivering 250 mW to an 8 Ω load without any additional components. The supply voltage range is 5 V to 18 V, and the (inverting and non-inverting) input terminals are biased to ground (or to a negative supply) via internal 50 kΩ resistors. The output is automatically centered at half the supply voltage. Feedback resistors are also provided internally to set the voltage gain at 20.

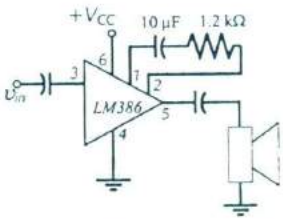
The pin connections for the *LM386* are shown in Fig. 18-57(a), and the circuit connections for functioning as an amplifier with a gain of 20 is illustrated in part (b). Figure 18-57(c) shows how a capacitor and resistor can be connected at pins 1 and 8 to achieve a larger voltage gain. With the 10 μF capacitor alone, a maximum gain of 200 is obtained. The resistor in series with the capacitor allows the voltage gain to be set anywhere between 20 and 200.



(a) *LM386* pin connections



(b) Amplifier with A_{CL} = 20



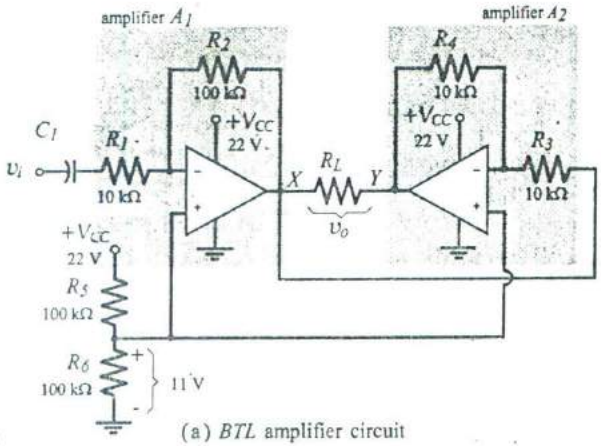
(c) Amplifier with A_{CL} = 50

Figure 18-57
The LM386 IC power amplifier can be connected to have a closed-loop gain from 20 to 200.

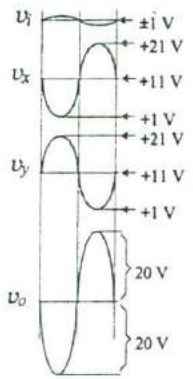
Bridge-Tied Load Amplifier

All of the power amplifiers already discussed have been *single-ended* (*SE*); meaning that they provide power to a load that has one terminal grounded and the other terminal connected to the amplifier output. These amplifiers either use a plus-minus supply with directly-coupled loads, or have a capacitor-coupled load and a single-polarity supply. A *bridge-tied load* (*BTL*) amplifier uses a single-polarity supply and a direct-coupled load.

Figure 18-58(a) shows the basic circuit of a *BTL* amplifier. The two op-amps are connected to function as inverting amplifiers, but note from the resistor values that A_1 has a voltage gain of 10 and that A_2 has a gain of 1. Each amplifier has a single-polarity supply (V_{CC}), and a voltage divider (R_5 and R_6) provides a bias voltage of 0.5 V_{CC} to the op-amp noninverting input terminals. The load resistor (R_L) is connected from the output of A_1 to the output of A_2. This is the *bridge-tied load* configuration.



(a) *BTL* amplifier circuit



(b) Circuit waveforms

Figure 18-58
A bridge-tied load (BTL) amplifier uses two op-amp circuits with their outputs connected to opposite ends of the load.

When no *ac* signal is applied, the *dc* voltage level at the load terminals (*X* and *Y*) is 0.5 V_{CC}; in this case, 11 V for a 22 V supply. As illustrated by the waveforms in Fig. 18-58(b), a +1 V *ac* input to A_1 produces a -10 V change at load terminal *X*. This (-10 V) is also applied to the input of A_2, resulting in a +10 V change at load terminal *Y*. Thus, a peak of 20 V is developed across the load, negative at *X* and positive at *Y*. When the *ac* input goes to -1 V, a 20 V peak load voltage is again produced, but with the load polarity reversed. So, although a single-polarity +22 V supply is used, the output is 40 V peak-to-peak, and no load coupling capacitor is required. A (similar performance) single-ended amplifier producing a 40 V peak-to-peak output would require either a ±22 V supply for a direct-coupled load, or a +44 V supply for a capacitor-coupled load.

Figure 18-59 shows the pin connections and typical application of a *TPA4861*, 1 W integrated circuit *BTL* audio power amplifier. The load is connected across the two output terminals (5 and 8), external resistors R_I and R_F set the voltage gain, and the signal is

coupled to R_l via C_l. The supply voltage (V_{DD}) is internally divided to bias the op-amp noninverting terminals to 0.5 V_{DD}. The bias point is externally accessible so that it can be bypassed to ground (via C_B) for soft start-up and to minimize noise.

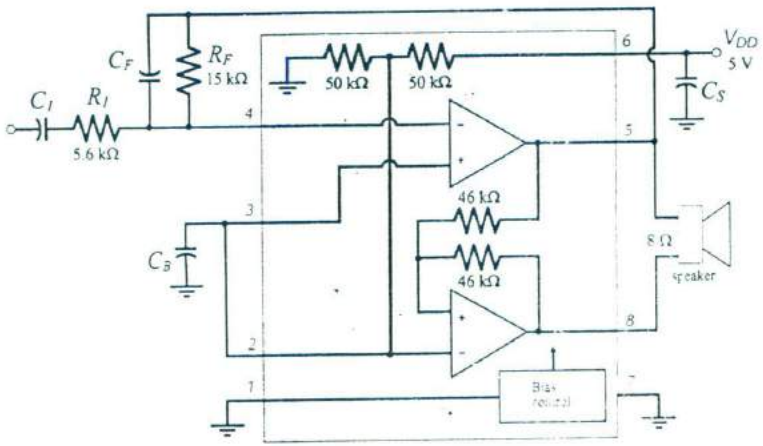


Figure 18-59
TPA4861 bridge-tied load IC amplifier.

A *TPA4861* using a +5 V supply can dissipate 1 W in an 8 Ω load. The overall voltage gain for the (*BTL*) amplifier is twice the gain of the inverting amplifier stage.

$$A_{CL} = \frac{2\,R_F}{R_I} \qquad \textbf{(18-33)}$$

Because the signal is applied to an inverting amplifier, the input resistance is set by resistor R_I. The *IC* manufacturer recommends that R_I should be selected in the range of 5 kΩ to 20 kΩ. Also, if R_F exceeds 50 kΩ, a small capacitor (C_F = 5 pF) should be connected in parallel with it for *ac* stability.

The input capacitor (C_I) sets the circuit low cutoff frequency. So,

$$X_{CI} = R_I \text{ at } f_1 \qquad \textbf{(18-34)}$$

The internal voltage divider resistance (50 kΩ||50 kΩ) is connected in series with the bypass capacitor (C_B). The impedance of C_B should typically be one tenth of the series resistance:

$$X_{CB} = 2.5\ \text{k}\Omega \text{ at } f_1 \qquad \textbf{(18-35)}$$

Example 18-24

Analyse the circuit in Fig. 18-59 to determine the load power dissipation when a ±0.5 V signal is applied at the input.

Solution

Eq. 18-33.
$$A_{cl} = \frac{2R_f}{R_i} = \frac{2 \times 15\ k\Omega}{5.6\ k\Omega}$$
$$\approx 5.4$$

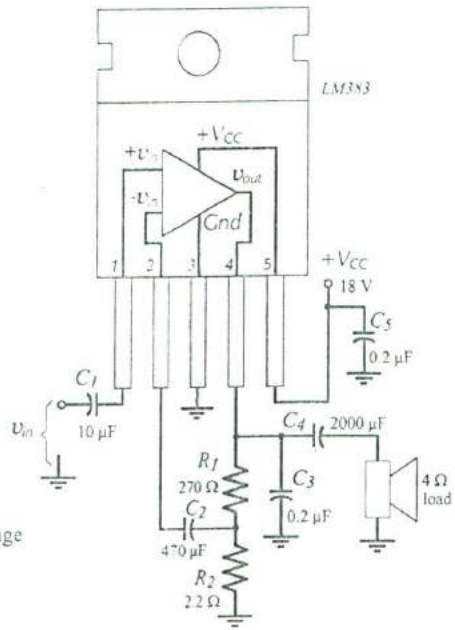
$$V_o = A_{cl} \times v_s = \pm 5.4 \times 0.5\ V$$
$$= \pm 2.7\ V$$

$$P_o = \frac{V_p^2}{2R_L} = \frac{(2.7\ V)^2}{2 \times 8\ \Omega}$$
$$\approx 0.46\ W$$

7 W IC Power Amplifier

The *LM383* can deliver 7 W to a 4 Ω load. No additional output transistors are required because the amplifier can produce a 3.5 A peak output current. Overload protection circuitry is included, and internal bias is provided for the input terminals. The single-polarity supply voltage ranges from 5 V to 20 V. Amplifier voltage gain can be programmed by means of external components. The circuit bandwidth is 30 kHz at a gain of 40 dB.

(a) *LM383* five-lead *TO-220* package



(b) Connection for amplifier with $P_o = 7$ W

Figure 18-60
LM383 IC power amplifier connected to dissipate 7 W in a 4 Ω load.

Figure 18-60 shows an *LM383* (in a 5 pin *TO220* package) connected to function as a (non-inverting) audio amplifier. Capacitors C_1 and C_4 are for coupling the signal and load. Resistors R_1 and R_2 are feedback components that set the circuit

voltage gain, and capacitor C_2 couples the feedback voltage to the inverting input terminal. Other components are for circuit stability. Note that the resistance of R_2 is 2.2 Ω. This is because the inverting input terminal is connected to a transistor emitter terminal (internally) that has an input resistance around 20 Ω. Capacitor C_2 must be very large to couple the feedback voltage to the (low resistance) inverting input. The circuit functions as a noninverting amplifier.

68 W IC Power Amplifier

Figure 18-61(a) shows a power amplifier circuit using an *LM3886* IC audio amplifier. The *LM3886* can deliver 68 W to a 4 Ω load using a ±28 V supply. Alternatively, it can be used to dissipate 38 W in an 8 Ω load, again using a ±28 V supply. The circuit operates as a noninverting amplifier with the closed-loop gain set by resistors R_3 and R_4, and the low cutoff frequency set by capacitor C_1. Potentiometer R_1 allows the signal amplitude to be adjusted. Switch S_1 is a *mute* control.

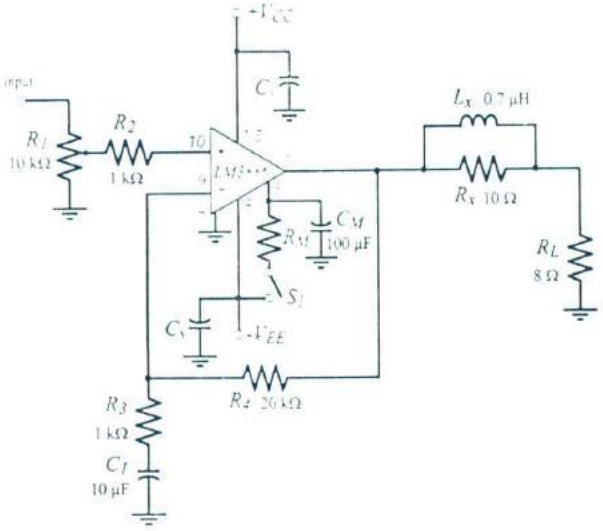


Figure 18-61
LM3886, 68 W audio power amplifier.

Practise Problems

18-10.1 A power amplifier using an *LM391* driver (as in Fig. 18-54) has a ±20 V supply, a 50 Ω load, and power Darlington output *BJTs* with h_{fe} = 600. Calculate the maximum output power, and the peak output current from the integrated circuit.

18-10.2 Calculate the efficiency of the circuit in Fig. 18-59 when delivering 1 W to the speaker. The quiescent current for the *TPA4861* is specified as 2.5 mA.

18-10.3 Determine the signal amplitude for the circuit in Fig. 18-60 to dissipate 7 W in the load. Also, calculate the low cutoff frequency.

Chapter-18 Review Questions

Section 18-1

18-1 Sketch the circuit of a transformer-coupled Class-*A* amplifier. Briefly explain the operation of the circuit.

18-2 Derive the equation for the *ac* load reflected into the primary of the transformer in a Class-*A* amplifier. Also, write the equations for *dc* and *ac* load resistances.

18-3 Sketch approximate I_C/V_{CE} transistor characteristics and an *ac* load line for a Class-*A* amplifier. Draw waveforms to show the transistor output voltage change with change in base current. Briefly explain.

18-4 Write equations for a Class-*A* transformer-coupled amplifier for: *dc* supply power, *ac* power to the transformer primary, and circuit efficiency. Show that the maximum theoretical efficiency of a Class-*A* amplifier is 50%.

Section 18-2

18-5 Sketch the circuit of a transformer-coupled Class-*B* power amplifier output stage. Explain the circuit operation.

18-6 Sketch approximate composite characteristics for a Class-*B* output stage and the *ac* load line. Draw waveforms to show the transistor output voltage change with change in base current. Briefly explain.

18-7 Sketch the circuit of a Class-*AB* transformer-coupled output stage, and explain the difference between Class-*B* and Class-*AB* amplifiers. Also, explain the difference in the performance of the two circuits.

18-8 Draw the complete circuit of a Class-*AB* transformer-coupled amplifier with a Class-*A* driver stage. Explain the operation of the circuit.

18-9 Sketch approximate composite characteristics for a Class-*AB* amplifier and the *ac* load line. Briefly explain.

18-10 Write equations for a Class-*B* transformer-coupled amplifier for: *dc* input power to the output stage, *ac* power delivered to the transformer primary, and circuit efficiency. Show that the maximum theoretical efficiency of a Class-*B* amplifier is 78.6%

Section 18-3

18-11 For a transformer-coupled Class-*B* power amplifier, write equations for the resistance seen when *looking-into* one-half of the center-tapped transformer primary, and the resistance seen when *looking-into* the whole winding of the center-tapped transformer primary.

18-12 For a transformer-coupled Class-*B* power amplifier, write an equation for the power delivered to the transformer

primary in terms of peak primary voltage and reflected load. Also,write an equation for the peak current in terms of primary power and voltage.

18-13 Explain the *safe operating area (SOA)* for the output transistors in a power amplifier.

Section 18-4

18-14 Sketch the circuit of a complementary emitter follower, and explain its operation.

18-15 Sketch the basic circuit of a capacitor-coupled Class-*AB* complementary symmetry amplifier. Explain the *dc* biasing and *ac* operation of the circuit.

18-16 For the amplifier in Question 18-15, write equations for the average supply current to the output stage, the *dc* supply power, and the transistor power dissipation.

18-17 Sketch a direct-coupled Class-*AB* complementary symmetry amplifier. Explain the circuit operation.

Section 18-5

18-18 Sketch the circuit of a Darlington-connected complementary emitter follower output stage for a Class-*AB* power amplifier. Explain the operation of the circuit, and discuss its advantages.

18-19 Sketch the circuit of a quasi-complementary emitter follower output stage. Explain the circuit operation, and discuss its advantages.

18-20 Show how the maximum current can be limited in the output transistors of direct-coupled and capacitor-coupled Class-*AB* power amplifiers. Explain.

18-21 Show how a power amplifier can be protected from the effects of power supply ripple and transients. Explain.

Section 18-6

18-22 Sketch the circuit of a power amplifier with a single *BJT* input stage, an output driver stage, a complementary symmetry Darlington output with a capacitor-coupled load, and overall negative feedback.

18-23 Explain the biasing arrangement for the two amplification stages of the circuit in Question 18-22, and write an equation for the *ac* voltage gain.

18-24 Sketch the circuit of a direct-coupled power amplifier that uses a *npn* transistor differential input stage, a Class-*A* intermediate stage with a constant-current load, and a quasi-complementary emitter follower output stage.

18-25 Explain the *dc* and *ac* operation of the circuit in Question 18-24, and show how a Zener diode may be used to

minimize the effect of ripple voltage on the negative supply line.

Section 18-7

18-26 Compare power *MOSFETs* to power *BJTs*.

18-27 Draw the circuit of a direct-coupled power amplifier with a differential amplifier *BJT* input stage, two *n*-channel *MOSFETs* in the output stage, and overall negative feedback.

18-28 Explain the *dc* and *ac* operation of the circuit in Question 18-27.

18-29 Modify the circuit in Question 18-27 to use complementary *MOSFETs* in the output stage.

Section 18-8

18-30 Draw the circuit of a power amplifier with a direct-coupled complementary symmetry *BJT* output stage, an op-amp driver stage, and overall negative feedback.

18-31 Explain the *dc* and *ac* operation of the circuit in Question 18-30.

18-32 Show how the circuit in Question 18-30 can be modified to use bootstrapping capacitors. Explain the function and advantage of the bootstrap capacitors.

Section 18-9

18-33 Draw the basic circuit of a complementary *MOSFET* common-source power amplifier that uses an op-amp driver with the op-amp supply currents controlling the *MOSFETs*.

18-34 Explain the *dc* and *ac* operation of the circuit in Question 18-33.

18-35 For the circuit in Question 18-33, show how the *MOSFET* bias currents can be controlled by a single variable resistor. Explain.

18-36 Show how a current source can be used to control the *MOSFET* bias currents in the circuit in Question 18-33. Draw the current source circuit and explain its operation.

18-37 Discuss the output voltage swing that can be achieved with the circuit in Question 18-33. Show how the output voltage swing can be made greater than the supply voltage levels at the op-amp terminals.

Section 18-10

18-38 Refer to the *IC* power amplifier circuit in Fig. 18-54. Explain the function of every component in the circuit.

18-39 Draw a circuit diagram to show how the current in the output transistors of a power amplifier can be limited to a

desired maximum level. Explain the circuit operation.

18-40 Sketch the circuit of a bridge-tied load amplifier. Explain the circuit operation and discuss its advantages.

18-41 Explain the function of every component in the *IC* power amplifier circuit in Fig. 18-60.

Chapter-18 Problems

Section 18-1

18-1 A Class-*A* transformer-coupled amplifier, as in Fig. 18-1, has: V_{CC} = 20 V, R_1 = 3.9 kΩ, R_2 = 1 kΩ, R_E = 68 Ω, and R_L = 23 Ω. The transformer has: R_{PY} = 32 Ω, N_1 = 80, and N_2 = 20. Plot the *dc* load line and *ac* load line for this circuit on blank characteristics with vertical axis I_C = (0 to 100 mA) and horizontal axis V_{CE} = (0 to 40 V).

18-2. Assuming an 85% transformer efficiency, calculate the maximum efficiency for the circuit in Problem 18-1.

18-3 A Class-*A* amplifier (as in Fig. 18-1) has the following components: R_1 = 68 kΩ, R_2 = 22 kΩ, R_E = 2.2 kΩ. The supply is V_{CC} = 25 V, and the transformer has: R_L = 5 kΩ, r_L' = 8 kΩ, and R_{PY} = 33 Ω. Plot the *dc* load line and *ac* load line for this circuit on blank characteristics with vertical axis I_C = (0 to 5 mA) and horizontal axis V_{CE} = (0 to 40 V).

18-4 Calculate the maximum peak load voltage for the circuit in Problem 18-3. Assume a 100% transformer efficiency.

Section 18-2

18-5 A class B transformer-coupled output stage, as in Fig. 18-8, has a load resistance R_L = 23 Ω and a supply voltage V_{CC} = 40 V. The transformer has N_1 = 80, N_2 = 20, and a total primary winding resistance R_{PY} = 64 Ω. Using blank characteristics with I_C = (0 to 100 mA) and V_{CE} = (0 to 40 V), plot the complete *ac* load line.

18-6 Determine the maximum output voltage and power for the circuit in Problem 18-5 if the transistors have $V_{CE(sat)} \approx 0$ V.

18-7 A Class-*B* amplifier uses a transformer with 80% efficiency and with N_p/N_s = 5, where N_p is the total number of primary turns on the center-tapped primary. The supply voltage is 45 V, and the load resistance is 8 Ω. Determine the maximum output voltage and power. Assume the transistors have $V_{CE(sat)} \approx 0$ V.

18-8 Using blank composite characteristics with I_C = (0 to 1 A) and V_{CE} = (0 to 45 V), plot the complete *ac* load line for the circuit in Problem 18-7. Assume $R_{pj} << r_L$.

18-9 A Class-*AB* output stage (as in Fig. 18-11) has: V_{CC} = 30 V, R_4 = 6.8 kΩ, R_5 = 220 Ω, $R_6 = R_7$ = 22 Ω. The output

transformer has: $R_L = 24\ \Omega$ and $r_L' = 800\ \Omega$. Assuming a 75% transformer efficiency, calculate the power delivered to the load. Assume Q_2 and Q_3 have $V_{CE(sat)} = 0.5$ V.

18-10 Prepare suitable blank composite characteristics and draw the *ac* load line for the circuit in Problem 18-9.

Section 18-3

18-11 Specify the maximum transistor voltage, current, and power dissipation for the circuit described in Problem 18-7.

18-12 A Class-*A* transformer-coupled amplifier with a 24 V supply is to deliver 1.25 W to a 50 Ω load. Assuming a transformer efficiency of 80%, specify the transformer and transistor.

18-13 Plot *dc* and *ac* load lines (on blank characteristics) for the circuit in Problem 18-12.

18-14 A Class-*B* amplifier is to supply 8 W to a 12 Ω load. The supply is $V_{CC} = 25$ V. Specify the output transformer and transistors. Assume a transformer efficiency of 75%.

18-15 A Class-*AB* transformer-coupled power amplifier (as in Fig. 18-13) is to deliver 0.5 W to a 4 Ω load. The output transformer has $r_L' = 312\ \Omega$ when $R_L = 4\ \Omega$, and has an efficiency of 75%. Calculate a suitable supply voltage and specify the output transistors.

Section 18-4

18-16 A capacitor-coupled power amplifier as in Fig. 18-18 is to deliver 0.6 W to a 250 Ω load. Specify the supply voltage and the output transistors.

18-17 Determine suitable resistor values for the circuit in Problem 18-16. Assume that the output transistors have $h_{FE(min)} = 40$, $h_{ie} = 1\ \text{k}\Omega$, and $h_{ib} = 18\ \Omega$.

18-18 Calculate suitable capacitance values for the circuit in Problems 18-16 and 18-17 for a 50 Hz lower cutoff frequency.

18-19 A direct-coupled amplifier as in Fig. 18-23 is to deliver 2 W to a 20 Ω load. Specify the supply voltage and the output transistors. Assume that the output transistors have $h_{FE(min)} = 200$.

18-20 Determine resistor values for the circuit in Problem 18-19.

Section 18-5

18-21 A power amplifier is required to deliver 5 W to a 20 Ω load. The output stage is to use Darlington-connected *BJT*s and is to be direct-coupled, as in Fig. 18-24. Determine a suitable supply voltage, and specify all the output stage transistors. Assume $h_{FE2} = h_{FE3} = 20$ and $h_{FE4} = h_{FE5} = 100$.

18-22 Determine suitable resistor values for the amplifier output

stage in Problem 18-21.

18-23 A direct-coupled power amplifier using power Darlington *BJTs* with $h_{fe} = 2000$ and $V_{BE} = 1.5$ V is to dissipate 2 W in a 16 Ω load. Determine the required supply voltage and resistor values for the output stage, (see Fig. 18-25).

18-24 Modify the circuit in Problem 18-23 to include current limiting as in Fig. 18-27. The maximum current is to be limited to 20% above the calculated peak level.

18-25 Design a V_{BE} multiplier to replace the diode biasing stage for the output transistors in the circuit for Problem 18-23. Make V_B adjustable by ±20%.

18-26 The driver stage collector resistor (R_C) in the circuit designed for Problem 18-23 is to be replaced by a constant current circuit, as in Fig. 18-30. Design the constant current circuit.

18-27 The amplifier in Problems 18-16 and 18-17 is to be modified to use power supply decoupling as in Fig. 18-29(a). The ripple frequency is 120 Hz. Determine suitable values for R_{15} and C_D, and the new supply voltage level.

Section 18-6

18-28 A direct-coupled amplifier circuit as in Fig. 18-33 is to deliver 7 W to a 22 Ω load. Determine the supply voltage and specify transistors Q_5 through Q_8. Assume $h_{FE5} = h_{FE6} = 90$ and $h_{FE7} = h_{FE8} = 15$.

18-29 Determine suitable values for resistors R_9 through R_{15} for the circuit in Problem 18-30. Also, specify the diodes and transistors Q_3 and Q_4. Assume $I_{CBO} = 10$ μA for Q_7 and Q_8.

18-30 The input voltage to the circuit in Problems 18-28 and 18-29 is ±0.5 V. Determine suitable values for resistors R_1 through R_8.

18-31 The circuit in Problems 18-29 through 18-30 is to have a frequency range from 20 Hz to 50 kHz. Determine suitable capacitances for C_1, C_2, and C_6.

18-32 A direct-coupled amplifier as in Fig. 18-33 has $V_{CC} = \pm 20$ V, $V_{R9} = V_{R11} = 3$ V, and $R_L = 16$ Ω. Calculate the maximum power delivered to the load.

18-33 Specify Q_7 and Q_8 for the circuit in Problem 18-32.

18-34 Calculate the approximate efficiency for the circuit in Problem 18-32.

18-35 A direct-coupled amplifier, as in Fig. 18-33, uses *2N3904* and *2N3906 BJTs* for Q_5 and Q_6. Q_8 is a *2N3055* and Q_7 is complementary to Q_8. The supply voltage is ±25 V and the load resistance is 20 Ω. Determine the maximum output power and calculate the maximum collector current for Q_7 and Q_8, and the maximum base current for Q_5 and Q_6.

Section 18-7

18-36 A *MOSFET* power amplifier circuit as in Fig. 18-36 has V_{CC} = ±30 V and R_L = 50 Ω. Transistors Q_3 and Q_4 have $R_{D(on)}$ = 4 Ω. Determine the maximum power delivered to the load, and the power dissipated in each output transistor.

18-37 A *MOSFET* amplifier circuit as in Fig. 18-36 has a 25 Ω load resistance and uses output transistors with $R_{D(on)}$ = 3 Ω. Calculate the required supply voltage to dissipate 8 W in the load. Also, calculate the power dissipation in the output transistors.

18-38 The MOSFETs in Problem 18-37 have a threshold voltage of V_{TH} = 1.5 V and a transconductance of g_{fs} = 300 mA/V. Determine suitable *dc* voltage drops across resistors R_2 and R_3, and R_6 through R_9.

18-39 Calculate resistor and capacitor values for the circuit in Problems 18-37 and 18-38 if A_{CL} = 15 and f_1 = 80 Hz.

18-40 Calculate the approximate efficiency for the circuit in Problems 18-37 through 18-39.

18-41 Calculate the supply voltage for an amplifier circuit as in Fig. 18-36 to deliver 10 W to a 16 Ω load. The output *MOSFETs* have $R_{D(on)}$ = 1 Ω, V_{TH} = 2 V, and g_m = 2 S.

18-42 Determine suitable *dc* voltage levels for the circuit in Problem 18-41.

18-43 The amplifier in Problems 18-41 and 18-42 has v_{in} = ±0.7 V, and its low cutoff frequency is to be 40 Hz. Calculate all resistor and capacitor values.

Section 18-8

18-44 A direct-coupled Class-*AB* power amplifier using a complementary emitter follower output stage and a operational amplifier driver (as in Fig. 18-39) is to deliver 2.4 W to a 30 Ω load. Calculate the required supply voltage and specify the output transistors in terms of: $V_{CE(max)}$, $I_{C(max)}$, and power dissipation.

18-45 Determine suitable *dc* voltage and current levels for the circuit in Problem 18-44, and calculate all resistor values if v_{in} = ±0.5 V.

18-46 The circuit in Problems 18-44 and 18-45 is to have a frequency range from 30 Hz to 30 kHz. Calculate the capacitor values, and determine the minimum slew rate for the op-amp.

18-47 Modify the circuit in Problems 18-44 through 18-46 to use bootstrapping capacitors, as in Fig. 18-41. Determine suitable values for the bootstrapping capacitors, and calculate the new maximum peak output voltage that can be produced by the modified circuit.

Section 18-9

18-48 The common-source power amplifier circuit in Fig. 18-52 has the following components: $R_7 = R_8 = 680\ \Omega$, $R_9 = R_{10} = 1.2\ k\Omega$, $R_4 = R_6 = 18\ k\Omega$, $R_5 = 820\ \Omega$, $R_L = 32\ \Omega$. The supply voltage is ±30 V, the op-amp supply current is 1 mA, the Q_2 collector current is 1 mA, and the *MOSFETs* have $R_{D(on)} = 1.5\ \Omega$, and $g_m = 1.2$ S. Determine the gate-source bias voltage for Q_3 and Q_4, and the maximum output power.

18-49 Calculate the op-amp supply terminal voltages, and the op-amp peak output voltage for the circuit in Problem 18-48. Also, determine the required signal voltage to give maximum output.

18-50 Design the bias control circuit for the circuit in Problem 18-48 to give $I_{C2} = 1$ mA ±50%.

18-51 A direct-coupled Class-*AB* common-source power amplifier, as in Fig. 18-52 without the current source, is to deliver 8 W to a 12 Ω load. Calculate the required supply voltage if the output transistors have $R_{D(on)} = 0.95\ \Omega$, $V_{th} = 2$ V, and $g_m = 0.9$ S.

18-52 The circuit in Problem 18-51 has $v_{in} = \pm 0.9$ V, and an op-amp with $I_s = 1.3$ mA and $I_{o(max)} = 15$ mA. Determine suitable resistor values.

18-53 The circuit in Problems 18-51 and 18-52 is to have a frequency range from 40 Hz to 45 kHz. Calculate the capacitor values, and determine the minimum slew rate for the op-amp.

Section 18-10

18-54 A direct-coupled Class-*AB* audio power amplifier is to be designed to dissipate 5 W in a 16 Ω load. The circuit is to use quasi-complementary connected output transistors, and a *LM391* driver, as in Fig. 18-54. Calculate the required supply voltage, and specify the *BJTs*. Assume $h_{FE} = 20$ for Q_3 and Q_4.

18-55 Select suitable resistances for R_{E3} and R_{E4} in the circuit for Problem 18-54 to limit the output current to 20% above the required peak level, as illustrated in Fig. 18-56.

18-56 A *TPA4861 BTL* amplifier is to be used to dissipate 1 W in a 15 Ω load. The input voltage is ±0.7 V, and the low cutoff frequency is to be 25 Hz. Calculate the required supply voltage and suitable resistances for R_I and R_F (in Fig. 18-59). Also, determine suitable capacitor values.

Practise Problem Answers

18-1.1 [Q point: $I_C = 3.1$ mA, $V_{CE} = 10.2$ V], [point A: $I_C = 0$, $V_{CE} = 15$ V], [point B: $I_C = 0$, $V_{CE} = 21.1$ V]

18-1.2 25.6%

18-2.1 37.7%

18-2.2 [Q point: $I_C = 4.8$ mA, $V_{CE} = 26.7$ V], [point A and A': $I_C = 24.8$ mA, $V_{CE} = 25.6$ V], [point B and B': $I_C = 46.7$ mA, $V_{CE} = 2.55$ V]

18-3.1 10 V, (20 V, 26 mA, 67.5 mW)

18-3.2 1.09 W, 50 V, 640 mA

18-4.1 21 V, (21 V, 90 mA, 200 mW)

18-4.2 1.8 kΩ, 50 Ω variable

18-5.1 ±16 V, 2.7 kΩ, 100 Ω

18-5.2 15 kΩ, 2.2 kΩ, 2 kΩ

18-5.3 10 kΩ, (56 kΩ + 1.5 kΩ), 1 kΩ, 500 Ω variable

18-6.1 4.7 kΩ, 3.3 kΩ, 4.7 kΩ, 1.2 kΩ, 180 Ω, 4.7 kΩ, 15 μF, 30 μF

18-7.1 18 μF, 22 μF, 0.82 μF

18-7.2 ±15 V, 12 V, 14.3 V, 1.3 V, 10.7 V, 17.7 V, 1.3 V

18-7.3 4.7 kΩ, 12 kΩ, 6.8 kΩ, 120 Ω, 4.7 kΩ, 100 kΩ, 820 kΩ, (1.2 MΩ + 150 kΩ), 100 kΩ, 10 μF, 33 μF, 0.47 μF, 0.47 μF

18-8.1 12.1 V, 146 mW, 6.6 kHz

18-8.2 ±12 V, 3.5 V/μs

18-9.1 1.2 kΩ, 1.2 kΩ, 1.2 kΩ, 1.2 kΩ

18-9.2 5.6 kΩ, 390 Ω, 1 kΩ variable, 560 Ω, 560 Ω

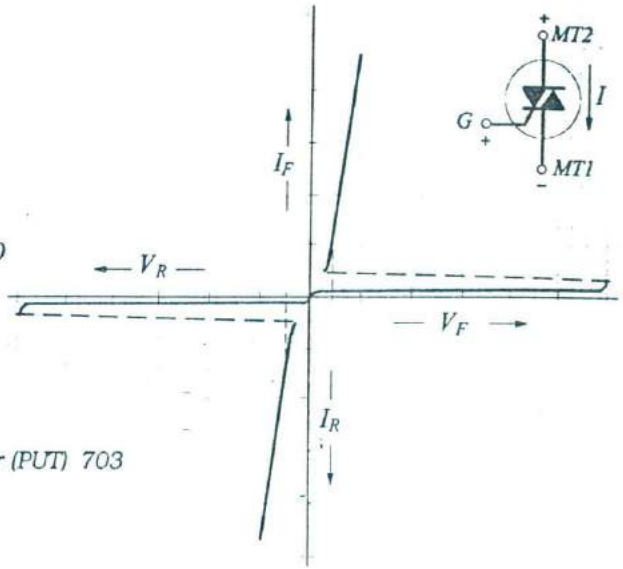
18-9.3 100 kΩ, 5.6 kΩ, 100 kΩ, 0.82 μF, 1.5 μF, 39 pF

18-10.1 2.25 W, 0.5 mA

18-10.2 62.5%

18-10.3 ±60 mV, 19.9 Hz

Chapter 19
Thyristors



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Objectives

You will be able to:

1. *Sketch the basic construction of an SCR and explain its operation. Draw typical SCR characteristics, and define the device parameters.*
2. *Sketch and explain the following SCR circuits: 90° phase control, 180° phase control, zero-point triggering, crowbar, heater control.*
3. *Design and analyze the above types of SCR circuits.*
4. *Sketch the basic construction of a TRIAC and explain its operation. Draw typical TRIAC characteristics, and define the device parameters.*
5. *Discuss TRIAC Quadrant I to IV triggering.*
6. *Sketch and explain TRIAC phase control and zero-point triggering circuits.*
7. *Design and analyze the above types of TRIAC circuits.*
8. *Sketch characteristics and graphic symbols for the following devices: DIAC, SUS, SBS, GTO, SIDAC. Explain the operation and applications for each device.*
9. *Sketch the basic construction of a UJT and explain its operation. Draw typical UJT characteristics, and define the device parameters.*
10. *Sketch the basic construction of a PUT and explain its operation. Draw typical PUT characteristics, and define the device parameters.*
11. *Sketch and explain relaxation oscillators and thyristor control circuit using UJTs and PUTs.*
12. *Design and analyze the above types of UJT and PUT circuits.*

Introduction

The *silicon-controlled rectifier* (*SCR*) can be thought of as an ordinary rectifier with a control element. The current flowing into the control element, which is termed the *gate*, determines the anode-to-cathode voltage at which the device commences to conduct. The *SCR* is widely applied as an *ac* power control device. The gate bias may keep the device *off*, or it may permit conduction to commence at any desired point in the forward half-cycle of a sinusoidal input. Many other devices, such as the *DIAC* and the *TRIAC*, are based on the *SCR* principle. Collectively, *SCR*-type devices are known as thyristors. This term is derived from *thyratron* and transistor, the thyratron being a gas-filled electron tube that behaves like an *SCR*.

The *unijunction transistor* (*UJT*) is a three-terminal device quite different from bipolar and field effect transistors. The device input, called the *emitter*, has a resistance that rapidly decreases when the input voltage reaches a certain level. This effect is termed a *negative resistance* and it makes the *UJT* useful in timing and oscillator circuits. The *programmable unijunction transistor* (*PUT*) is an *SCR*-type device that behaves like a *UJT*.

19-1 Silicon Controlled Rectifier (SCR)

SCR Operation

The *silicon-controlled rectifier* (*SCR*) consists of four layers of semiconductor material, alternately *p*-type and *n*-type as illustrated in Fig. 19-1(a). Because of its construction, the *SCR* is sometimes referred to as a *four-layer* diode, or a *pnpn* device. The layers are designated p_1, n_1, p_2, and n_2, as shown. There are three junctions; J_1, J_2, and J_3, and three terminals; *anode* (*A*), *cathode* (*K*), and *gate* (*G*). Figure 19-1(b) shows the *SCR* circuit symbol.

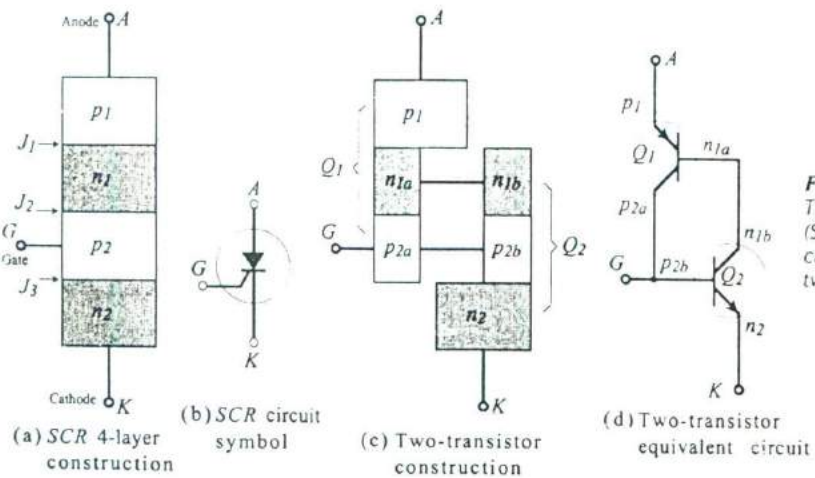
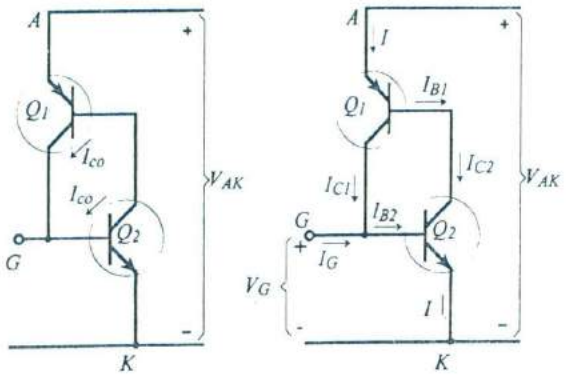


Figure 19-1
The silicon controlled rectifier (SCR) is a four-layer device that can be explained in terms of a two-transistor equivalent circuit.

To understand *SCR* operation, it is necessary to imagine layers n_1 and p_2 split into n_{1a}, n_{1b}, p_{2a} and p_{2b} as shown in Fig. 19-1(c). Since n_{1a} is connected to n_{1b}, and p_{2a} is connected to p_{2b}, nothing is really changed. However, it is now possible to think of p_1, n_{1a}, p_{2a} as a *pnp* transistor, and n_{1b}, p_{2b}, n_2 as an *npn* transistor. Replacing the transistor block representations in Fig. 19-1(c) with the *pnp* and *npn BJT* circuit symbols gives the *two-transistor equivalent circuit* in Fig. 19-1(d). It is seen that the Q_1 collector is connected to the Q_2 base, and the Q_2 collector is commoned with the Q_1 base. The Q_1 emitter is the *SCR* anode terminal, the Q_2 emitter is the cathode, and the junction of the Q_1 collector and the Q_2 base is the *SCR* gate terminal.

To forward bias an *SCR*, a voltage (V_{AK}) is applied positive on the anode (*A*), negative on the cathode (*K*), as shown in Fig. 19-2(a). If the gate (*G*) is left unconnected only small leakage currents (I_{CO}) flow, and both transistors remain *off*. Reference to Fig. 19-1(a) shows that the leakage currents are the result of junction J_2 being reverse biased when *A* is positive and *K* is negative.



(a) Leakage current when the gate is open-circuited

(b) Gate current triggers the *SCR* on

Figure 19-2
When the SCR gate current is zero, the device normally remains off. The flow of gate current (I_G) triggers the SCR on.

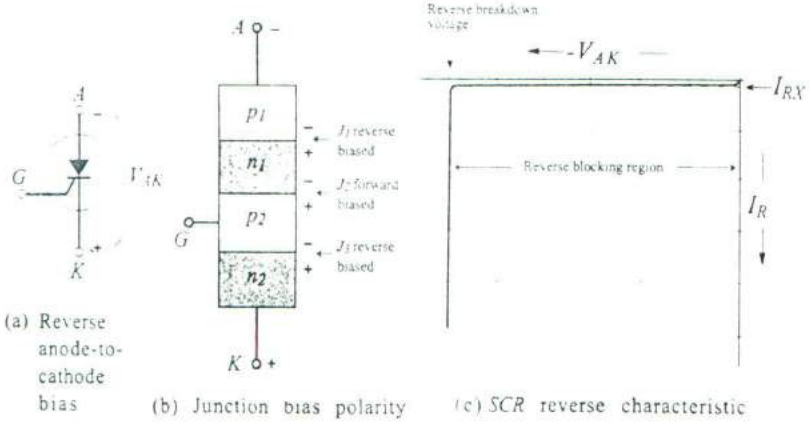
When a negative gate-cathode voltage ($-V_G$) is applied, the Q_2 base-emitter junction is reverse biased, and only small leakage currents continue to flow, so both Q_1 and Q_2 remain *off*. A positive gate-cathode voltage forward biases the Q_2 base-emitter junction, causing a gate current ($I_G = I_{B2}$) to flow, and producing a Q_2 collector current (I_{C2}), [see Fig. 19-2(b)]. Because I_{C2} is the same as I_{B1}, Q_1 also switches *on* and I_{C1} flows providing base current I_{B2}. Each collector current provides much more base current than needed by the transistors, and even when I_G is switched *off*, the transistors remain *on*, conducting heavily with only a small anode-to-cathode voltage drop. The ability of the *SCR* to remain *on* when the triggering current is removed is referred to as *latching*.

To switch the *SCR on*, only a brief pulse of gate current is required. Once switched *on*, the gate has no further control and the device remains *on* until V_{AK} is reduced to near zero.

Consider Fig. 19-1(a) again. With a forward (anode-to-cathode) bias, junctions J_1 and J_3 are forward biased, while J_2 is reverse biased. When V_{AK} is made large enough, J_2 will break down and the resultant current flow across the junction constitutes collector current in each transistor. Each collector current flows into the base of the other transistor causing both transistors to switch *on*. Thus, the *SCR* can be triggered *on* with the gate open-circuited.

SCR Characteristics and Parameters

Figure 19-3(a) shows an *SCR* with a reverse bias anode-to-cathode voltage ($-V_{AK}$), (negative on *A*, positive on *K*). Note that the gate terminal is open-circuited. Figure 19-3(b) shows that the reverse bias voltage causes junction J_2 to be forward biased and J_1 and J_3 to be reverse biased. When $-V_{AK}$ is small, a *reverse leakage current* (I_{RX}) flows. This is plotted as the reverse characteristic ($-V_{AK}$ versus I_R) on Fig. 19-3(c). I_{RX} is typically around 100 μA, and is sometimes referred to as the *reverse blocking current*.



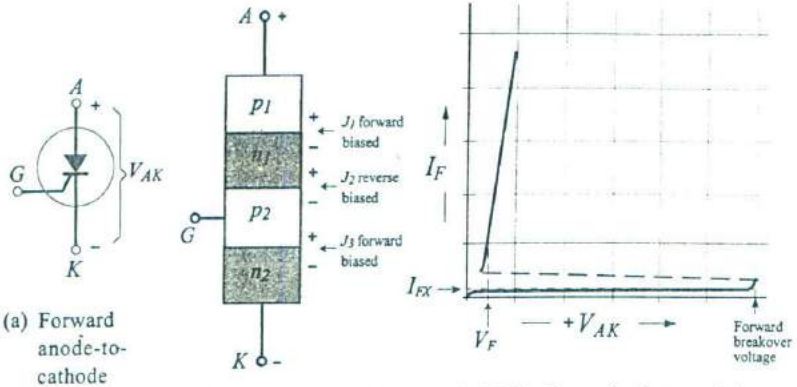
(a) Reverse anode-to-cathode bias (b) Junction bias polarity (c) *SCR* reverse characteristic

Figure 19-3
When V_{AK} is negative, J_2 is forward biased, and J_1 and J_3 are reverse biased. A small reverse leakage current flows while $-V_{AK}$ is less than the breakdown voltage.

When the level of $-V_{AK}$ is increased, I_{RX} remains approximately constant until the reverse breakdown voltage is reached. At this point the reverse-biased junctions (J_1 and J_3) break down and the reverse current (I_R) increases very rapidly. If I_R is not limited (by additional circuit components) the device will be destroyed by excessive current flow. The region of the reverse characteristics before breakdown is termed the *reverse blocking region*.

An *SCR* with a forward bias anode-to-cathode voltage (positive on *A*, negative on *K*) is shown in Fig. 19-4(a). Here again, the gate terminal is open-circuited. As illustrated in Fig. 19-4(b), $+V_{AK}$ forward biases J_1 and J_3 and reverse biases J_2. With low levels of $+V_{AK}$, a small *forward leakage current* (I_{FX}) flows. This is actually the reverse leakage current at junction (J_2), and so (like I_{RX}), it is typically around 100 μA. Also like I_{RX}, I_{FX} remains substantially constant until $+V_{AK}$ is made large enough to cause (reverse biased) J_2 to break down. The applied voltage at this point is termed the forward breakover voltage ($V_{F(BO)}$). This is illustrated by the *forward*

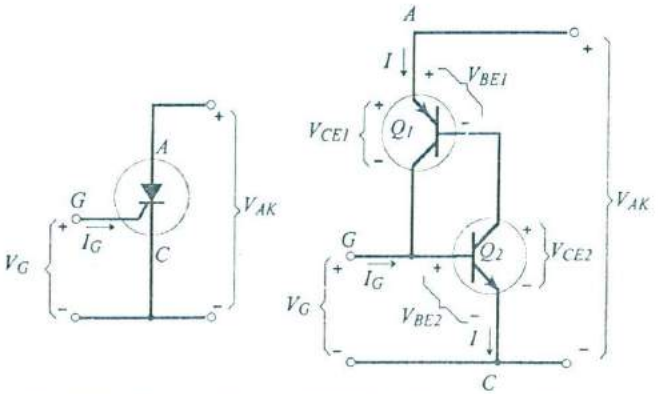
characteristics (I_F versus $+V_{AK}$) in Fig. 19-4(c). When $V_{F(BO)}$ is reached, the component transistors (Q_1 and Q_2) are immediately switched *on* into saturation as already explained, and the anode-to-cathode voltage falls rapidly to the *forward conduction voltage* V_F. The device is now into the *forward conduction region*, and I_F must be limited to protect the *SCR* from excessive current levels.



(a) Forward anode-to-cathode bias (b) Junction bias polarity (c) *SCR* forward characteristic

Figure 19-4
When V_{AK} is Positive, J_2 is reverse biased, and J_1 and J_3 are forward biased. A small forward leakage current flows while $+V_{AK}$ is less than the forward breakover voltage.

So far, the *SCR* forward characteristics have been discussed only for the case of $I_G = 0$. Now consider the effect of I_G levels greater than zero, [Fig. 19-5(a)]. As already shown, when $+V_{AK}$ is less than $V_{F(BO)}$ and I_G is zero, a small leakage current flows. This current is too small to have any effect on the level of $+V_{AK}$ that causes *SCR* switch *on*. When I_G is made just slightly larger than the junction leakage currents, it still has a negligible effect on the level of $+V_{AK}$ for switch-*on*. Now consider the opposite extreme. When I_G is made larger than the minimum base current required to switch Q_2 *on*, the *SCR* switches-*on* when $+V_{AK}$ forward biases the base-emitter junctions of Q_1 and Q_2. [Fig. 19-5(b) and Fig. 19-6].



(a) *SCR* with gate current (b) *SCR* voltage drops when *on*

Figure 19-5
A gate current (I_G) can cause the SCR to switch-on at a low V_{AK} level.

The complete forward characteristics for an *SCR* are shown in Fig. 19-6. Note that when $I_G = I_{G4}$ switch-*on* occurs with $+V_{AK}$ at a relatively low level (V_4). Gate currents between I_{GO} and I_{G4} permit device switch-*on* at voltages greater than V_4 and less than $V_{F(BO)}$. The region of the forward characteristics before switch-*on* occurs is known as the *forward blocking region*, and the region after switch-*on* is termed the *forward conduction region*, as illustrated. In the forward conduction region, the *SCR* behaves as a forward-biased rectifier. The forward (anode-to-cathode) voltage (V_F) when the device is *on* is typically 1.7 V.

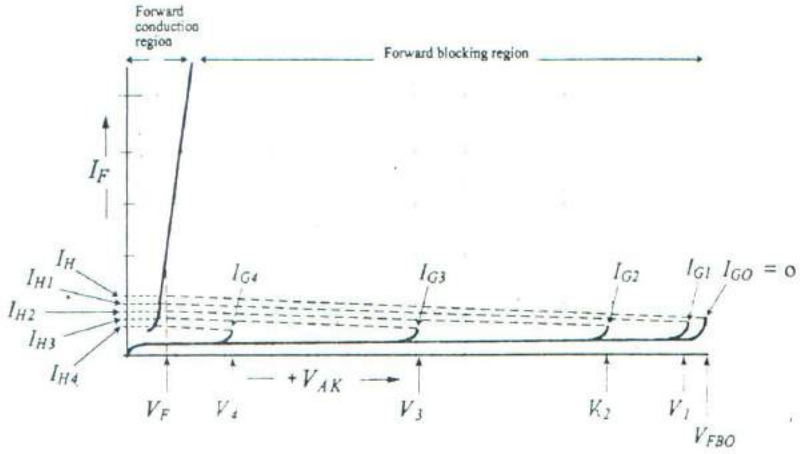


Figure 19-6
Forward characteristics for an SCR. Higher levels of gate current (I_G) cause the SCR to conduct at lower anode-to-cathode voltages ($+V_{AK}$).

To switch an *SCR off*, the forward current (I_F) must be reduced below the *holding current* (I_H), (see Fig. 19-6). The holding current is the minimum level of I_F that maintains *SCR* conduction. If a gate current greater than zero is maintained while the *SCR* is *on*, lower levels of holding current (I_{H1}, I_{H2}, etc.,) are possible.

SCR Specification

As in the case of most electronic devices, the *SCR* maximum voltage and current are important for any given application. The forward breakover voltage and reverse breakdown voltage have already been discussed. The maximum forward voltage that may be applied without causing the *SCR* to conduct is termed the *forward blocking voltage* (V_{DRM}). Similarly, the maximum reverse voltage that may be applied is the *reverse blocking voltage* (V_{RRM}).

The maximum *SCR* current is variously specified as: the *average current* ($I_{T(AV)}$), the *rms current* ($I_{T(RMS)}$), and the *peak non-repetitive surge current* (I_{TSM}). The first two of these need no explanation. The third is a relatively large current that can normally be permitted to flow for a maximum of a half-cycle of a 60 Hz sine wave. The *circuit fusing rating* (I^2t) is another parameter that defines the maximum nonrepetitive forward current. This can be used to calculate the maximum time duration for a given forward current surge. In many circuit applications the *SCR* current is limited by a series-connected load, so there is usually no need to consider surge current levels, except in the case of capacitive loads.

Some of the range of available *SCRs* is illustrated by the partial specifications and packages shown in Fig. 19-7. With 800 mA rms current and 30 V forward and reverse blocking voltage, the *2N5060* is a relatively low-current, low-voltage, device. This is packaged in the typical plastic *TO-92* transistor-type enclosure. Note that the *peak reverse gate voltage* (V_{GRM}) is 5 V. The *2N6396 SCR* is capable of handling a maximum *rms* current of 12 A, and has forward and reverse blocking voltage of 200 V. The package is a *TO-220* plastic enclosure with a metal tab for mounting on a heat sink. For the *C35N*, the peak forward and reverse voltage is 960 V, and maximum *rms* current is 35 A. The device package is designed for bolt-mounting to a heat sink.

	2N5060	2N6396	C35N
Peak forward & reverse voltage (V_{DRM} & V_{RRM})	30 V	200 V	960 V
Maximum rms current ($I_{T(RMS)}$)	0.8 A	12 A	35 A
Forward *on* voltage (V_{TM})	1.7 V	1.7 V	2 V
Holding current (I_H)	5 mA	6 mA	100 mA
Gate trigger current (I_{GT})	200 μA	12 mA	6 mA
Gate trigger voltage (V_{GT})	0.8 V	0.9 V	3 V
Gate reverse voltage (V_{GRM})	5 V	5 V	5 V

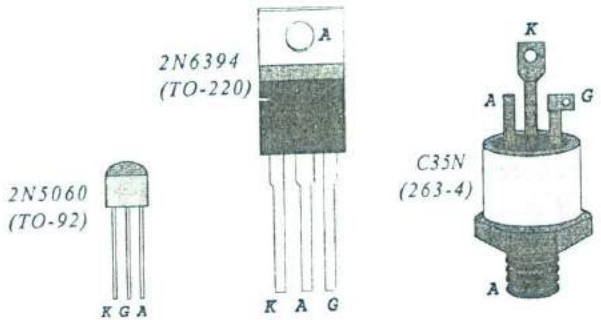


Figure 19-7
Partial specifications and packages for three SCRs for different voltage and current levels.

Section 19-1 Review

19-1.1 Sketch the four-layer construction of an SCR and the two transistor equivalent circuit. Explain the device operation.

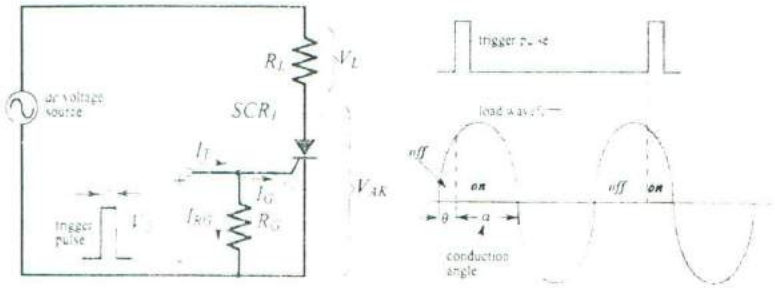
19-1.2 Sketch SCR forward and reverse characteristics. Briefly explain.

19-2 SCR Control Circuits

Pulse Control

The simplest of SCR control circuits is shown in Fig. 19-8(a). If SCR_1 was an ordinary rectifier, the *ac* supply voltage would be half-

wave rectified and only the positive half-cycles would appear across the load (R_L). The same would be true if the *SCR* gate had a continuous bias voltage to keep it *on* when the anode-cathode voltage goes positive. A trigger pulse applied to the gate can switch the device *on* at any time during the positive half-cycle of the supply voltage. The *SCR* continues to conduct during the rest of the positive half-cycle, and then it switches *off* when the instantaneous level of the supply approaches zero. The resultant load waveform is a portion of the positive half-cycle commencing at the instant that the *SCR* is triggered [Fig. 19-8(b)]. Resistor R_G holds the gate-cathode voltage at zero when no trigger input is present.



(a) *SCR* pulse control circuit (b) Circuit waveforms

Figure 19-8
An SCR can be triggered on by a pulse applied to the gate. Once triggered, the device remains on until the load current falls below the holding current.

Load waveforms that result from the *SCR* being switched *on* at different points in the positive half-cycle of the supply voltage are shown in Fig. 19-9. It is seen that the average load current is controlled by the *SCR* conduction angle. Thus, the load power dissipation can be varied by adjusting the *SCR* switch-*on* point. It should be noted that the *SCR* cannot be triggered precisely at the 0° point in the waveform, because the anode-to-cathode voltage must be at lease equal to the forward *on* voltage (V_{TM}) for the device. Also, the *SCR* will switch *off* before the 90° point when the load current falls below the holding current.

The instantaneous level of the load voltage is the instantaneous supply voltage (e_s) minus the *SCR* forward voltage (V_{TM});

$$V_L = e_s - V_{TM} \qquad \textbf{(19-1)}$$

The load current can be calculated from V_L and R_L, and the instantaneous supply voltage ($e_{s(o)}$) that causes the *SCR* to switch *off* can be determined from V_{TM}, R_L, and the holding current;

$$e_{s(o)} = V_{TM} + (I_H \times R_L) \qquad \textbf{(19-2)}$$

For any given application, the selected *SCR* must have forward and reverse blocking voltages greater that the peak supply voltage. Its specified maximum *rms* current must also be greater than the *rms* load current. When designing the circuit, the gate current used should be at least three times the specified I_G for the device.

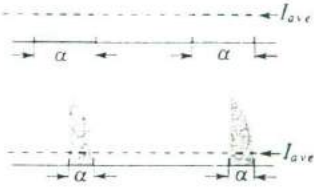


Figure 19-9
The average load current can be varied by controlling the SCR conduction angle.

Note that the required triggering current (I_T) for the circuit in Fig. 19-8 is the sum of I_G and the resistor current I_{RG}, as illustrated.

Example 19-1

Select a suitable *SCR* for the circuit in Fig. 19-8(a), if the *rms* supply voltage is 24 V and the load resistance is 25 Ω. Also, calculate the instantaneous supply voltage that causes the *SCR* to switch *off*.

Solution

peak supply voltage,

$$V_{s(pk)} = 1.414 \times V_s = 1.414 \times 25\ \text{V}$$
$$= 33.9\ \text{V}$$

SCR forward and reverse blocking voltage,

$$V_{DRM}\ \&\ V_{RRM} > 33.9\ \text{V}$$

Referring to the partial specification for the *2N5060* to *2N5064* range of *SCRs* in Fig. 19-10, it is found that the *2N5060* has $V_{DRM} = 30$ V and the *2N5061* has $V_{DRM} = 60$ V. So, the *2N5060* would *not* be suitable, while the *2N5061* would seem to be a suitable device.

$$I_{l(pk)} = \frac{V_{s(pk)} - V_{T(M)}}{R_l} = \frac{33.9\ \text{V} - 1.7\ \text{V}}{25\ \Omega}$$
$$= 1.29\ \text{A}$$

For a half-wave rectified sinusoidal waveform,

$$I_{l(rms)} = 0.5\ I_{l(pk)} = 0.5 \times 1.29\ \text{A}$$
$$= 0.64\ \text{A}$$

The *2N5061* has $I_{T(RMS)} = 0.8$ A.
So, the *2N5061* is a suitable *SCR*.

Switch *off* voltage;

From Eq. 19-2, $e_{s(o)} = V_{TM} + (I_H \times R_l)$
$= 1.7\ \text{V} + (5\ \text{mA} \times 25\ \Omega)$
$\approx 1.8\ \text{V}$

2N5060 to 2N5064		
Peak forward & reverse voltage (V_{DRM} & V_{RRM})	*2N5060*	30 V
	2N5061	60 V
	2N5062	100 V
	2N5063	150 V
	2N5064	200 V
Maximum rms current ($I_{T\,RMS}$)		0.8 A
Forward *on* voltage (V_{TM})		1.7 V
Holding current (I_H)		5 mA
Gate trigger current (I_G)		200 μA

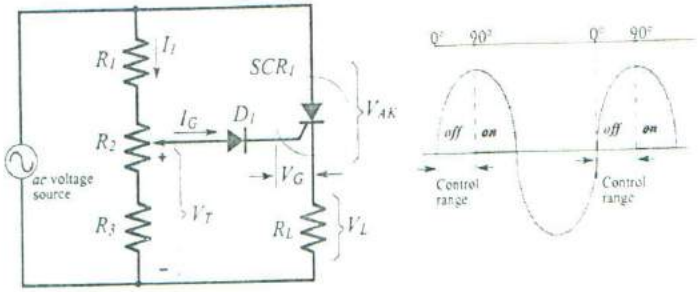
Figure 19-10
Partial specification for 2N5060 to 2N5064 SCRs.

90° Phase Control

In the *90° phase-control circuit* shown in Fig. 19-11, the gate triggering voltage is derived from the *ac* supply via resistors R_1, R_2, and R_3. When the moving contact is set to the top of R_2, the *SCR* can be triggered *on* almost immediately at the commencement of the positive half-cycle of the input. When the moving contact is set to the bottom of R_2, the *SCR* might not switch *on* until the peak of the positive half-cycle. Between these two extremes, the device can be switched *on* somewhere between the zero level and the peak of the positive half-cycle, (between *0°* and *90°*). If the triggering

voltage (V_T) is not large enough to trigger the *SCR* at 90°, then the device will not trigger *on* at all, because V_T is greatest at the supply voltage peak and falls *off* past the peak.

Diode D_1 in Fig. 19-11 is included in the circuit to protect the *SCR* gate from the negative voltage that would otherwise be applied to it during the negative half-cycle of the *ac* supply.



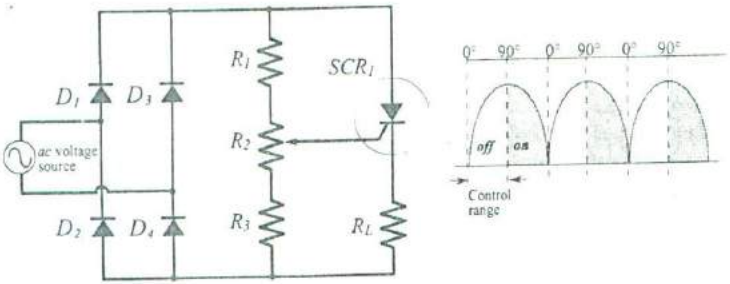
(a) 90° phase control circuit (b) Circuit waveforms

Figure 19-11
SCR 90° phase control circuit. The SCR can be triggered on anywhere between 0° and 90°.

The load for an *SCR* phase control circuit could be a permanent magnet motor, so that the circuit controls the motor speed. Alternatively, the load might be a heater or a light, and in this case the circuit controls the heater temperature or the light intensity.

The voltage divider (R_1 R_2 R_3) in Fig. 19-11 is designed in the usual way for the required range of adjustment of V_T. The voltage divider current (I_1) is selected much larger than the *SCR* gate current. The instantaneous triggering voltage at switch-*on* is,

$$V_T = V_{D1} + V_G \qquad \textbf{(19-3)}$$



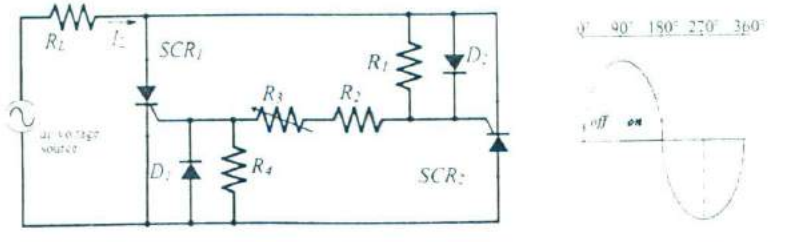
(a) 90° phase control circuit with full wave rectified supply (b) Circuit waveforms

Figure 19-12
SCR 90° phase control circuit with a full wave rectified supply.

Figure 19-12 shows a 90° phase control circuit with its *ac* voltage source full-wave rectified. This gives a larger maximum power dissipation in the load than a non-rectified source. Also, diode D_1 in Fig. 19-11 is not required in Fig. 19-12 because the *SCR* gate does not become reverse biased.

In the circuit in Fig. 19-13(a) the two *SCRs* are connected in inverse-parallel and they operate independently as 90° phase control circuits. SCR_1 controls the load current during the positive half-cycle of the supply voltage, and SCR_2 controls the current during the negative half-cycle. The triggering voltage for each *SCR* is set by the voltage divider network R_1 through R_4 and adjusted by variable resistor R_3. Diodes D_1 and D_2 protect the gate terminals of each *SCR* from excessive reverse voltage.

During the supply voltage positive half-cycle, D_2 is forward biased and current flows through R_2, R_3, and R_4. The voltage drop across R_4, triggers SCR_1 at the desired point in the positive half cycle. When triggered, the *SCR* forward voltage switches to a low level, and remains there until the instantaneous supply voltage level approaches zero. During the supply negative half-cycle, D_1 is forward biased to produce current flow through R_1, R_2, and R_3. With R_1 equal to R_4, the voltage drop across R_1 triggers SCR_2 at the same point in the negative half-cycle as SCR_1 in the positive half-cycle. The resultant 90° full-wave phase controlled load waveform is shown in Fig. 19-13(b).



(a) 90° full-wave phase control circuit (b) load current waveform

Figure 19-13
90° full-wave phase control circuit using two inverse-parallel connected SCRs.

Example 19-2

The *SCR* in Fig. 19-14 is to be triggered *on* between 5° and 90° during the positive half-cycle of the 30 V supply. The gate triggering current and voltage are 200 μA and 0.8 V. Determine suitable resistance values for R_1, R_2, and R_3.

Solution

Peak supply voltage,

$$V_{s(pk)} = 1.414 \times V_s = 1.414 \times 30\ \text{V} = 42.4\ \text{V}$$

at 5°, $e_s = V_{s(pk)} \sin 5° = 42.4\ \text{V} \sin 5° \approx 3.7\ \text{V}$

at 90°, $e_s = V_{s(pk)} = 42.4\ \text{V}$

Eq. 19-3, $V_T = V_{D1} + V_G = 0.7\ \text{V} + 0.8\ \text{V} = 1.5\ \text{V}$

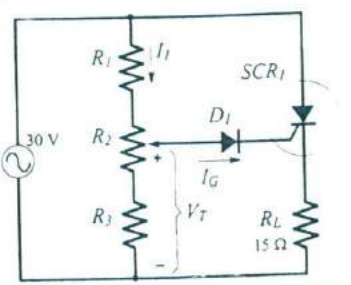


Figure 19-14
SCR 90° phase control circuit for Example 19-2.

To trigger at $e_s = 3.7$ V, the R_2 moving contact is at the top.

so, $V_{R2} + V_{R3} = V_T = 1.5$ V

and, $V_{R1} = e_s - V_T = 3.7\text{ V} - 1.5\text{ V}$
$= 2.2$ V

$I_{T(min)} >> (I_G = 200\,\mu\text{A})$

select $I_{T(min)} = 1$ mA

$$R_1 = \frac{V_{R1}}{I_T} = \frac{2.2\text{ V}}{1\text{ mA}}$$
$$= 2.2\text{ k}\Omega \text{ (standard value)}$$

$$R_2 + R_3 = \frac{V_T}{I_T} = \frac{1.5\text{ V}}{1\text{ mA}}$$
$$= 1.5\text{ k}\Omega$$

To trigger at $e_s = 42.4$ V, the R_2 moving contact is at the bottom.

so, $V_{R3} = V_T = 1.5$ V

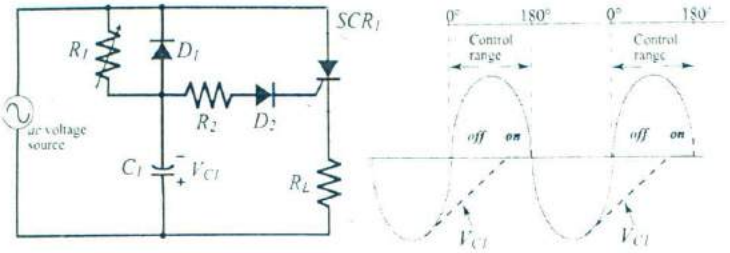
and, $$I_T = \frac{e_s}{R_1 + R_2 + R_3} = \frac{42.4\text{ V}}{2.2\text{ k}\Omega + 1.5\text{ k}\Omega}$$
≈ 11.5 mA

$$R_3 = \frac{V_T}{I_T} = \frac{1.5\text{ V}}{11.5\text{ mA}}$$
$= 130\ \Omega$ (use 120 Ω standard value)

$R_2 = (R_2 + R_3) - R_3 = 1.5\text{ k}\Omega - 120\ \Omega$
$= 1.38$ kΩ (use 1.5 kΩ standard value potentiometer)

180° Phase Control

In the circuit shown in Fig. 19-15, resistor R_1 and capacitor C_1 determine the point in the supply voltage cycle where the *SCR* switches *on*. During the negative half-cycle of the supply, C_1 is charged via diode D_1 to the negative peak of the supply voltage. When the negative peak is passed, D_1 is reverse biased because its anode (connected to C_1) is more negative than its cathode. With D_1 reversed, C_1 commences to discharge via R_1. While C_1 voltage remains negatively, D_2 is reverse biased and the gate voltage cannot go positive to trigger the *SCR on*. Depending on the values of C_1 and R_1, the capacitor might be completely discharged at the beginning of the positive half-cycle of the supply; allowing SCR_1 to switch *on*. Alternatively, C_1 might retain some negative charge past the end of positive half-cycle; keeping SCR_1 *off*. Resistor R_2 is included in the circuit to restrict the level of the gate current.



(a) 180° phase control circuit (b) Circuit waveforms

Figure 19-15
SCR 180° phase control circuit. R_1 adjustment allows the SCR triggering point to be set anywhere between 0° and 180° in the positive half-cycle of the ac supply voltage.

Design of the 180° phase control circuit can commence with selection of a capacitor much larger than stray capacitance. A maximum resistance for R_1 should then be calculated to discharge the capacitor voltage to zero during the time from the negative peak of the supply voltage to the 180° point in the positive half-cycle. The capacitor voltage does not decrease linearly as Fig. 19-16 implies. However, the maximum resistance for R_1 can be most easily calculated by assuming a linear discharge. The average value of the discharging voltage (E) is first determined. Figure 19-16 shows that E is -0.636 $V_{s(pk)}$ for 0.25 T, and +0.636 $V_{s(pk)}$ for 0.5 T, which averages out to approximately 0.2 $V_{s(pk)}$ for the total discharge time of 0.75 T. Now the equation for discharge of a capacitor to zero volts via a resistor may be applied.

$$t = R\,C \ln [(E - E_i)/E]$$

Substituting the appropriate quantities into the equation gives,

$$R_1 \approx \frac{0.75\ T}{C_1 \ln 6} \qquad \textbf{(19-4)}$$

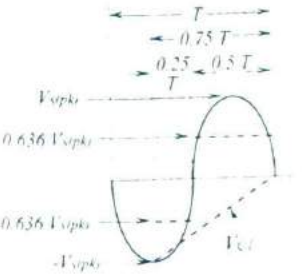


Figure 19-16
Discharge times and voltages for C_1 in the circuit in Fig. 19-15.

Practise Problems

19-2.1 The 90° phase control circuit in Fig. 19-11 has a 115 V, 60 Hz supply, and R_L = 50 Ω. Specify the required *SCR*, and calculate suitable resistor values for switch *on* between 7° and 90°.

19-2.2 The 180° phase control circuit in Fig. 19-15 has a 50 V, 60 Hz supply, and the *SCR* has V_G = 0.5 V and I_G = 100 μA. Determine suitable values for R_1 and C_1. Also, calculate a resistance for R_2 to limit the gate current to a maximum of 50 mA.

19-3 More SCR Applications

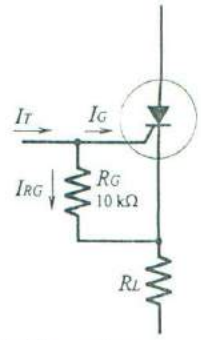
SCR Circuit Stability

An *SCR* circuit is stable when it operates correctly; switching *on* and *off* only at the desired instants. Unwanted triggering (also called *false triggering*) can be produced by noise voltages at the gate, transient voltages at the anode terminal, or by very fast voltages changes at the anode (termed *dv/dt triggering*).

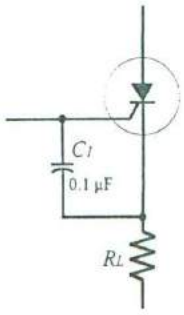
Obviously, gate noise voltages might be large enough to forward bias the gate-cathode junction and cause false triggering. Anode voltage transients (produced by other devices connected to the same *ac* supply) could exceed the *SCR* breakover voltage, and thus trigger it into conduction. The *dv/dt* effect occurs when the anode voltage changes instantaneously, such as when the supply is switched *on* at its peak voltage level. The *SCR* capacitance is charged very quickly, and the charging current is sufficient to trigger the device.

Gate noise problems can be minimized by keeping the gate connecting leads short, and by the use of a gate bias resistor [R_G in Fig. 19-17(a)]. This should be connected as close as possible to the *SCR* gate-cathode terminals, because connecting conductors between R_G and the device could pick up noise that might cause triggering. Biasing the gate negative with respect to the cathode can also be effective in combating noise. Capacitor C_1 in Fig. 19-17(b) can be used to short circuit gate noise voltages. C_1 also operates in conjunction with the anode-gate capacitance as a voltage divider that reduces the possibility of *dv/dt* triggering. C_1 is usually in the 0.01 μF to 0.1 μF range, and like R_G, it should be connected close to the *SCR* terminals.

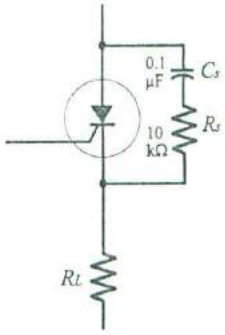
An *RC snubber circuit* can be used to prevent triggering by anode terminal transients, [Fig. 19-17(c)]. A snubber is usually necessary for inductive loads, and might also be required for resistive loads. With an *ac* supply, there is a phase difference between an inductive load current and the supply voltage, and this can cause loss of *SCR* control. Also, the current through an inductor with a *dc* supply will not go to zero immediately when the *SCR* switches *off*. A snubber circuit is necessary in both cases.



(a) Gate resistor



(b) Gate capacitor



(c) Snubber circuit

Figure 19-17
Unwanted gate noise triggering can be prevented by R_G or C_1 at the gate-cathode terminals. The use of a snubber circuit prevents triggering by transients at the anode terminal.

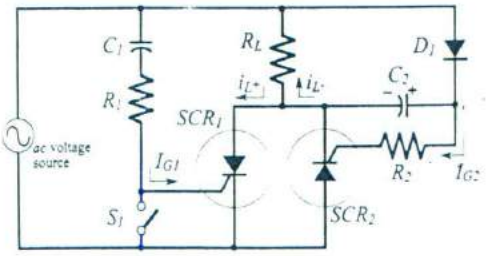
Zero-Point Triggering

When an *SCR* is switched *on* while the instantaneous level of the supply voltage is greater than zero, surge currents occur that generate *electromagnetic interference* (*EMI*). The *EMI* can interfere with other nearby circuits and equipment, and the switching transients can affect control of the *SCR*. Circuits can be designed to trigger an *SCR on* at the instant the *ac* supply is crossing the zero voltage point from the negative half-cycle to the positive half-cycle. This is called *zero-point triggering*, and it effectively eliminates the *EMI* and the switching transients.

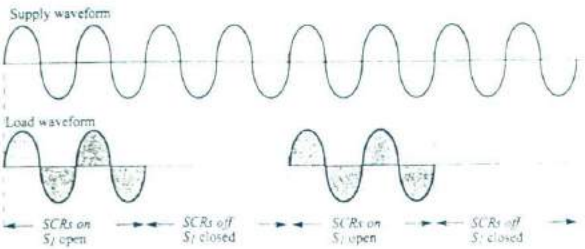
The zero-point triggering circuit in Fig. 19-18(a) shows two inverse-parallel connected *SCRs* that each have *RC* triggering circuits; C_1 and R_1 for SCR_1, and C_2 and R_2 for SCR_2. SCR_1 is held *off* while switch S_1 is closed, and because capacitor C_2 is uncharged SCR_2 remains *off*. With S_1 open, positive triggering current (I_{G1}) begins to flow when the supply voltage commences to go positive. As illustrated, I_{G1} flows via C_1 and R_1 to the gate of SCR_1 triggering it into conduction at the zero-crossing point. SCR_1 provides a path for (*positive*) load current (i_{L+}).

With SCR_1 *on*, capacitor C_2 charges (with the polarity shown) almost to the peak of the supply voltage. When the supply voltage

crosses zero from the positive half-cycle to the negative half-cycle SCR_1 switches *off*. Also, D_1 becomes reverse biased, and the charge on C_1 provides triggering current (I_{G2}) to SCR_2. Thus, SCR_2 is switched *on* at the start of the supply negative half-cycle, providing a path for (*negative*) load current (i_L).



(a) Zero-point triggering circuit



(b) Circuit waveforms

Figure 19-18
In an SCR zero-point triggering circuit the devices are switched on only when the supply waveform crosses the zero-voltage point.

Both *SCRs* continue to switch *on* and *off* at the zero-crossing points while S_1 remains open, and both stay *off* when S_1 is closed. SCR_2 cannot switch *on* unless SCR_1 has first been *on*, and because of this the arrangement is sometimes termed a *master-slave* circuit; SCR_1 being the *master* and SCR_2 the *slave*. The waveforms in Fig. 19-18(b) show that power is supplied to the load for several cycles of the supply while S_1 is open, and no load power dissipation occurs for several cycles while S_1 remains closed. The switch might be controlled by a temperature sensor or other device.

Crowbar Circuit

A *crowbar circuit* (also known as an *overvoltage protection circuit*) is illustrated in Fig. 19-19. This circuit protects a sensitive load against an excessive *dc* supply voltage. When the supply (V_S) is at its normal voltage level, it is too low to cause the Zener diode (D_1) to conduct. Consequently, there is no current through the gate bias resistor (R_1), and no voltage drop across R_1. The gate voltage (V_G) remains equal to zero, and the *SCR* remains *off*. When the supply voltage exceeds V_Z, D_1 conducts, and the resultant voltage drop across R_1 triggers the *SCR* into conduction. The voltage across the load is now reduced to the *SCR* forward voltage drop. The voltage across V_Z and R_1 is also reduced to the *SCR* forward voltage, and the *dc* voltage source is short-circuited by the *SCR*.

The voltage source must have a current limiting circuit to protect the source and to minimize *SCR* power dissipation. The supply must be switched *off* for the SCR to cease conducting.

Example 19-3

The *dc* voltage source in the *SCR* crowbar circuit in Fig. 19-19 has $V_s = 5$ V and $I_{L(max)} = 300$ mA. The load voltage is not to exceed 7 V. Select suitable components for D_1 and R_1, and specify the *SCR*. Assume that $V_G = 0.8$ V.

Solution

$$V_z = V_{L(max)} - V_G = 7\text{ V} - 0.8\text{ V}$$
$$= 6.2\text{ V}$$

For D_1, select a *1N753* with $V_z = 6.2$ V

Select $I_{z(min)} = 1$ mA

$$R_1 = \frac{V_G}{I_z} = \frac{0.8\text{ V}}{1\text{ mA}}$$
$$= 800\ \Omega \text{ (use 820 } \Omega \text{ standard value)}$$

SCR specification:

$$V_{DRM} > 7\text{ V}, I_{T(AV)} > 300\text{ mA}$$

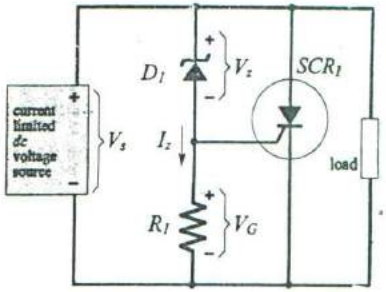


Figure 19-19
An SCR crowbar circuit (or overvoltage protection circuit) short-circuits the load when the supply voltage exceeds a predetermined level.

Heater Control Circuit

The circuit in Fig. 19-20 uses a temperature-sensitive control element (R_2). The resistance of R_2 decreases when the temperature increases, and increases when the temperature falls. Diode D_1 keeps capacitor C_1 charged to the supply voltage peak, and C_1 together with resistor R_1 behaves as a constant current source for R_2. When R_2 is raised to the desired temperature, V_G drops to a level that keeps the *SCR* from triggering. When the temperature drops, the resistance of R_2 increases, causing V_G to increase to the *SCR* triggering level. The result is that the load power is turned *off* when the desired temperature is reached, and turned *on* again when the temperature falls to a predetermined level. Rectifier D_2 might be included, as illustrated, to pass the negative half-cycle of the supply waveform to the load.

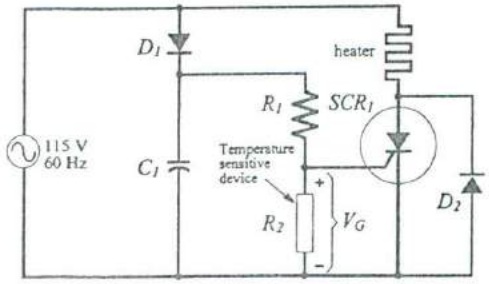


Figure 19-20
SCR heater control circuit. The SCR is triggered on when the temperature is below a specified level, and held off when the temperature is satisfactory.

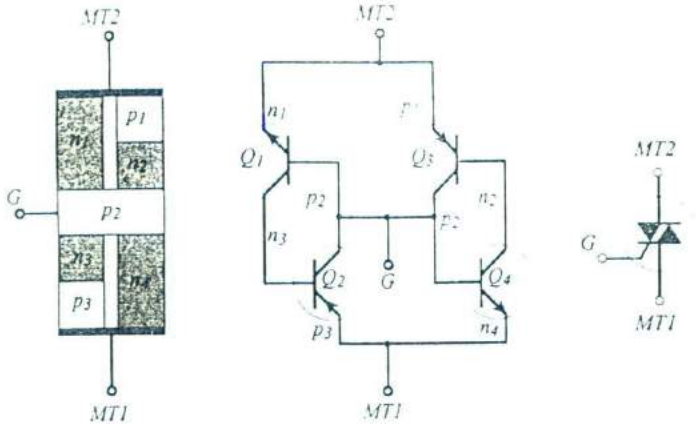
Practise Problems

19-3.1 The *SCR* in the circuit in Fig. 19-20 triggers when V_G is 0.8 V or higher, but will not trigger when V_G is 0.6 V. The temperature sensing element (R_2) has a resistance of 400 Ω at 95°C and 300 Ω at 100°C. Determine suitable values for R_1 and C_1 that will trigger the *SCR* at 95°C and leave it untriggered at 100 °C.

19-4 TRIAC and DIAC

TRIAC Operation and Characteristics

The basic construction, equivalent circuit, and graphic symbol for a *TRIAC* are shown in Fig. 19-21. The *TRIAC* behaves as two inverse-parallel connected *SCRs* with a single gate terminal. Sections n_1, p_2, n_3, and p_3, in Fig. 19-21(a) form one *SCR* that can be represented by transistors Q_1 and Q_2 in Fig. 19-21(b). Similarly, p_1, n_2, p_2, and n_4, form another *SCR* with the transistor equivalent circuit Q_3 and Q_4. Layer p_2, common to the two *SCRs*, functions as a gate for both sections of the device. The two outer terminals cannot be identified as anode and cathode; instead they are designated *main terminal 1 (MT1)* and *main terminal 2 (MT2)*, as illustrated. The *TRIAC* circuit symbol is composed of two inverse-parallel connected *SCR* symbols. [Fig. 19-21(c)].



(a) Basic *TRIAC* construction (b) Equivalent circuit (c) Circuit symbol

Figure 19-21
Basic construction, equivalent circuit, and graphic symbol for a TRIAC.

When *MT2* is positive with respect to *MT1*, transistors Q_3 and Q_4 can be triggered *on* [Fig. 19-21(b)]. In this case current flow is from *MT2* to *MT1*. When *MT1* is positive with respect to *MT2*, Q_1 and Q_2 can be switched *on*. Now current flow is from *MT1* to *MT2*. It is seen that the *TRIAC* can be made to conduct in either direction. Regardless of the *MT2*/*MT1* voltage polarity, the characteristics for the *TRIAC* are those of a forward-biased *SCR*. This is illustrated by the typical *TRIAC* characteristics shown in Fig. 19-22.

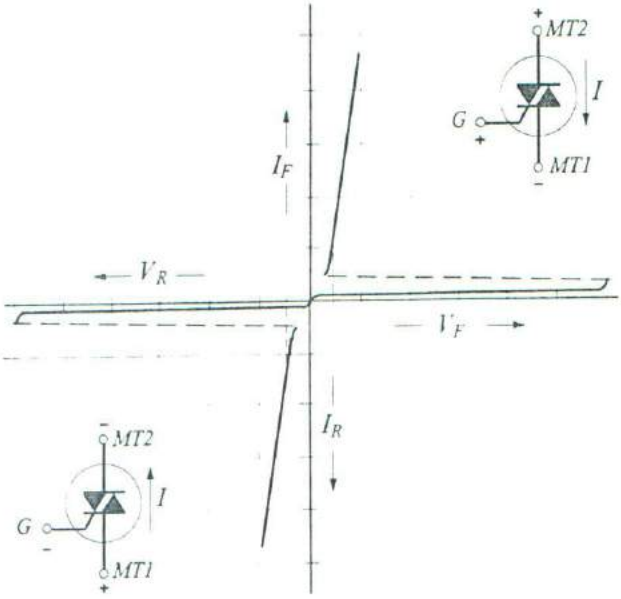


Figure 19-22
TRIAC characteristics. These are similar to the characteristics of two inverse-parallel connected SCRs.

TRIAC Triggering

The characteristics and circuit symbol in Fig. 19-22 show that when *MT2* is positive with respect to *MT1*, the *TRIAC* can be triggered *on* by application of a positive gate voltage. Similarly, when *MT2* is negative with respect to *MT1*, a negative gate voltage triggers the device into conduction. However, a negative gate voltage can also trigger the *TRIAC* when *MT2* is positive, and a positive gate voltage can trigger the device when *MT2* is negative.

Figure 19-23 shows the triggering conditions for a *2N6346*, 8 A, 200 V *TRIAC*. The voltage polarity for *MT2* is identified as *MT2*(+) or *MT2*(-), and the gate polarity is listed as *G*(+) or *G*(-). From the first line of the specifications, it is seen that with *MT2* positive the device gate triggering voltage is +0.9 V minimum and +2 V maximum. From the second line, still with *MT2* positive, triggering can be produced by a negative gate voltage; -0.9 V to -2.5 V. The third line shows *MT2* negative and the gate trigger voltage as -1.1 V to -2 V. Also, with *MT2* negative (fourth line), triggering can be effected by a positive gate voltage; +1.4 V to +2.5 V.

2N6346 TRIAC		
V_{GT}	Min	Max
MT2 (+), G (+)	0.9 V	2 V
MT2 (+), G (-)	0.9 V	2.5 V
MT2 (-), G (-)	1.1 V	2 V
MT2 (-), G (+)	1.4 V	2.5 V

Figure 19-23
Partial specification showing the triggering conditions for a 2N6346 TRIAC.

The *TRIAC* triggering conditions are further illustrated by the diagram in Fig. 19-24. The vertical line identifies *MT2* as positive or negative, and the horizontal line shows the gate voltage as positive or negative. The *TRIAC* is defined as operating in one of the four quadrants: *I*, *II*, *III*, or *IV*. In *quadrant I*, *MT2* is positive, the gate voltage is positive, and current flow is from *MT2* to *MT1*, as shown. When *MT2* is positive and the device is triggered by a negative gate voltage, the *TRIAC* is operating in *quadrant II*. In this case, current flow is still from *MT2* to *MT1*. *Quadrant III* operation occurs when *MT2* is negative and the gate voltage is negative. Current flow is now from *MT1* to *MT2*. In *quadrant IV*, *MT2* is again negative, the gate voltage is positive, and current flow is from *MT1* to *MT2*.

Normally, a *TRIAC* is operated in either *quadrant I* or *quadrant III*. When this is the desired condition, it might be necessary to design the circuit to avoid *quadrant II* or *quadrant IV* triggering.

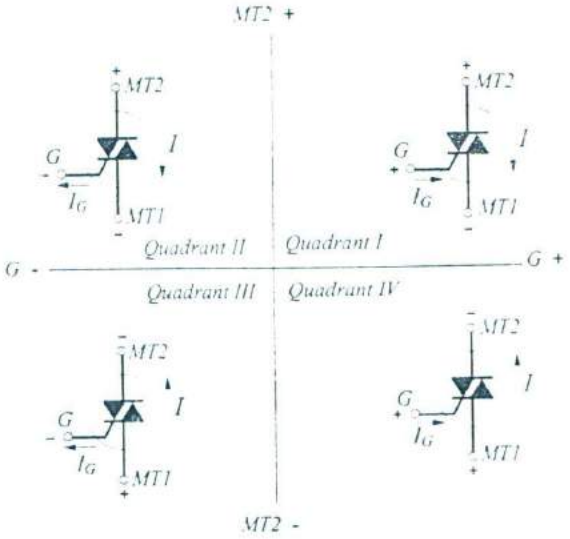
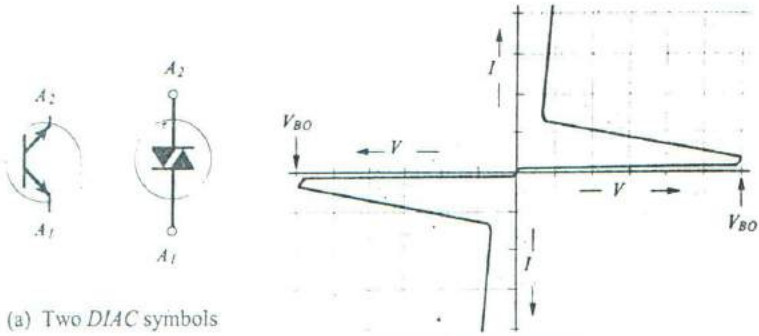


Figure 19-24
Quadrant diagram illustrating the TRIAC four-quadrant operating conditions.

DIAC

A *DIAC* is basically a low-current *TRIAC* without a gate terminal. Switch-*on* is effected by raising the applied voltage to the breakover voltage. Two different *DIAC* symbols in general use are shown in Fig. 19-25(a), and typical *DIAC* characteristics are illustrated in Fig. 19-25(b). Note that the terminals are identified as *anode 2* (A_2) and *anode 1* (A_1). Figure 19-26 shows partial specifications for two *DIACs*. The *HS-10* has a switching voltage that ranges from a minimum of 8 V to a maximum of 12 V. Switching current is a maximum of 400 μA. The *HS-60* switching voltage is 56 V to 70 V, and maximum switching current is 50 μA. Both devices have a 250 mW power dissipation, and each is contained in a cylindrical low-current diode-type package. *DIACs* are most often applied in triggering circuit for *SCRs* and *TRIACs*.



(a) Two *DIAC* symbols

(b) *DIAC* characteristics

Figure 19-25
The DIAC is basically a low-current TRIAC without a gate terminal.

DIACs

	V_S		$I_{S(max)}$	P_D
	Min	Max		
HS-10	8 V	12 V	400 μA	250 mW
HS-60	56 V	70 V	50 μA	250 mW

Figure 19-26
Partial specifications for two DIACs.

Section 19-4 Review

19-4.1 Sketch the construction and transistor equivalent circuit of a *TRIAC*. Explain the device operation.

19-4.2 Sketch *TRIAC* characteristics. Briefly explain.

19-5 TRIAC Control Circuits

TRIAC Phase Control Circuit

A *TRIAC* circuit that allows approximately 180° of phase control is shown in Fig. 19-27(a). The waveforms in Fig. 19-27(b) illustrate the circuit operation. With the *TRIAC* (Q_1) *off* at the beginning of the supply voltage positive half-cycle, capacitor C_1 is charged positively via resistors R_1 and R_2, as shown. When V_{C1} reaches the *DIAC* switching voltage plus the Q_1 gate triggering voltage, D_1 conducts producing gate current to trigger Q_1 *on*. C_1 discharges until the discharge current falls below the D_1 holding current level. The *TRIAC* switches *off* at the end of the supply positive half-cycle, and then the process is repeated during the supply negative half-cycle. The rate of charge of C_1 is set by variable resistor R_1, so that the Q_1 conduction angle is controlled by adjustment of R_1.

Example 19-4

Estimate the smallest conduction angle for Q_1 for the circuit in Fig. 19-27(a). The supply is 115 V, 60 Hz, and the components are: $R_1 = 25\ k\Omega$, $R_2 = 2.7\ k\Omega$, $C_1 = 3\ \mu F$. The D_1 breakover voltage is 8 V, and $V_C = 0.8$ V for Q_1.

Solution

At Q_1 switch-on, $V_{C1} = V_{D1} + V_G = 8\text{ V} - 0.8\text{ V}$

$= 8.8\text{ V}$

Assume the average charging voltage is,

$E = 0.636 \times V_{acpk} = 0.636 \times 1.414 \times 115\text{ V}$

$\approx 103\text{ V}$

Average charging current, $I_C \approx \dfrac{E}{R_1 + R_2} = \dfrac{103\text{ V}}{25\text{ k}\Omega + 2.7\text{ k}\Omega}$

$\approx 3.7\text{ mA}$

Charging time $t \approx \dfrac{C_1 V_{C1}}{I_C} = \dfrac{3\ \mu\text{F} \times 8.8\text{ V}}{3.7\text{ mA}}$

$\approx 7.1\text{ ms}$

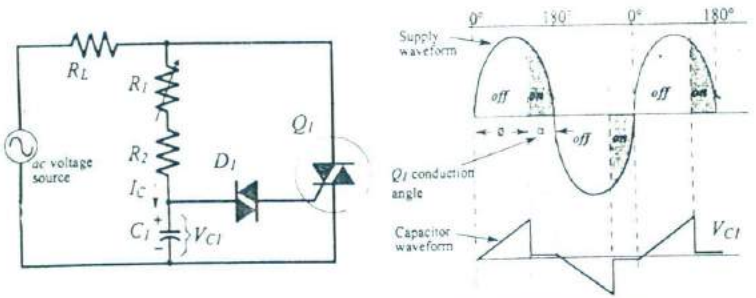
$T = \dfrac{1}{f} = \dfrac{1}{60\text{ Hz}} = 16.7\text{ ms}$

Q_1 switch-on point $\alpha \approx \dfrac{t \times 360}{T} = \dfrac{7.1\text{ ms} \times 360}{16.7\text{ ms}}$

$= 153$

Conduction angle $\alpha = 180 - \alpha = 180 - 153$

$= 27$



(a) Phase control circuit (b) Circuit waveforms

Figure 19-27 *TRIAC phase control circuit and circuit waveforms. Q_1 is switched on when the capacitor charges to D_1 breakover voltage.*

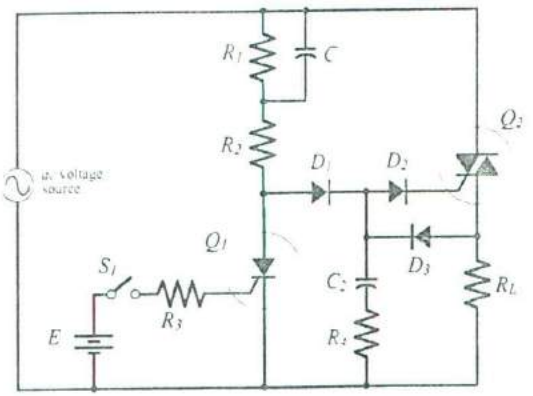
TRIAC Zero-Point Switching Circuit

The *TRIAC zero-point switching circuit* in Fig. 19-28(a) produces a load waveform similar to that for the *SCR* zero-point circuit in Fig. 19-18. The load power dissipation is controlled by switching the *TRIAC on* for several cycles of the supply voltage and *off* for several cycles, with switch-*on* occurring only at the negative-to-positive zero crossing point of the supply waveform, and switch-*off* taking place at the positive-to-negative zero point. Q_1 is a low-current *SCR* that controls the switching point of Q_2.

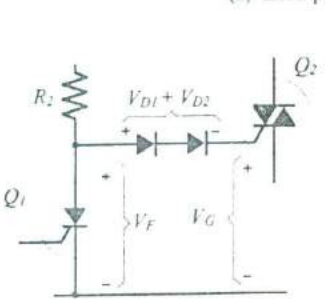
With switch S_1 closed, Q_1 is *on*, and the Q_1 forward voltage drop is below the level required for triggering Q_2, ($V_{G2} + V_{D1} + V_{D2}$). [see Fig. 19-28(b)]. Thus, no gate current flows to Q_2, and no conduction occurs. Q_1 switches *off* when S_1 is opened, so that I_G flows to Q_2 gate via C_1, R_2, D_1, and D_2 to trigger Q_2 into conduction, [Fig. 19-28(c)]. With Q_2 conducting, capacitor C_2 is charged via D_3 almost to the positive peak of the load voltage, [Fig. 19-28(d)]. The *TRIAC* switches *off* at the end of the positive half-cycle. Then, the charge on C_2 (applied to the gate via D_2) triggers Q_2 *on* again just after the zero-crossing point into the negative half-cycle. (It should be noted this is *quadrant IV* triggering.)

The initial Q_2 switch-*on* occurs only at the beginning of the positive half-cycle of the supply voltage. If S_1 is opened during the supply positive half-cycle, Q_1 continues to conduct until the end of the half-cycle, thus keeping Q_2 *off*. With Q_2 *off*, C_2 remains uncharged, and so it cannot trigger Q_2 *on* during the supply negative half-cycle. Q_2 triggering now occurs at the beginning of the next positive cycle.

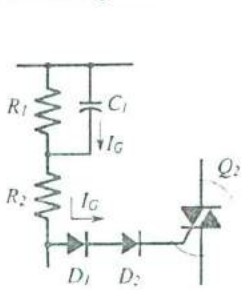
If S_1 is opened during the supply negative half-cycle, Q_2 cannot be triggered into conduction, again because of the lack of charge on C_2. It is seen that Q_2 conduction can commence only at the beginning of the positive half-cycle of the supply voltage. Also, once triggered, Q_2 conduction continues until the end of the cycle.



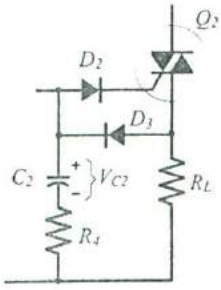
(a) Zero-point switching circuit



(b) With Q_1 *on* Q_2 is held *off*



(c) I_{G2} flows when Q_1 is off



(d) V_{C2} triggers Q_2

Figure 19-28
Zero-point switching circuit for a TRIAC. While Q_1 is on, Q_2 cannot switch on. With Q_1 off, Q_2 commences to conduct at the beginning of the supply positive half-cycle.

To design the circuit in Fig. 19-28, the *TRIAC* is first selected to pass the required load current and to survive the peak supply voltage. Resistor R_2 is a low-resistance component calculated to limit the peak surge current to the Q_2 gate in the event that the peak supply voltage is applied to the circuit without Q_1 being *on*. Capacitor C_1 has to supply triggering current (I_G) to Q_2 at the zero crossing point of the supply waveform when Q_1 is *off*. Usually I_{G2} is selected around three times the specified $I_{G(max)}$ for Q_2, and C_1 is then calculated from the simple equation for capacitor charge: $C = (I \times t)/\Delta V$. In this case $\Delta V/t$ can be replaced by the rate-of-change of the supply voltage at the zero crossing point, which is $(2\pi f V_p)$. So, the C_1 equation is,

$$C_1 = \frac{I_{G2}}{2\pi f V_p} \qquad (19\text{-}5)$$

Resistor R_1 can now be determined by using the selected gate current for Q_2 (I_{G2}) as the peak anode current for Q_1: $R_1 = V_p/I_{G2}$. The Q_1 gate resistor (R_3) is calculated from the Q_1 triggering current and the voltage of the *dc* source: $R_3 = (E - V_{G1})/I_{G1}$.

The Q_2 gate current is again used in the calculation of R_4 and C_2. To trigger Q_2 at the start of the supply negative half-cycle, I_{G2} must flow from C_2 into the Q_2 gate, so $R_4 = V_p/I_{G2}$. A suitable capacitance for C_2 is now calculated by again using the simple capacitance equation $C_2 = (I_{G2} \times t)/\Delta V$. In this case, time t is selected much larger than the Q_2 turn-on time, and ΔV is approximately 0.1 V_p.

SCR Q_1 must pass the selected anode current (I_{G2}) and survive the peak supply voltage. The diodes must each survive the peak supply voltage and pass the Q_2 triggering current.

IC Zero Voltage Switch

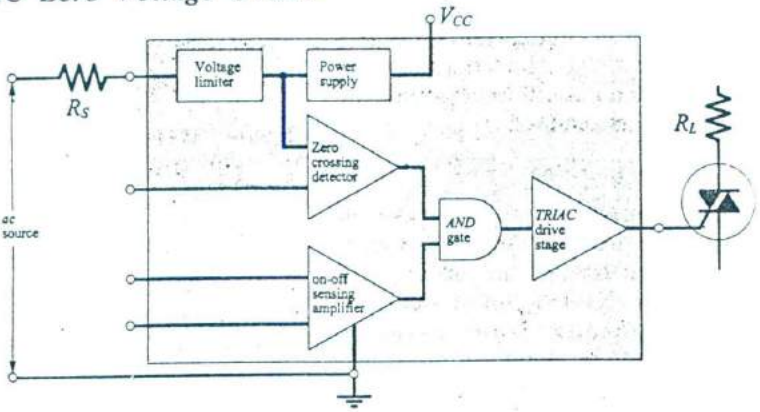


Figure 19-29
Functional block diagram for an integrated circuit zero voltage switch, or TRIAC driver.

The functional block diagram for a typical integrated circuit *TRIAC* driver, known as a *zero voltage switch*, is shown in Fig. 19-29. The device contains a *voltage limiter* and a *dc power supply*, so that it operates directly from the *ac* supply to the load to be controlled. There is also a *zero crossing detector* (see Section 14-9) that

provides an output pulse each time the supply waveform crosses the zero level. The zero crossing detector output is fed to an *AND gate* (see Section 3-11), and the *AND* gate output goes to the *TRIAC drive* stage that produces the current pulse to the *TRIAC* gate. An *on-off sensing amplifier* is used to sense the voltage level from an externally-connected transducer; for example, a temperature sensing transducer would be used if the load is a heater. When the temperature drops to a predetermined level, the on-off sensing amplifier provides an input to the *AND* gate. The gate triggering pulse from the *TRIAC* drive stage occurs at the supply zero-crossing points only when the temperature is below the desired level. The circuit load waveforms are similar to those shown in Fig. 19-18.

Practise Problems

19-5.1 Determine suitable components for the *TRIAC* zero-point switching circuit in Fig. 19-28, given the following: (for Q_1: I_G = 200 μA, V_f = 2 V), (for Q_2: I_G = 30 mA, I_{GM} = 1 A, t_{on} = 100 μs), E = 6 V, ac source = 115 V, 60 Hz.

19-6 SUS, SBS, GTO, and SIDAC

SUS

The *silicon unilateral switch* (*SUS*), also known as a *four layer diode* and as a *Schokley diode*, can be treated as a low-current *SCR* without a gate terminal. Figure 19-30 shows the *SUS* circuit symbol and typical forward characteristics. The device triggers into conduction when a *forward switching voltage* (V_S) is applied. At this point a minimum *switching current* (I_S) must flow. Also, the voltage falls to a *forward conduction voltage* (V_F) at switch *on*, and conduction continues until the current level falls below the *holding current* (I_H). The *2N4988 SUS* has V_S ranging from 7.5 V to 9 V, I_S = 150 μA, and I_H = 0.5 mA. *SUS* reverse characteristics are similar to *SCR* reverse characteristics; a very small reverse current flows until the reverse breakdown voltage is reached.

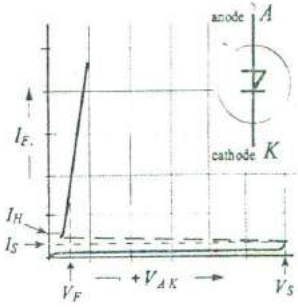


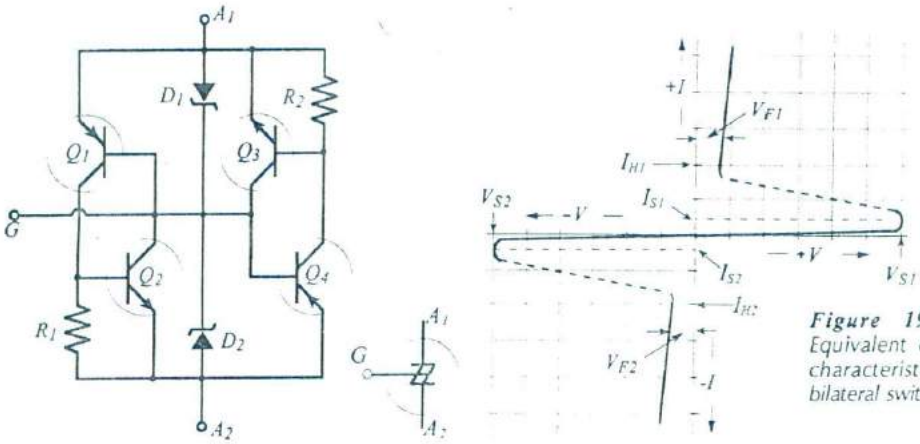
Figure 19-30
SUS circuit symbol and forward characteristics.

SBS

It might be convenient to think of a *silicon bilateral switch* (*SBS*) as an *SUS* with a gate terminal, or as a low-current *TRIAC*. However, the *SBS* is not simply another four-layer device. Silicon bilateral switches are actually integrated circuits constructed of matched transistors, diodes, and resistors. This produces better parameter stability than is possible with four-layer devices. The *SBS* equivalent circuit in Fig. 19-31(a) is similar to the *TRIAC* equivalent circuit with the addition of resistors R_1 and R_2 and Zener diodes D_1 and D_2. The device circuit symbol in Fig. 19-31(b) is seen to be composed of inverse-parallel connected *SUS* symbols with a gate terminal added. Note that the terminals are identified as *anode 1* (A_1), *anode 2* (A_2), and *gate* (*G*). The typical *SBS* characteristics shown in Fig. 19-31(c) are essentially the same

shape as *TRIAC* characteristics.

Returning to the equivalent circuit, the *SBS* switches *on* when a positive A_1A_2 voltage is large enough to cause D_2 to break down. This produces base current in Q_1, resulting in Q_1 collector current that switches Q_2 *on*. Similarly, a negative A_1A_2 voltage causes D_1 to break down, producing base current in Q_4 that turns Q_4 and Q_3 *on*. The switching voltage is the sum of the Zener diode voltage and the transistor base-emitter voltage, ($V_S = V_Z + V_{BE}$). The Zener diode has a positive *temperature coefficient* (*TC*) and the transistor base-emitter voltage has a negative *TC*. This results in a very small *TC* for the *SBS* switching voltage.



(a) Equivalent circuit (b) Symbol (c) Characteristics

Figure 19-31
Equivalent circuit, symbol and characteristics for the silicon bilateral switch (SBS).

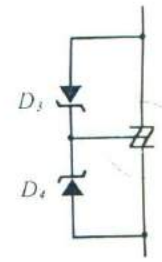
The partial specification for a *MBS4991 SBS* in Fig. 19-32 shows a switching voltage that ranges from 6 V to 10 V. Note also that the *switching voltage differential* (the difference between the switching voltages in opposite directions), (V_{S1} - V_{S2}), is 0.5 V maximum. The maximum switching current is a 500 µA, and the *switching current differential* (I_{S1} - I_{S2}) is 100 µA.

MBS4991 SBS

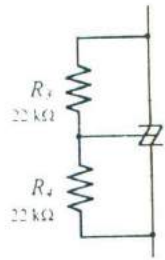
	Min	Typ	Max
Switching voltage (V_S)	6 V	8 V	10 V
Switching current (I_S)		175 µA	500 µA
Switching voltage differential		0.3 V	0.5 V
Switching current differential			100 µA
Gate trigger current (I_{GF})			100 µA
Forward on voltage (V_F)		1.4 V	1.7 V

Figure 19-32
Partial specification for the MBS4991 silicon bilateral switch.

SBS devices are frequently used with the gate open-circuited, so that they simply breakdown to the forward voltage drop when the applied voltage increases to the switching voltage level. The switching voltage can be reduced by connecting Zener diodes with V_Z lower than 6.8 V between the gate and the anodes, as shown in Fig. 19-33(a). The new switching voltage is approximately (V_Z + 0.7 V). The switching voltage can also be modified by the use of external resistors, [Fig. 19-33(b)]. Taking the gate current into account, it can be shown that the two 22 kΩ resistors reduce V_S to approximately 3.6 V.



(a) V_S modification by external Zeners



(b) V_S modification by external resistors

Figure 19-33
The switching voltage for an SBS can be modified by externally-connected Zener diodes or resistors.

The use of an *SBS* in a *TRIAC* phase control circuit is illustrated in Fig. 19-34. This is essentially the same as the circuit using a *DIAC* in Fig. 19-27. The *SBS* turns *on* and triggers the *TRIAC* when the capacitor voltage equals the *SBS* switching voltage plus the *TRIAC* gate triggering voltage.

For an *SBS* to switch *on*, the total resistance in series with it must have a maximum value that allows the switching current to flow. If the resistance is so large that it restricts the current to a level below the *SBS* switching current, the device will not switch *on*. Also, the series resistance must not be so small that it allows the holding current to flow when the *SBS* is supposed to switch *off*. These restrictions also apply to *SCRs*, *TRIACS*, *DIACS*, and other similar switching devices. Switch-*off* is usually no problem in thyristor circuits with *ac* supplies, because the devices normally switch *off* when the instantaneous supply voltage reduces to zero. With *dc* supplies, more care must be taken with resistor sizes.

Figure 19-35 shows a simple circuit that requires careful design to ensure that the *SBS* switches *on* and *off* as required. The circuit is a *relaxation oscillator* that produces an exponential output waveform, as illustrated. Capacitor C_1 is charged via resistor R_1 from the *dc* supply voltage (E). When the capacitor voltage (V_C) reaches the *SBS* switching voltage (V_S), D_1 switches *on* and rapidly discharges the capacitor to the D_1 forward voltage (V_F). Then D_1 switches *off*, and the capacitor commences to charge again. The *SBS* will not switch *off* if the D_1 holding current (I_H) continues to flow through R_1 when V_C equals V_F. *SBS* switch-*on* will normally occur when V_C equals V_S regardless of the R_1 resistance, because the capacitor discharge should provide the switching current (I_S). However, it is best to select R_1 small enough to allow I_S to flow at D_1 switch *on*.

The approximate oscillation frequency can be determined from the capacitor charging time (t), and the equation for t is derived from the *RC* charging equation.

$$t = CR\ ln[\frac{E - V_F}{E - V_S}] \qquad (19\text{-}6)$$

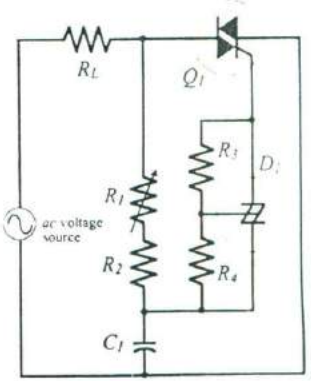


Figure 19-34
Use of an SBS in a TRIAC phase control circuit. The TRIAC is triggered by the current surge when the SBS switches on.

Example 19-5

The *SBS* in the circuit in Fig. 19-35 has the following parameters: V_S = 10 V, V_f = 1.7 V, I_S = 500 μA, I_H = 1.5 mA. Calculate the maximum and minimum

resistances for R_1 for correct circuit operation when $E = 30$ V. Also, determine the capacitor charging time when $R_1 = 27$ kΩ and $C_1 = 0.5$ μF.

Solution

$$R_{1(max)} = \frac{E - V_S}{I_S} = \frac{30\text{ V} - 10\text{ V}}{500\ \mu\text{A}}$$

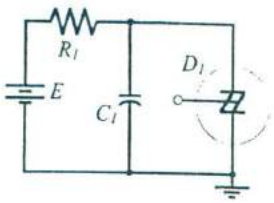
$$= 40\ \text{k}\Omega$$

$$R_{1(min)} = \frac{E - V_F}{I_H} = \frac{30\text{ V} - 1.7\text{ V}}{1.5\text{ mA}}$$

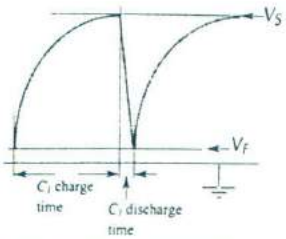
$$= 18.9\ \text{k}\Omega$$

Eq. 19-6, $$t = CR\ ln[\frac{E - V_F}{E - V_S}] = 0.5\ \mu\text{F} \times 27\ \text{k}\Omega\ \ ln[\frac{30\text{ V} - 1.7\text{ V}}{30\text{ V} - 10\text{ V}}]$$

$$= 4.7\ \text{ms}$$



(a) Relaxation oscillator circuit

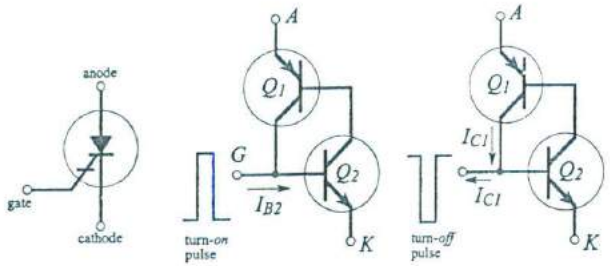


(b) Circuit waveforms

Figure 19-35
SBS relaxation oscillator. C_1 charges via R_1 to the SBS switching voltage. D_1 switches on at that point and rapidly discharges C_1.

GTO

When an *SCR* is triggered into conduction by application of a gate current, the gate looses control and the device continues to conduct until the forward current falls below the holding current. A *gate turn-off* (*GTO*) device is essentially an *SCR* designed to be switched *on* and *off* by an applied gate signal. The circuit symbol for a *GTO* is shown in Fig. 19-36(a), and the two-transistor equivalent circuit for the device is illustrated in Fig. 19-36(b) and (c). Note that at switch-*on*, the gate current has just got to be large enough to supply base current to transistor Q_2. However, at switch-*off*, the Q_1 collector current has to be diverted through the gate terminal in order to turn Q_2 off. Consequently, for device turn-*off* relative large levels of gate current are involved; approaching half the *GTO* forward current.



(a) Symbol (b) Switch-*on* (c) Switch-*off*

Figure 19-36
The gate turn-off device GTO i effectively an SCR that can b switched off by a voltage applie to the gate.

SIDAC

The *SIDAC* is a two-terminal thyristor designed mainly for use in over-voltage protection situations. As a bilateral device with no gate terminal, it simply breaks down to its forward voltage drop when the applied terminal voltage (of either polarity) rises to the breakover voltage level. Like other thyristors, there is a minimum current that must flow to latch the *SIDAC* into an *on* state. Also,

when switched *on* conduction continues until the current falls below a holding current level.

The circuit symbol and typical characteristics for a *SIDAC* are shown in Fig. 19-37. Available devices have breakover voltages ranging from 110 V to 280 V. Typically *on* state voltages is 1.1 V, *rms* current is 1 A, and holding current is 100 mA.

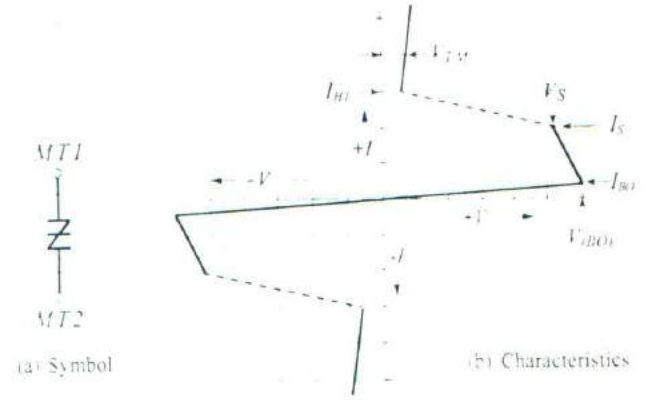


Figure 19-37
Circuit symbol and characteristics for a SIDAC.

Figure 19-38 shows a *SIDAC* used to protect a *dc* power supply from *ac* line transients. Normally, the *SIDAC* will behave as an open-circuit. A voltage transient on the *ac* line will cause it to break down to its forward voltage level, so that it essentially short-circuits the transformer output. This will cause a fuse to blow or a circuit breaker to trip, thus interrupting the *ac* supply.

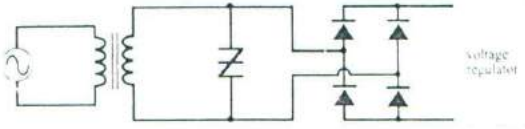


Figure 19-38
SIDAC used for protecting a dc power supply against transients on the supply line.

Practise Problems

19-6.1 The *SBS* in the circuit in Fig. 19-34 has $V_S \approx 4$ V, $I_S = 500\,\mu$A, and $I_{F(max)} = 200$ mA. The *ac* supply is 115 V, and $R_3 = R_4 = 22$ kΩ. Determine suitable resistances for R_1 and R_2.

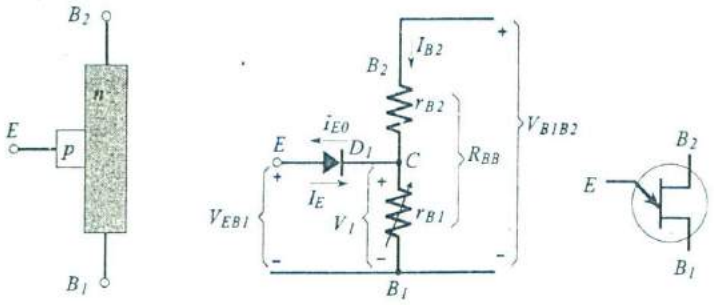
19-7 UJT and PUT

UJT Operation

The *Unijunction transistor* (*UJT*) consists of a bar of lightly-doped *n*-type silicon with a block of *p*-type material on one side, [see Fig. 19-39(a)].The end terminals of the bar are identified as *Base 1* (B_1) and *Base 2* (B_2), and the *p*-type block is named the *emitter* (*E*).

Figure 19-39(b) shows the *UJT* equivalent circuit. The resistance of the *n*-type silicon bar is represented as two resistors, r_{B1} from B_1

to *point C*, and r_{B2} from B_2 to C, as illustrated. The sum of r_{B1} and and r_{B2} is identified as R_{BB}. The *p*-type emitter forms a *pn*-junction with the *n*-type silicon bar, and this junction is shown as a diode (D_1) in the equivalent circuit.



(a) Basic construction (b) Equivalent circuit (c) Circuit symbol

Figure 19-39
A unijunction transistor (UJT) is made up of a p-type emitter joined to a bar of n-type semiconductor.

With a voltage V_{B1B2} applied as illustrated, the voltage at the junction r_{B1} and r_{B2} is,

$$V_1 = V_{B1B2} \times \frac{r_{B1}}{R_{BB}}$$

Note that V_1 is also the voltage at the cathode of the diode; *point C* in the equivalent circuit.

With the emitter terminal open-circuited, the resistor current is,

$$\boldsymbol{I_{B2} = \frac{V_{B1B2}}{R_{BB}}} \qquad \textbf{(19-7)}$$

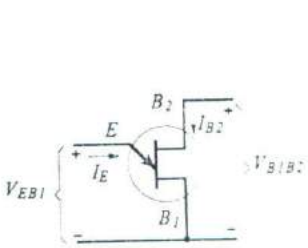
If the emitter terminal is grounded, the pn-junction is *reverse* biased and a small *emitter reverse current* (I_{E0}) flows.

Now consider what happens when the emitter voltage (V_{EB1}) is slowly increased from zero. When V_{EB1} equals V_1 the emitter current is zero. (With equal voltage levels on each side of the diode, neither reverse nor forward current flows.) A further increase in V_{EB1} forward biases the *pn*-junction and causes a forward current (I_E) to flow from the *p*-type emitter into the *n*-type silicon bar. When this occurs, charge carriers are injected into the r_{B1} region. The resistance of the semiconductor material is dependent on doping, so the additional charge carriers cause the resistance of the r_{B1} region to rapidly decrease. The decrease in resistance reduces the voltage drop across r_{B1}, and so the *pn*-junction is more heavily forward biased. This in turn results in a greater emitter current, and more charge carriers that further reduce the resistance of the r_{B1} region. (The process is termed *regenerative*.) The input voltage is *pulled down*, and the emitter current (I_E) is increased to a limit determined by the V_{EB1} source resistance. The device remains in this *on* condition until the emitter input is open-circuited, or until I_E is reduced to a very low level.

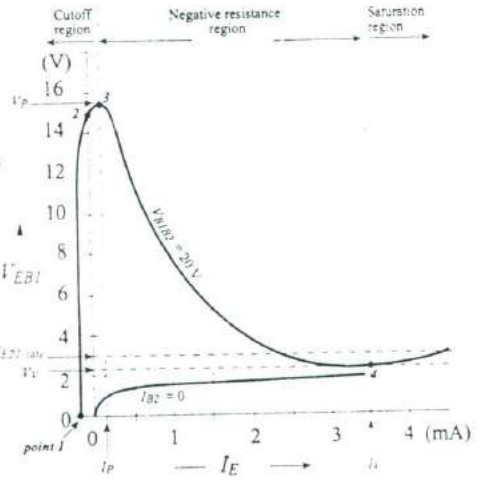
The circuit symbol for a *UJT* is shown in Fig. 19-39(c). As always, the arrowhead points in the conventional current direction for a forward-biased junction. In this case it points from the *p*-type emitter to the *n*-type bar.

UJT Characteristics

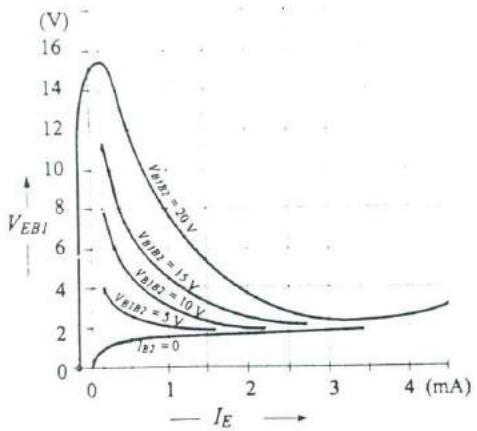
A plot of emitter voltage V_{EB1} versus emitter current I_E gives the *UJT* emitter characteristics. Refer to the *UJT* terminal voltages and currents identified in Fig. 19-40(a) and to the equivalent circuit in Fig. 19-39(b). Note that when $V_{B1B2} = 0$, $I_{B2} = 0$ and $V_i = 0$. If V_{EB1} is now increased from zero, the resultant plot of V_{EB1} and I_E is simply the characteristic of a forward-biased diode with some series resistance. This is the characteristic for $I_{B2} = 0$ in Fig. 19-40(b).



(a) *UJT* voltages and currents



(b) Characteristics for $I_B = 0$ and $V_{B1B2} = 20$ V



(c) Family of *UJT* characteristics

Figure 19-40
The UJT characteristics show that the device triggers on at various levels of emitter voltage V_{EB1} depending upon the level of supply voltage V_{B1B2}.

When V_{B1B2} is 20 V the level of V_1 [Fig. 19-39(b)] might be around 15 V, depending on the resistances of r_{B1} and r_{B2}. With V_{B1B2} = 20 V and V_E = 0, the emitter junction is reverse biased and the emitter reverse current I_{E0} flows, as shown at *point 1* on the V_{B1B2} = 20 V characteristic in Fig. 19-40(b). Increasing the level of V_{EB1} until it equals V_1 gives I_E = 0; *point 2* on the characteristic. Further increase in V_{EB1} forward biases the emitter junction, and this gives the *peak point* on the characteristic (*point 3*). At the peak point, V_{EB1} is identified as the *peak voltage* (V_P) and I_E is termed the *peak current* (I_P).

Up until the peak point the *UJT* is said to be operating in the *cutoff region* of its characteristics. When V_{EB1} arrives at the peak voltage, charges carriers are injected from the emitter to decrease the resistance of r_{B1}, as already explained. The device enters the *negative resistance region*, r_{B1} falls rapidly to a *saturation resistance* (r_S), and V_{EB1} falls to the *valley voltage* (V_V). [*point 4* on the characteristic in Fig. 19-40(b)]. I_E also increases to the *valley current* (I_V) at this time. Further increase in I_E causes the device to enter the *saturation region* where V_E equals the sum of V_D and $I_E r_S$.

Starting with V_{B1B2} lower than 20 V gives a lower peak point voltage and a different characteristic. Thus, using various levels of V_{B1B2}, a family of V_{EB1}/I_E characteristics can be plotted for a given *UJT*, as shown in Fig. 19-40(c).

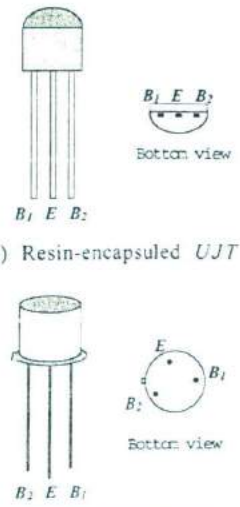


Figure 19-41
UJT packages and terminals.

UJT Packages

Two typical *UJT* packages with the terminal identified are shown in Fig 19-41. These are similar to low-power *BJT* packages.

UJT Parameters

Interbase Resistance **(R_{BB})**: This is the sum of r_{B1} and r_{B2} when I_E is zero. Consider Fig. 19-42 that shows a portion of the manufacturer's data sheet for *2N4949 UJT*. R_{BB} is specified as 7 kΩ typical, 4 kΩ minimum, and 12 kΩ maximum. The value of R_{BB}, together with the maximum power dissipation P_D, determine the maximum value of V_{B1B2} that may be used. With I_E = 0,

$$V_{B1B2(max)} = \sqrt{(R_{BB} P_D)} \qquad \textbf{(19-8)}$$

Like all other devices, the P_D of the *UJT* must be derated for increased temperature levels.

2N4949 UJT

	Min	Typ	Max
Interbase resistance (R_{BB})	4 kΩ	7 kΩ	12 kΩ
Intrinsic standoff ratio (η)	0.74		0.86
Emitter saturation voltage ($V_{EB1(sat)}$)		2.5 V	3 V
Peak point current (I_P)		0.6 μA	1 μA
Valley point current (I_V)	2 mA	4 mA	

Figure 19-42
Partial specification for a 2N4949 UJT.

Example 19-6

A *UJT* has $R_{BB(min)} = 4\ k\Omega$, $P_D = 360$ mW at 25 °C, and a power derating factor $D = 2.4$ mW/°C. Calculate the maximum V_{B1B2} that should be used at a temperature of 100 °C.

Solution

Eq. 8-20, $P_{D(100°)} = P_{D(25°)} - [D\,(T_J - 25°)]$
$= 360\ mA - [2.4\ mW/°C\,(100° - 25°)]$
$= 180$ mW

Eq. 19-8, $V_{B1B2(max)} = \sqrt{(R_{BB} P_D)} = \sqrt{(4\ k\Omega \times 180\ mW)}$
$= 26.8$ V

Intrinsic Standoff Ratio (η): The *intrinsic standoff ratio* is simply the ratio of r_{B1} to R_{BB}. The peak point voltage is determined from η, the supply voltage, and the diode voltage drop:

$$V_p = V_D + \eta V_{B1B2} \qquad (19\text{-}9)$$

Emitter Saturation Voltage ($V_{EB1(sat)}$). The emitter voltage when the *UJT* is operating in the saturation region of its characteristics; the minimum V_{EB1} level. Because it is affected by the emitter current and the supply voltage, $V_{EB1(sat)}$ is specified for given I_E and V_{B1B2} levels.

Example 19-7

Determine the maximum and minimum triggering voltages for a *2N4949 UJT* with $V_{B1B2} = 25$ V.

Solution

From Fig. 19-42, $\eta = 0.74$ minimum, 0.86 maximum

Eq. 19-9, $V_{p(max)} = V_D + (\eta_{max} V_{B1B2}) = 0.7\ V + (0.86 \times 25\ V)$
$= 22.2$ V

$V_{p(min)} = V_D + (\eta_{min} V_{B1B2}) = 0.7\ V + (0.74 \times 25\ V)$
$= 19.2$ V

Peak Point Emitter Current (I_P): I_P is important as a lower limit to the emitter current. If the emitter voltage source resistance is so high that I_E is not greater than I_P the *UJT* will simply not trigger *on*. The maximum emitter voltage source resistance is,

$$R_{E(max)} = \frac{V_{B1B2} - V_P}{I_P} \qquad (19\text{-}10)$$

Valley Point Current (I_V): I_V is important in some circuits as an upper limit to the emitter current. If the emitter voltage source resistance is so low that I_E is equal to or greater than I_V the *UJT* will remain *on* once it is triggered; it will not switch *off*. So, the minimum emitter voltage source resistance is,

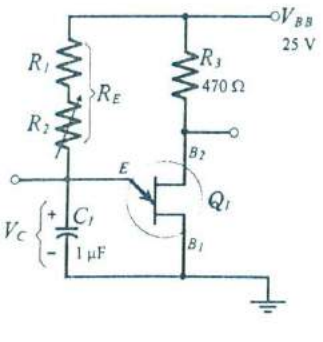
$$R_{E(min)} = \frac{V_{B1B2} - V_{EB1(sat)}}{I_V} \qquad \textbf{(19-11)}$$

UJT Relaxation Oscillator

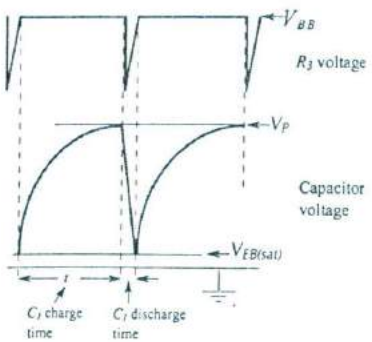
The relaxation oscillator circuit in Fig. 19-43(a) consists of a *UJT* and a capacitor (C_1) charged via resistance R_E. When the capacitor voltage (V_C) reaches V_P the *UJT* fires and rapidly discharges C_1 to $V_{EB1(sat)}$. The device then cuts *off* and the capacitor commences charging again. The cycle is repeated continually, generating a sawtooth waveform across C_1, as illustrated in Fig. 19-43(b). The time (t) for the capacitor to charge from $V_{EB1(sat)}$ to V_P may be calculated, and the frequency of the sawtooth determined approximately as $1/t$. The discharge time (t_D) is difficult to calculate because the *UJT* is in its negative resistance region and its resistance is changing. However, t_D is much less than t, and so it can normally be neglected. Rewriting Eq. 19-6,

$$t = CR\ ln[\frac{V_{BB} - V_{EB1}}{V_{BB} - V_P}] \qquad \textbf{(19-12)}$$

Resistor R_3 in the circuit in Fig. 19-43 is included to produce a spike waveform output, as illustrated. When the *UJT* fires, the current surge through terminal B_2 produces the negative-going voltage spike across R_3. A resistor could also be included in series with terminal B_1 to produce positive-going spikes. Both resistor values should be much lower than the R_{BB} for the *UJT*.



(a) *UJT* relaxation oscillator



(b) Circuit waveforms

Figure 19-43
UJT relaxation oscillator circuit and waveforms. C_1 charges to V_p when the UJT fires, then C_1 is discharged to $V_{BE(sat)}$.

Example 19-8

Calculate the $R_{E(max)}$ and $R_{E(min)}$ for the relaxation oscillator circuit in Fig. 19-43. The *UJT* is a *2N4949* with I_p = 0.6 μA, I_V = 2 mA, and $V_{EB1(sat)}$ = 2.5 V. Also,

determine the approximate maximum oscillating frequency for the circuit when $R_E = 18\ k\Omega$, $C_1 = 1\ \mu F$, and $V_P = 20\ V$.

Solution

From Example 19-7,

$$V_{p(min)} = 19.2\ V, \text{ and } V_{p(max)} = 22.2\ V$$

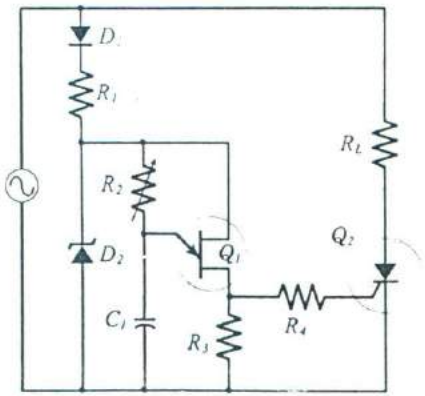
Eq. 19-10,
$$R_{E(max)} = \frac{V_{BB2} - V_{p(max)}}{I_p} = \frac{25\ V - 22.2\ V}{0.6\ \mu A}$$
$$= 4.7\ M\Omega$$

Eq. 19-11,
$$R_{E(min)} = \frac{V_{BB2} - V_{EB1(sat)}}{I_v} = \frac{25\ V - 2.5\ V}{2\ mA}$$
$$= 11.25\ k\Omega$$

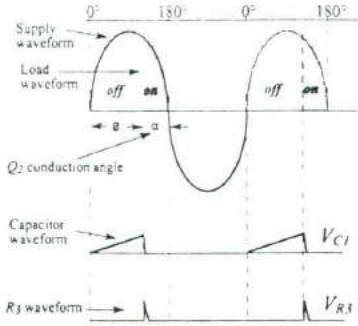
Eq. 19-12,
$$t = CR\ ln[\frac{V_{BB2} - V_{EB1(sat)}}{V_{BB2} - V_p}]$$
$$= 1\ \mu F \times 18\ k\Omega\ \ ln[\frac{25\ V - 2.5\ V}{25\ V - 20\ V}]$$
$$= 27\ ms$$

Eq. 19-12,
$$f = \frac{1}{t} = \frac{1}{27\ ms}$$
$$= 37\ Hz$$

UJT Control of an SCR



(a) *UJT* control circuit for *SCR*



(b) Circuit waveforms

Figure 19-44
UJT 180° phase control circuit for an SCR. Resistor R_2 controls the C_1 charging rate and the SCR firing point.

Unijunction transistors are frequently employed in *SCR* and *TRIAC* control circuits. In the typical circuit shown in Fig. 19-44(a) diode D_1, resistor R_1, and Zener diode D_2 provide a low-voltage *dc* supply to the *UJT* circuit derived from the positive half-cycle of the *ac*

supply voltage. D_1 also isolates the *UJT* circuit during the supply negative half-cycle. Capacitor C_1 is charged via resistor R_2 to the *UJT* firing voltage, and the *SCR* is triggered by the voltage drop across R_3. By adjusting R_2 the charging rate of C_1 and the *UJT* firing time can be selected. The waveforms in Fig. 19-44(b) show that 180° of *SCR* phase control is possible.

Practise Problems

19-7.1 A *2N4870 UJT* has the following parameters: $P_D = 300$ mW at 25°C, $D = 3$ mW/°C, $\eta = 0.56$ to 0.75, $R_{BB} = 4$ kΩ to 9.1 kΩ, $V_{EB1(sat)} = 2.5$ V, $I_P = 1$ μA to 5 μA, $I_V = 2$ mA to 5 mA. Determine the maximum V_{B1B2} that may be used at 75°C.

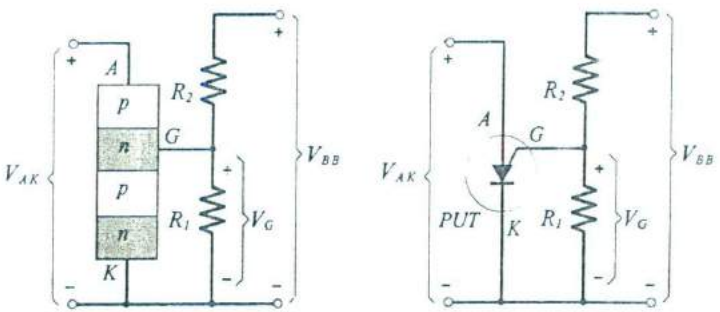
19-7.2 Calculate the $V_{P(max)}$ and $V_{P(min)}$ for a *2N4870* when $V_{BB} = 30$ V.

19-7.3 A *2N4870* is used in the circuit in Fig. 19-44. If D_2 has $V_Z = 30$ V, determine the maximum and minimum resistance values for R_2.

19-8 Programmable Unijunction Transistor (PUT)

PUT Operation

The *programmable unijunction transistor* (*PUT*) is actually an *SCR*-type device used to simulate a *UJT*. The interbase resistance (R_{BB}) and the intrinsic standoff ratio (η) can be programmed to any desired values by selecting two resistors. This means that the device firing voltage (the peak voltage V_P) can also be programmed.



(a) *PUT* four-layer construction (b) *PUT* circuit

Figure 19-45
The programmable unijunction transistor (PUT) is an SCR-type device that can be connected to function like a UJT.

Consider Fig. 19-45(a) which shows a four-layer device with its gate connected to the junction of resistors R_1 and R_2. Note that the gate terminal is close to the anode of the device, instead of the cathode as for an *SCR*. The anode-gate junction becomes forward biased when the anode is positive with respect to the gate. When this occurs, the device is triggered *on*. The anode-to-cathode voltage then drops to a low level, and the *PUT* conducts heavily until the current becomes too low to sustain conduction. To simulate the *UJT* performance, the anode of the device acts as the

UJT emitter, and R_1 and R_2 operate as r_{B1} and r_{B2}, respectively. Parameters R_{BB}, η, and V_P are programmed by selection of R_1 and R_2. The four-layer block diagram is replaced with the *PUT* graphic symbol in Fig. 19-45(b). Note that this is the same as the *SCR* symbol except that the gate terminal is at the anode.

PUT Characteristics

The typical *PUT* characteristic (V_{AK} plotted versus I_A) shown in Fig. 19-46 are seen to be very similar to *UJT* characteristics. A small gate reverse current (I_{AGO}) flows while the anode-gate junction is reverse biased. At this point the *PUT* is in the cutoff region of the characteristics. When the anode voltage is raised sufficiently above the gate voltage (V_G in Fig. 19-45), the *PUT* is triggered into the negative resistance region of its characteristics, and the anode-cathode voltage falls rapidly to the valley voltage (V_v). Further increase in I_A causes the device to operate in its saturation region.

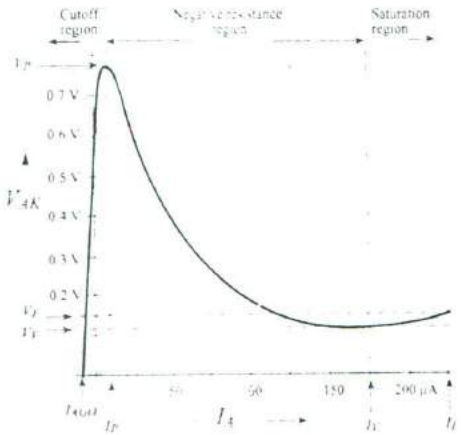


Figure 19-46
The typical V_{AK}/I_A characteristics for a PUT are similar to UJT characteristics.

PUT Parameters

The intrinsic standoff ratio for the *PUT* is,

$$\eta = \frac{R_1}{R_1 + R_2} \qquad \textbf{(19-13)}$$

The gate voltage is simply,

$$V_G = \eta V_{BB} \qquad \textbf{(19-14)}$$

and the peak voltage is,

$$V_P = V_D + \eta V_{BB} \qquad \textbf{(19-15)}$$

where V_D is the anode-gate junction voltage, typically 0.7 V.

The gate source resistance (R_G) is an important quantity because it affects the peak current and valley current for the *PUT*. R_G is the resistance at the junction of voltage divider R_1 and R_2, (Fig. 19-45).

$$R_G = R_1 \| R_2 \quad \textbf{(19-16)}$$

Refer to the partial specification for a *2N6027 PUT* in Fig. 19-47, and note the typical quantities. With $R_G = 1\ M\Omega$, $I_P = 1.25\ \mu A$ and $I_V = 18\ \mu A$; with $R_G = 10\ k\Omega$, $I_P = 4\ \mu A$ and $I_V = 150\ \mu A$.

2N6027 PUT

		Typ	Max
Peak current (I_P)	(R_G = 1 MΩ)	1.25 μA	2 μA
	(R_G = 10 kΩ)	4 μA	5 μA
Valley current (I_V)	(R_G = 1 MΩ)	18 μA	50 μA
	(R_G = 10 kΩ)	150 μA	—
Forward voltage (V_F)	(I_F = 50 mA)	0 8 V	1.5 V

Figure 19-47
Partial specification for a programmable unijunction transistor.

PUT Applications

A *PUT* can be applied in any circuit where a *UJT* might be used. Figure 19-48 shows a *PUT* relaxation oscillator used to control an *SCR*. This circuit operates in essentially the same way as the *UJT* circuit in Fig. 19-44. It should be noted that there are upper and lower limits to the resistance that can be connected in series with the *PUT* anode for correct operation of the device. This is similar to the $R_{E(min)}$ and $R_{E(max)}$ requirement for the *UJT*.

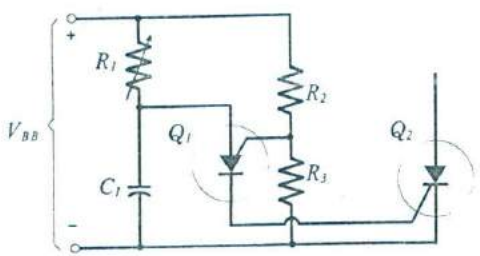


Figure 19-48
SCR phase control circuit using a PUT relaxation oscillator.

A battery charger circuit using a *PUT* (Q_1) and an *SCR* (Q_2) is shown in Fig. 19-49. The *ac* supply voltage is full-wave rectified and applied via current-limiting resistor R_5 to the anode of the *SCR*. The *SCR* is triggered into conduction by the *PUT* output coupled via transformer T_1. The *PUT* gate voltage (V_G) is set by the voltage divider (R_3, R_4, and R_5). While V_G is lower than the Zener diode voltage (V_Z), capacitor C_1 is charged via R_1 to the *PUT* peak voltage. At this point the *PUT* fires and triggers the *SCR on*.

As the battery charges, its voltage (E_B) increases, and thus V_G also increases. The increased V_G level raises the V_P of the *PUT* and causes C_1 to take a longer time charge. Consequently, the *SCR* is held *off* for a longer portion of the *ac* supply half-cycle. This means that the average charging current is gradually reduced as the

battery approaches full charge. When E_B is fully charged, V_G is raised to the V_Z level, so that D_6 conducts and stops C_1 voltage increase before the *PUT* fires. Thus, the *SCR* remains *off*, and battery charging stops. The circuit will not operate if the battery is connected with the wrong polarity.

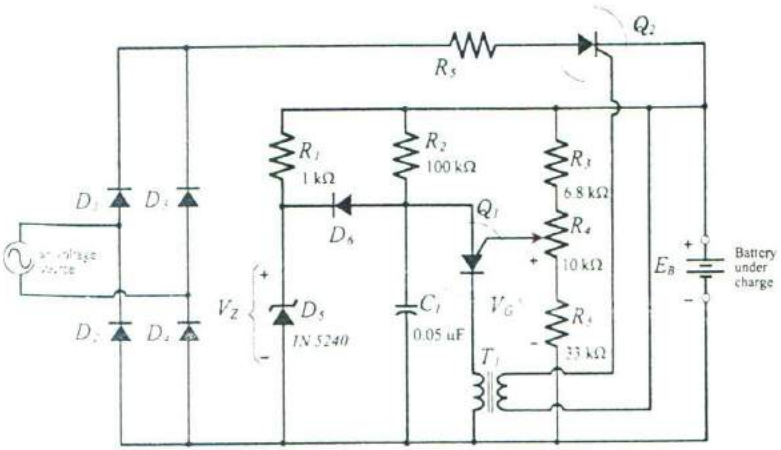


Figure 19-49
SCR battery charger using a PUT control circuit.

Example 19-9

Calculate $V_{P(max)}$ and $V_{P(min)}$ for the *PUT* in the circuit in Fig. 19-49 when E_B = 12 V. Also, determine the gate bias resistance R_G, and calculate the maximum and minimum resistances for R_2 if the *PUT* is a *2N6027*.

Solution

Eq. 19-13,
$$\eta_{(max)} = \frac{R_4 + R_5}{R_3 + R_4 + R_5} = \frac{10\ \text{k}\Omega + 33\ \text{k}\Omega}{6.8\ \text{k}\Omega + 10\ \text{k}\Omega + 33\ \text{k}\Omega}$$
$$= 0.86$$

$$\eta_{(min)} = \frac{R_5}{R_3 + R_4 + R_5} = \frac{33\ \text{k}\Omega}{6.8\ \text{k}\Omega + 10\ \text{k}\Omega + 33\ \text{k}\Omega}$$
$$= 0.66$$

Eq. 19-15,
$$V_{P(max)} = V_D + (\eta_{(max)} V_{BB}) = 0.7\ \text{V} + (0.86 \times 12\ \text{V})$$
$$= 11\ \text{V}$$

$$V_{P(min)} = V_D + (\eta_{(max)} V_{BB}) = 0.7\ \text{V} + (0.66 \times 12\ \text{V})$$
$$= 8.6\ \text{V}$$

Eq. 19-16,
$$R_G = (R_3 + 0.5\,R_4) \| (R_5 + 0.5\,R_4)$$
$$= (6.8\ \text{k}\Omega + 5\ \Omega) \| (33\ \text{k}\Omega + 5\ \text{k}\Omega)$$
$$= 9\ \text{k}\Omega$$

$$R_{2(max)} = \frac{E - V_{P(max)}}{I_P} = \frac{12\ \text{V} - 11\ \text{V}}{4\ \mu\text{A}}$$
$$= 250\ \text{k}\Omega$$

$$R_{2(min)} = \frac{E - V_F}{I_V} = \frac{12\,V - 0.8\,V}{150\,\mu A}$$
$$= 74\,k\Omega$$

Practise Problems

19-8.1 The circuit in Fig. 19-48 has: $V_{BB} = 15$ V, $R_2 = 12\,k\Omega$, and $R_3 = 18\,k\Omega$. The *PUT* has $I_P = 10\,\mu A$, $I_V = 100\,\mu A$, and $V_F = 1$ V. Calculate R_G, η, V_P, and the maximum and minimum resistances for R_1.

19-8.2 Determine the voltage that the battery will be charged to in Fig. 19-49 when the moving contact is at the middle point on R_4. Assume that the *PUT* will stop firing when V_{AG} is reduced to 0.5 V.

Chapter-19 Review Questions

Section 19-1

19-1 Sketch the construction of a silicon controlled rectifier. Also, sketch the two-transistor equivalent circuit and show how it is derived from the *SCR* construction. Label all terminals and explain how the device operates.

19-2 Sketch typical *SCR* forward and reverse characteristics. Identify all regions of the characteristics and all important current and voltage levels. Explain the shape of the characteristics in terms of the *SCR* two-transistor equivalent circuit.

19-3 List the most important *SCR* parameters and state typical quantities for low, medium, and high current devices.

Section 19-2

19-4 Draw the circuit diagram to show how an *SCR* can be triggered by application of a pulse to the gate terminal. Sketch the circuit waveforms and explain its operation.

19-5 Sketch a 90° phase control circuit for an *SCR*. Draw the load waveform and explain the operation of the circuit. Also, show the circuit and load waveforms when the *ac* supply is full-wave rectified.

19-6 Draw the diagram for a 90° phase control circuit using two *SCRs* for full-wave phase control. Draw the load waveforms and briefly explain the circuit operation.

19-7 Sketch a 180° phase control for an *SCR*. Draw the load waveform and explain the circuit operation.

Section 19-3

19-8 Briefly discuss *SCR* circuit stability, and draw diagrams to show methods that can be used to improve stability.

19-9 Draw the diagram for an *SCR* zero-point triggering circuit. Explain the circuit operation and advantages, and draw the load waveform.

19-10 Sketch a circuit that uses an *SCR* to protect a load from excessive *dc* supply voltage. Briefly explain.

19-11 Draw a diagram for an *SCR* heater control circuit using a temperature-sensitive device. Explain the circuit operation.

Section 19-4

19-12 Draw sketches to show the construction, equivalent circuit, and characteristics of a *TRIAC*. Identify all important voltage and current levels on the characteristics and explain the operation of the device.

19-13 Using appropriate diagrams, explain the four quadrant operating conditions for a *TRIAC*.

19-14 Draw the typical characteristics for a *DIAC*. Explain the *DIAC* operation, and sketch the two circuit symbols used for the device.

Section 19-5

19-15 Draw the diagram for a *TRIAC* 180° phase control circuit. Draw all waveforms, and explain the circuit operation.

19-16 Draw the diagram for an *TRIAC* zero-point triggering circuit and carefully explain its operation

19-17 Sketch the functional block diagram for an *IC* zero voltage switch for *TRIAC* control. Discuss the components of the block diagram.

Section 19-6

19-18 Using appropriate diagrams, briefly explain a silicon unilateral switch (*SUS*). Draw the device circuit symbol.

19-19 Sketch the equivalent circuit and characteristics for a silicon bilateral switch (*SBS*). Explain how the device construction differs from other thyristors. Discuss the device operation, state typical parameters, and show how the switching voltage can be modified.

19-20 Sketch a relaxation oscillator circuit using an *SBS*. Draw the output waveform, and explain the circuit operation.

19-21 Draw the circuit symbol and equivalent circuit for a gate turnoff device (*GTO*) and discuss its operation.

19-22 Draw the circuit symbol and typical characteristics for a *SIDAC*. Discuss its operation and applications.

Section 19-7

19-23 Draw sketches to show the basic construction and equivalent circuit of a unijunction transistor (*UJT*). Briefly explain the device operation.

19-24 Sketch typical *UJT* V_{EB1}/I_E characteristics for $I_{B2} = 0$, $V_{B1B2} = 20$ V, and $V_{B1B2} = 10$ V. Identify each region and all important points on the characteristics, and explain the shape of the characteristics.

19-25 Define the following *UJT* parameters: intrinsic standoff ratio, interbase resistance, emitter saturation voltage, peak point current, valley point current.

19-26 Draw the circuit of a *UJT* relaxation oscillator with provision for frequency adjustment and spike waveform. Show all waveforms and explain the circuit operation.

19-27 Sketch a *UJT* circuit for controlling an *SCR*. Also, draw all waveforms, and briefly explain how the circuit operates.

Section 19-8

19-28 Draw the basic block diagram and basic circuit for a programmable unijunction transistor (*PUT*), and explain the device operation.

19-29 Sketch typical *PUT* characteristic, explain how the intrinsic stand-off ratio may be programmed, and identify the most important *PUT* parameters.

19-30 Draw a basic *PUT* circuit for controlling an *SCR*, and explain its operation.

19-31 Draw the circuit diagram of a battery charger using a *PUT* and an *SCR*. Explain the circuit operation.

Chapter-19 Problems

Section 19-1

19-1 Consult *2N6167* and *2N1595* *SCR* specifications to determine the typical values for: V_{DRM}, I_T, V_{TM}, I_H, I_{GT}, V_{GT}.

Section 19-2

19-2 Select a suitable *SCR* from Fig. 19-10 for a circuit with a 115 V *ac* supply. Calculate the minimum load resistance that can be supplied, and determine the instantaneous voltage level when the *SCR* switches *off*.

19-3 A 33 Ω resistor is supplied from an *ac* source with a 60 V peak level. Current to the load is to be switched *on* and *off* by an *SCR*. Select a suitable device from the specifications in Appendix 1-17, and determine the instantaneous supply voltage at which the *SCR* switches off.

19-4 An *SCR* with a 115 V *ac* supply controls the current through a 150 Ω load resistor. A 90° phase-control circuit (as in Fig. 19-11) is employed to trigger the *SCR* between 12° and 90°. The gate trigger current is 50 μA and the trigger voltage is 0.5 V. Calculate suitable resistor values.

19-5 The circuit in Fig. 19-12 has a 50 V *ac* supply and $R_L = 20\ \Omega$. Determine suitable resistance values for R_1, R_2, and R_3 for the *SCR* to be triggered anywhere between 7.5° and 90°. The gate trigger current and voltage are 500 μA and 0.6 V.

19-6 The circuit in Problem 19-5 uses a *2N5170 SCR* (see Appendix 1-17). Calculate the instantaneous supply voltage level when the *SCR* switches *off*.

19-7 Design the circuit in Fig. 19-13 for 10° to 90° phase control and specify the *SCRs*. The *ac* supply is 115 V, $R_L = 12\ \Omega$, and the *SCRs* have $V_G = 0.6$ V and $I_G = 100$ μA.

19-8 A 180° phase circuit as in Fig. 19-15 has a 40 V, 400 Hz *ac* supply and $R_L = 22\ \Omega$. The *SCR* has $V_G = 0.5$ V, $I_G = 60$ μA, and $I_{GM} = 20$ mA. Determine suitable resistor and capacitor values, and specify the *SCRs* and the diodes.

Section 19-3

19-9 An *SCR* crowbar circuit (as in Fig. 19-19) is connected to a 12 V *dc* supply with a 200 mA current limiter. Design the crowbar circuit to protect the load from voltage levels greater than 13.5 V. Assume that $V_G = 0.7$ V for the *SCR*.

19-10 A zero-point triggering circuit (as in Fig. 19-18) is to control the power dissipation in a 12 Ω load resistor with a 115 V, 60 Hz *ac* supply. Assuming that the *SCRs* have $V_G = 0.5$ V and $I_{G(min)} = 10$ mA, determine suitable capacitor and resistor values.

19-11 An *SCR* heater control circuit (as in Fig. 19-20) is to switch *on* at 68°C and *off* at 71°C. The circuit is to operate from a 50 V, 60 Hz supply, and the available temperature-sensitive device has a resistance of 500 Ω at 68°C and 350 Ω at 71°C. The load resistance is $R_L = 2.5\ \Omega$ and the *SCR* has $V_G = 0.6$ V. Determine suitable component values, and calculate the *SCR* gate voltage at 71°C.

19-12 Specify the *SCRs* required for the circuits in Problems 19-9, 10, and 11 in terms of maximum anode-cathode voltage and maximum anode current.

Section 19-4

19-13 Consult specifications for *2N6071* and *2N6343 TRIACs* to determine the maximum supply voltage, maximum *rms* current, and the typical quadrant *I* gate triggering voltage.

Section 19-5

19-14 A light dimmer uses a *TRIAC* 180° phase control circuit, as in Fig. 19-27. The *ac* supply is 220 V, 60 Hz, and the total load is 750 W. The *TRIAC* has triggering current $I_G = 200$ μA, maximum gate current $I_{GM} = 50$ mA, and $V_G = 0.7$ V. The *DIAC* has $V_S = 9.2$ V and $I_S = 400$ μA. Determine suitable component values.

19-15 The *TRIAC* control circuit in Fig. 19-27 has the following components: R_L = 100 Ω, R_1 = 10 kΩ, R_2 = 500 Ω, C_1 = 3.9 μF. The *DIAC* has V_S = 7 V and the *TRIAC* has V_G = 1 V. The *ac* supply is 60 V, 60 Hz. Determine the minimum conduction angle for the *TRIAC*.

19-16 Specify the *TRIACs* required for the circuits in Problems 19-14 and 15.

19-17 The *TRIAC* zero-point switching circuit in Fig. 19-28 uses an *SCR* with I_G = 100 μA and V_F = 1.5 V. The *TRIAC* has I_G = 5 mA, I_{GM} = 500 mA, and t_{on} = 50 μs. The control voltage is E = 5 V, the *ac* source is 60 V, 60 Hz, and the load is R_L = 15 Ω. Determine suitable component values.

Section 19-6

19-18 A relaxation oscillator (as in Fig. 19-35) uses an *SBS* with V_S = 8 V, V_F = 1 V, I_S = 300 μA, and I_H = 1 mA. The *dc* supply is E = 40 V. Calculate maximum and minimum R_1 values for correct operation of the circuit.

19-19 A relaxation oscillator (as in Fig. 19-35) has a 25 V supply, a 1 μF capacitor, and a 12 kΩ series resistor. The capacitor is to charge up to 15 V and then discharge to approximately 1 V. Specify the required *SBS* in terms of forward conduction voltage, switching voltage, switching current, and holding current.

19-20 The phase control circuit in Fig. 19-34 has the following components: R_L = 18 Ω, R_1 = 12 kΩ, R_2 = 470 Ω, C_1 = 10 μF. Resistors R_3 and R_4 are replaced with 3.3 V Zener diodes, and the *TRIAC* triggering voltage is V_G = 1 V. The *ac* supply is 115 V, 60 Hz. Determine the *TRIAC* minimum conduction angle.

Section 19-7

19-21 Determine the maximum power dissipation for a *2N2647 UJT* at an ambient temperature of 70°C. Also, calculate the maximum level of V_{B1B2} that may be used at 70°C. Appendix 1-18 gives partial specification for the *2N2647*.

19-22 Calculate the minimum and maximum V_{EB1} triggering levels for a *2N2647 UJT* when V_{B1B2} = 20 V.

19-23 A relaxation oscillator (as in Fig. 19-43) uses a *2N2647 UJT* with V_{BB} = 25 V. Calculate the typical oscillation frequency if C_1 = 0.5 μF and R_E = 3.3 kΩ.

19-24 Calculate the maximum and minimum charging resistance values that can be used in the circuit of Problem 19-23.

19-25 The *UJT* phase control circuit in Fig. 19-44 has a 115 V, 60 Hz *ac* supply, and an *SCR* with V_G = 1 V and I_{GM} = 25 mA. Design the circuit to use a *2N2647 UJT* and a Zener diode with V_Z = 15 V.

Section 19-8

19-26 A *PUT* operating from a 25 V supply has $V_F = 1.5$ V and $I_G = 50$ μA. Determine values for R_1 and R_2 to program η to 0.75. Also, calculate V_P, V_V, R_{BB}, and R_G.

19-27 A *PUT* relaxation oscillator (as in Fig. 19-48) has a 20 V supply and a 0.68 μF capacitor. The *PUT* has $V_G = 1$ V and $I_G = 100$ μA. The peak capacitor voltage is to be 5 V and the oscillating frequency is to be 300 Hz. Determine suitable resistor values.

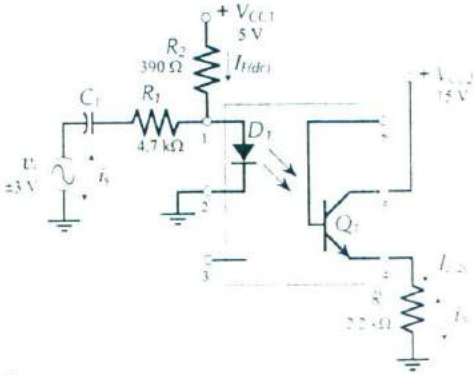
19-28 The *UJT* in Problem 19-23 is to be replaced with a *PUT*. Determine suitable resistance values for the gate bias voltage divider.

19-29 A *PUT* has a forward voltage of $V_F = 0.9$ V and $I_G = 200$ μA. The device is to be programmed to switch on at $V_G = 15$ V when operating from a 24 V supply. Determine values for R_1 and R_2, and calculate V_P, V_V, R_{BB}, and R_G.

Practise Problem Answers

19-2.1 163 V, 1.6 A, 18 kΩ, 1.5 kΩ, 180 Ω
19-2.2 10 kΩ, 0.82 μF, 1.5 kΩ
19-3.1 (68 kΩ + 12 kΩ), 4 μF
19-5.1 1 kΩ, 180 Ω, 5.6 kΩ, 1 kΩ, 2.5 μF, 1 μF
19-6.1 500 kΩ, 820 Ω
19-7.1 24.5 V
19-7.2 23.2 V, 17.5 V
19-7.3 1.36 MΩ, 6.25 kΩ
19-8.1 7.2 kΩ, 0.6, 9.7 V, 530 kΩ, 140 kΩ
19-8.2 13.4 V

Chapter 20
Optoelectronic Devices



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Objectives

You will be able to:

1. *Define important illumination units, and calculate illumination intensity at a given distance from a source.*
2. *Explain the fabrication and operation of a light emitting diode (LED), discuss its parameters, and design LED circuits.*
3. *Explain the operation of liquid crystal displays (LCDs). Show how LCDs and LEDs are used in seven-segment numerical displays, and calculate power dissipations in each type of display.*
4. *Explain the construction and operation of a photoconductive cell. Sketch the device characteristics, and discuss its parameters.*
5. *Design photoconductive cell circuits to bias BJTs on or off, energize relays, trigger Schmitt circuits etc.*
6. *Explain the construction and operation of a photodiode. Sketch photodiode characteristics, and discuss its parameters.*
7. *Design photodiodes into circuits where they operate as a photoconductive device, and as a photovoltaic device.*
8. *Explain solar cells, and design solar cell battery charger circuits.*
9. *Explain the operation of a phototransistor. Sketch phototransistor characteristics, and discuss its parameters. Also, explain photodarlingtons and photoFETs.*
10. *Design phototransistor circuit for energizing relays, triggering SCRs, etc.*
11. *Explain the construction and operation of optocouplers, and discuss optocoupler parameters.*
12. *Design optocoupler circuits for coupling pulse-type and linear signals between systems with different supply voltages.*

Introduction

Optoelectronic devices emit light, modify light, have their resistance affected by light, or produce currents and voltages proportional to light intensity.

Light-emitting diodes (*LEDs*) produce light, and are typically used as indicating lamps and in numerical displays. Liquid crystal displays (*LCDs*) which modify light are also used as numerical displays. Photoconductive cells have a resistance that depends upon illumination intensity. They are used in circuits designed to produce an output change when the light level changes. The current and voltage levels in photodiodes and phototransistors are affected by illumination. These devices are also used in circuit that have their conditions altered by light level changes. Illumination is converted into electrical energy by means of solar cells, and this energy is often used to charge storage batteries. Optocouplers combine *LEDs* and phototransistors to provide a means of coupling between circuits that have different supply voltages, while maintaining a high level of electrical insolation.

20-1 Light Units

The total light energy output, or *luminous flux* (ϕ_s), from a source can be measured in *milliwatts* (mW) or in *lumens* (lm), where 1 lm = 1.496 mW. The *luminous intensity* (E_s) (also termed *illuminance*) of a light source is defined as the luminous flux density per unit solid angle (or cone) emitting from the source, [see Fig. 20-1(a)]. This is measured in *Candelas* (*cd*), where one candela is equal to one lumen per unit solid angle, (assuming a point source that emits light evenly in all directions).

$$E_s = \frac{\phi_s}{4\pi} \qquad \textbf{(20-1)}$$

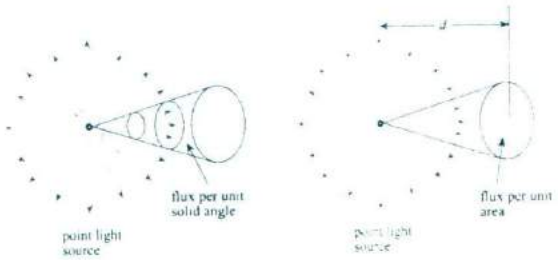
The light intensity (E_A) on an area at a given distance from the source is determined from the surface area of a sphere surrounding the source, [Fig. 20-1(b)]. At a distance of r meters, the luminous flux is spread over a spherical area of $4\pi r^2$ square meters, so

$$E_A = \frac{\phi_s}{4\pi r^2} \qquad \textbf{(20-2)}$$

When the total flux is expressed in lumens, Eq. 20-2 gives the luminous intensity in *lumens per square meter* (lm/m^2), also termed *lux* (*lx*). Comparing Eq. 20-2 to Eq. 20-1, it is seen that the luminous intensity per unit area at any distance r from a point source is determined by dividing the source intensity by r^2.

Luminous intensity can also be measured in *milliwatts per square centimeter* (mW/cm^2), or *lumens per square foot* (lm/ft^2), also known as a *foot candle* (*fc*), where 1 fc = 10.764 lx.

The light intensity of sunlight on the earth at noon on a clear day is approximately 107,640 lx, or 161 W/m². The light intensity from a 100 W lamp is approximately 4.8×10^3 cd, (allowing for a 90% lamp efficiency). At a distance of 2 m, this is 1.2×10^3 lx. An indicating lamp with a 3 mcd output can be clearly seen at a distance of several meters in normal room lighting conditions.



(a) Flux per unit solid angle (b) Flux per unit area

Figure 20-1
Light intensity can be expressed in flux per unit solid angle, or in flux per unit area.

Example 20-1

Calculate the light intensity 3 m from a lamp that emits 25 W of light energy. Also, determine the total luminous flux striking an area of 0.25 m² at 3 m from the lamp.

Solution

Eq. 20-2, $$E_A = \frac{\phi_s}{4\pi r^2} = \frac{25\text{ W}}{4\pi \times (3\text{ m})^2}$$

$$= 0.221\text{ W/m}^2 = 221\text{ mW/m}^2$$

$$\text{Total flux} = E_A \times \text{area} = 221\text{ mW/m}^2 \times 0.25\text{ m}^2$$

$$\approx 55\text{ mW}$$

Example 20-2

Determine the light intensity at a distance of 2 m from a 10 mcd source.

Solution

$$E_A = \frac{E_s\text{ (cd)}}{r^2} = \frac{10\text{ mcd}}{2^2}$$

$$= 2.5\text{ mlx}$$

Light energy is electromagnetic radiation; it is in the form of electromagnetic waves. So, it can be defined in terms of *frequency* or *wavelength*, as well as intensity. Wavelength, frequency, and velocity are related by the equation;

$$c = f\lambda \qquad \textbf{(20-3)}$$

where c = velocity = 3×10^8 m/s for electromagnetic waves
f = frequency in Hz
λ = wavelength in meters

The wavelength of visible light ranges from violet at approximately 380 nm (*nanometers*) to red at 720 nm. From Eq. 20-3 , the frequency extremes are:

$$f_{violet} = \frac{c}{\lambda} = \frac{3 \times 10^8 \text{ m/s}}{380 \text{ nm}}$$
$$\approx 8 \times 10^{14} \text{ Hz}$$
$$f_{red} = \frac{c}{\lambda} = \frac{3 \times 10^8 \text{ m/s}}{720 \text{ nm}}$$
$$\approx 4 \times 10^{14} \text{ Hz}$$

Practise Problems

20-1.1 A lamp is required to produce a light intensity of 213 lx at a distance of 5 m. Calculate the total light energy output of the lamp in watts.

20-1.2 Calculate the frequency of yellow light with a 585 nm wavelength.

20-1.3 Determine the light intensity 3.3 m from an 8 mcd lamp, and the total luminous flux striking a 4 cm^2 area at that location.

20-2 Light Emitting Diode (LED)

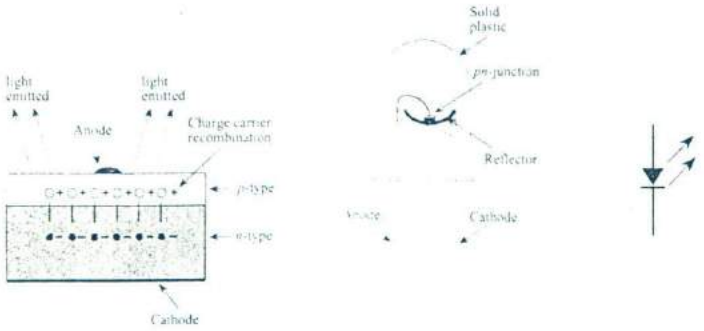
LED Operation and Construction

Charge carrier recombination occurs at a forward biased *pn*-junction as electrons cross from the *n*-side and recombine with holes on the *p*-side. Free electrons have a higher energy level than holes, and some of this energy is dissipated in the form of heat and light when recombination takes place. If the semiconductor material is translucent, the light is emitted and the junction becomes a light source; that is, a *light-emitting diode* (*LED*).

A cross-sectional view of an *LED* junction is shown in Fig. 20-2(a). The semiconductor material is gallium arsenide (*GaAs*), gallium arsenide phosphide (*GaAsP*), or gallium phosphide (*GaP*). An *n*-type epitaxial layer is grown upon a substrate, and the *p*-region is created by diffusion. Charge carrier recombinations occur in the *p*-region, so the *p*-region is kept uppermost to allow the light to escape. The metal film anode connection is patterned to allow most of the light to be emitted. A gold film is applied to the bottom of the substrate to reflect as much light as possible toward the surface of the device and to provide a cathode connection. *LEDs* made from *GaAs* emit infrared (invisible) radiation. *GaAsP* material provides either red light or yellow light, while red or green emission can be produced by using *GaP*. Using various materials, *LEDs* can be manufactured to produce light of virtually any color.

Figure 20-2(b) shows the typical construction of a *LED*. The *pn*-junction is mounted on a cup-shaped reflector, as illustrated, wires are provided for anode and cathode connection, and the device is encapsulated in an epoxy lens. The lens can be clear or colored, and (when not energized) the lens color identifies the *LED*

light color. The color of the light emitted by the energized *LED* is determined solely by the *pn*-junction material. Some *LEDs* have glass particles embedded in the epoxy lens to diffuse the emitted light and increase the viewing angle of the device. The *LED* circuit symbol is shown in Fig. 20-2(c). Note that the arrow directions indicate emitted light.



(a) *LED* junction (b) Typical construction (c) Graphic symbol

Figure 20-2
A light-emitting diode (LED) produces energy in the form of light when charge carrier recombination occurs at the pn-junction.

Characteristics and Parameters

LED characteristics are similar to those of other semiconductor diodes, except that (as shown in the partial specification in Fig. 20-3) the typical forward voltage drop is 1.6 V. Note also, that the reverse breakdown voltage can be as low as 3 V. In some circuits it is necessary to include a diode with a high reverse breakdown voltage in series with a *LED*. The forward current used with a *LED* is usually in the 10 mA to 20 mA range, but (depending on the particular device) the peak current can be as high as 90 mA. *LED* luminous intensity depends on the forward current level; it is usually specified at 20 mA. The peak wavelength of the light output is also normally listed on the specification.

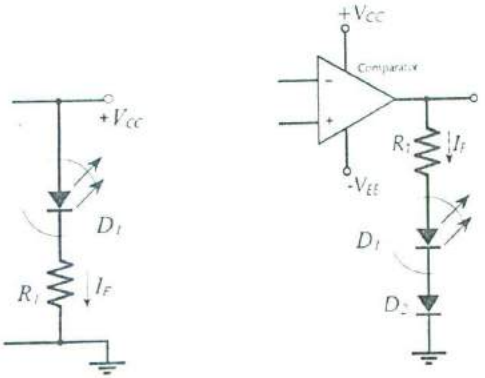
Typical LED Specification

	Min	Typ	Max
Luminous intensity (I_V at 20 mA)	4 mcd	8 mcd	
Forward voltage (V_F)	1.4 V	1.6 V	2.0 V
Reverse Breakdown voltage (V_{FBR})	3 V	10 V	
Peak forward current ($I_{F(max)}$)		90 mA	
Average forward current ($I_{F(av)}$)		20 mA	
Power dissipation (P_D)		100 mW	
Response speed (τ_S)		90 ns	
Peak wavelength (λ_P)		660 nm	

Figure 20-3
Partial specification for a typical light emitting diode.

LED Circuits

As explained, an *LED* is a semiconductor diode that emits light when a forward current is passed through the device. A single *LED* might simply be employed as a supply voltage *on/off* indicator, as illustrated in Fig. 20-4(a). A series-connected resistor (R_1) must be included to limit the current to the desired level. Figure 20-4(b) shows an *LED* connected at the output of a comparator to indicate a *high* output voltage. As well as the current-limiting resistor (R_1), an ordinary semiconductor diode (D_1) is connected in series with the *LED* to protect it from an excessive reverse voltage when the comparator output is negative.

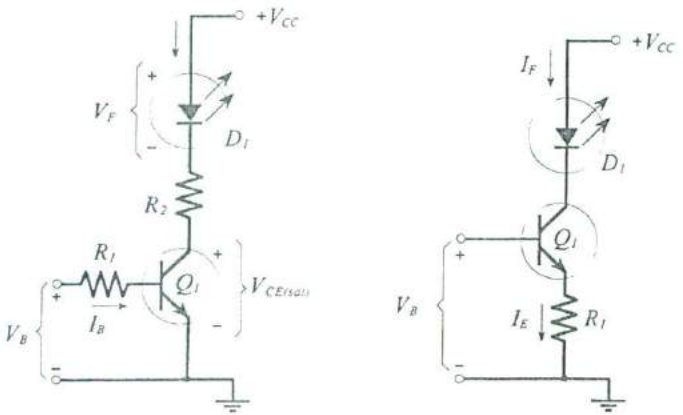


(a) *LED* as *on/off* indicator

(b) *LED* as *high* output voltage indicator

Figure 20-4
Light emitting diode indicator circuits.

LEDs are often controlled by a *BJT*, as illustrated in Fig. 20-5(a) and (b). Transistor Q_1 in Fig. 20-5(a) is switched into saturation by the input voltage (V_B). Resistor R_1 limits the transistor base current, and R_2 limits the *LED* current. In Fig. 20-5(b), the emitter resistor (R_1) limits the *LED* current to $(V_B - V_{BE})/R_1$.



(a) R_2 controls I_F. Q_1 is saturated

(b) R_1 controls I_F. Q_1 is *not* saturated

Figure 20-5
BJT control circuits for light emitting diodes.

Example 20-3

The *LED* in Fig. 20-5(a) is to have a forward current of approximately 10 mA. The circuit voltages are V_{CC} = 9 V, V_f = 1.6 V, and V_B = 7 V; and Q_1 has $h_{FE(min)}$ = 100. Calculate suitable resistance values for R_1 and R_2.

Solution

$$R_2 = \frac{V_{CC} - V_f - V_{CE(sat)}}{I_C} = \frac{9\text{ V} - 1.6\text{ V} - 0.2\text{ V}}{10\text{ mA}}$$

$$= 720\ \Omega \text{ (use 680 } \Omega \text{ standard value)}$$

I_C becomes,

$$I_C = \frac{V_{CC} - V_f - V_{CE(sat)}}{R_2} = \frac{9\text{ V} - 1.6\text{ V} - 0.2\text{ V}}{680\ \Omega}$$

$$= 10.6\text{ mA}$$

$$I_B = \frac{I_C}{h_{FE(min)}} = \frac{10.6\text{ mA}}{100}$$

$$= 106\ \mu\text{A}$$

$$R_1 = \frac{V_B - V_{BE}}{I_B} = \frac{7\text{ V} - 0.7\text{ V}}{106\ \mu\text{A}}$$

$$= 59\text{ k}\Omega \text{ (use 56 k}\Omega \text{ standard value)}$$

Practise Problems

20-2.1 The *LED* in the circuit in Fig. 20-5(b) is to pass a 20 mA current. The circuit voltages are V_{CC} = 15 V, V_f = 1.9 V, and V_B = 5 V. Determine a suitable resistance for R_1, and calculate V_{CE} for Q_1.

20-2.2 Determine suitable resistances for the circuits in Fig. 20-4 to give I_f = 15 mA. The *LEDs* have V_f = 1.8 V. Also, V_{CC} = 6 V in Fig. 20-4(a), and in Fig. 20-4(b) the op-amp output is V_o = ±9 V.

20-3 Seven-Segment Displays

LED Seven-Segment Display

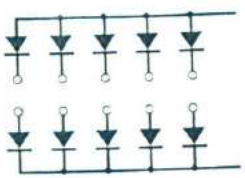
The arrangement of a *seven-segment LED* numerical display is shown in Fig. 20-6(a). The actual *LED* devices are very small, so, to enlarge the lighted surface, solid plastic *light pipes* are often employed, as shown. Any desired numeral from 0 to 9 can be indicated by passing current through the appropriate segments, [Fig 20-6(b)]. Part (c) in Fig. 20-6 shows three seven-segment displays together with a two-segment display referred to as a *half digit*. The whole display, termed a *three-and-a-half digit display*, can be used to indicate numerical values up to a maximum of 1999.

The *LEDs* in a seven-segment display may be connected in *common-anode* or in *common-cathode* configuration, [Fig. 20-6(d)]. When selecting a *LED* seven-segment display, it is important to

(a) Seven-segment *LED* display

(b) Seven-segment numeral displays

(c) Three-and-a-half digit display



(d) Common-anode and common-cathode connections

Figure 20-6
Light emitting diodes can be arranged in seven-segment format for numerical displays.

determine which of the two connecting arrangements is required.

The relatively large amounts of current consumed by *LED* seven-segment displays are their major disadvantage. Apart from this, *LEDs* have the advantage of long life and ruggedness.

Example 20-4

Calculate the total power supplied to a $3^1/_2$ digit *LED* display when it indicates 1999. A 5 V supply is used, and each *LED* has a 10 mA current.

Solution

total segments $N = [3 \times (\text{segments for 8})] + [1 \times (\text{segments for 1})]$

$= (3 \times 7) + (1 \times 2) = 23$

total current $I_T = N \times (\text{current per segment}) = 23 \times 10\ \text{mA}$

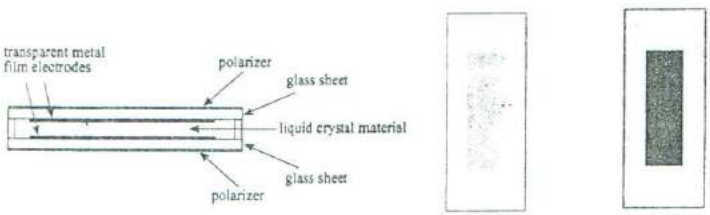
$= 230\ \text{mA}$

power $P = I_T \times V_{CC} = 230\ \text{mA} \times 5\ \text{V}$

$= 1.15\ \text{W}$

Liquid Crystal Cells

Liquid crystal material is a liquid that exhibits some of the properties of a solid. The molecules in ordinary liquids normally have random orientations. In liquid crystals the molecules are oriented in a definite crystal pattern.



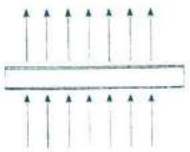
(a) Cross-section of a liquid crystal cell (b) Unergized cell (c) Energized cell

Figure 20-7
A liquid crystal cell consists of a layer of liquid crystal material sandwiched between glass sheets with transparent metal film electrodes and polarizers.

A liquid crystal cell consists of a very thin layer of liquid crystal material sandwiched between glass sheets, as illustrated in Fig. 20-7(a). The glass sheets have transparent metal film electrodes deposited on the inside surfaces. In the commonly used *twisted nematic* cell two thin polarizing optical filters are placed at the surface of each glass sheet. The liquid-crystal material employed twists the light passing through when the cell is not energized. This twisting allows the light to pass through the polarizing filters, so that the cell is semi-transparent. When energized, the liquid molecules are reoriented so that no twisting occurs, and no light can pass through. Thus, the energized cell can appear dark against a bright background. The cells can also be manufactured to appear bright against a dark background.

Seven-segment numerical (and other type) displays made from liquid crystal cells are referred to as *liquid crystal displays* (*LCDs*). Two types of *LCDs* are illustrated in Fig. 20-8. The *reflective*-type shown in Fig. 20-8(a) relies on reflected light. The cell is placed on a reflective surface, so that when not energized it is just as reflective as the surrounding material, consequently, it disappears. When energized, no light is reflected from the cell, and it appears dark against the bright background. The *transmittive* cell in Fig. 20-8(b) allows light to pass through from the back of the cell when not energized. When energized, the light is blocked, and here again the cell appears dark against a bright background. The *transreflective* cell is a combination of transmittive and reflective types.

(a) Reflective cell



(b) Transmittive cell

Figure 20-8
Reflective-type liquid crystal cells reflect incident light. Transmittive-type pass light from behind.

LCD Seven-Segment Display

Because liquid-crystal cells are light reflectors or transmitters rather than light generators, they consume very small quantities of energy. The only energy required by the cell is that needed to activate the liquid crystal. The total current flow through four small seven-segment *LCDs* is typically about 20 μA. However, *LCDs* require an *ac* voltage supply, either in the form of a sine wave or a square wave. This is because a continuous direct current flow produces a plating of the cell electrodes that could damage the device. Repeatedly reversing the current avoids this problem.

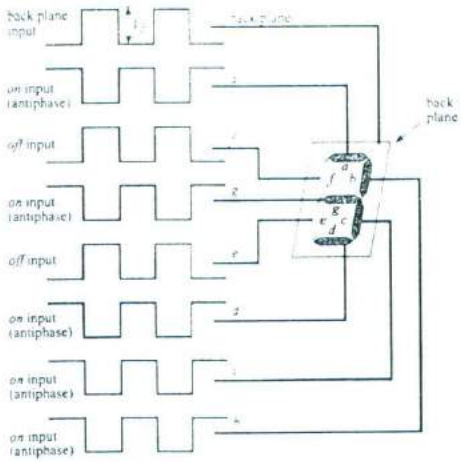


Figure 20-9
Liquid crystal display using a square wave supply. A segment is energized when its input is in antiphase with the back plane input.

A typical *LCD* supply is a 3 V to 8 V peak-to-peak square wave with a frequency of 60 Hz. Figure 20-9 illustrates the square wave drive method. The *back plane*, which is common to all of the cells, is supplied with a square wave, (with peak voltage V_p). Similar square wave applied to each of the other terminals are either in phase or in antiphase with the back plane square wave. Those cells with waveforms in phase with the back plane waveform (cells *e* and *f* in Figure 20-9) have no voltage developed across them. Both terminals of the segment are at the same potential, so they

are not energized. The cells with square waves in antiphase with the back plane input have a square wave with peak voltage $2V_p$ developed across them, consequently, they are energized.

Unlike *LED* displays, which are usually quite small, *LCDs* can be fabricated in almost any convenient size. The major advantage of *LCDs* is their low power consumption. Perhaps the major disadvantage of the *LCD* is its decay time of 150 ms (or more). This is very slow compared to the rise and fall times of *LEDs*. In fact, the human eye can sometimes observe the fading out of *LCD* segments switching *off*.

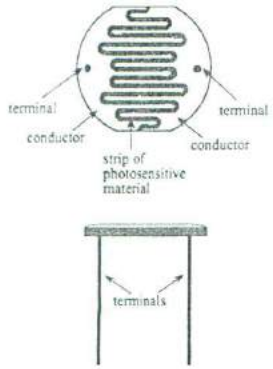
Practise Problems

20-3.1 Calculate the total power supplied to a $3\frac{1}{2}$ digit *LCD* display indicating 1999. The supply is a square wave with an 8 V peak level, and the current to each segment is 5 μA.

20-4 Photoconductive Cell

Cell Construction

Light striking the surface of a material can provide sufficient energy to cause electrons within the material to break away from their atoms. Thus, free electrons and holes (*charge carriers*) are created within the material, and consequently its resistance is reduced. This is known as the *photoconductive effect*.



(a) Photoconductive cell construction

(b) Circuit symbol

Figure 20-10
A photoconductive cell consists of a strip of light-sensitive material situated between two conductors.

The construction of a typical photoconductive cell is illustrated in Fig. 20-10(a), and the graphic symbol is shown in Fig. 20-10(b). Light-sensitive material is arranged in the form of a long strip zigzagged across a disc-shaped base. The connecting terminals are fitted to the conducting material on each side of the strip; they are *not* at the ends of the strip. Thus, the light sensitive material is actually a short, wide strip between the two conductors. For added protection, a transparent plastic cover is usually included.

Cadmium sulfide (*CdS*) and cadmium selenide (*CdSe*) are the two materials normally used in photoconductive cell manufacture. Both respond rather slowly to changes in light intensity. For cadmium selenide, the response time (t_{res}) is around 10 ms, while for cadmium sulfide it may be as long as 100 ms. Temperature sensitivity is another important difference between the two materials. There is a large change in the resistance of a cadmium selenide cell with changes in ambient temperature, but the resistance of cadmium sulfide remains relatively stable. As with all other devices, care must be taken to ensure that the power dissipation is not excessive. The *spectral response* of a cadmium sulfide cell is similar to that of the human eye: it responds to visible light. For a cadmium selenide cell, the spectral response is at the longer wavelength end of the visible spectrum and extends into the infrared region.

Characteristics and Parameters

Typical illumination characteristic for a photoconductive cell are shown in Fig. 20-11. It is seen that, when the cell is not illuminated its resistance can be greater than 100 kΩ. This is known as the *dark resistance* of the cell. When the cell is illuminated, its resistance might fall to a few hundred ohms. Note that the scales on the illumination characteristic are logarithmic.

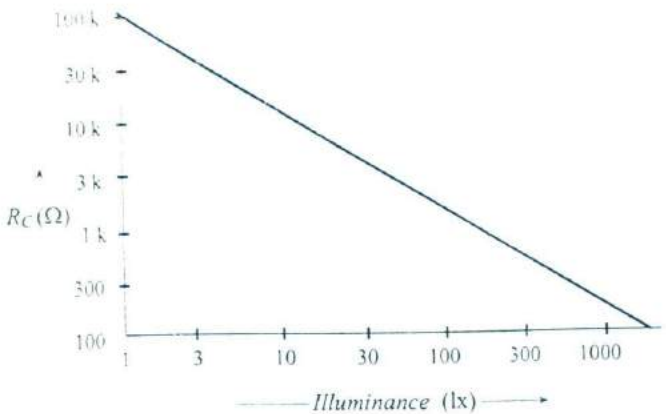


Figure 20-11
Typical photoconductive cell illumination characteristics. The resistance is usually very high when the cell is dark, and relatively low when illuminated.

Typical Photoconductive Cell Specification

PD (mW)	Max ac (V)	Dark Resistance	λP (nm)	Resistance at 10 lx
200	180	100 kΩ	550	6 kΩ (min) 18 kΩ (max)

Figure 20-12
Partial specification for a typical photoconductive cell.

A typical photoconductive cell specification is shown in Fig. 20-12. As well as maximum voltage and power dissipation, the cell dark resistance and the resistance at a 10 lx illumination is listed. Note the wide range of cell resistance at a 10 lx. The light wavelength that gives peak response (λP) is also given on the

specification. Cell *sensitivity* is sometimes used, and this is simply the cell current for a given voltage and given level of illumination.

Applications

Figure 20-13 shows a photoconductive cell used for relay control. When the cell is illuminated, its resistance is low and the relay current is at its maximum. Thus, the relay is energized. When the cell is dark, its high resistance keeps the current down to a level too low to energize the relay. Resistance R_1 is included to limit the relay current to the desired level when the cell resistance is low.

Example 20-5

A relay is to be controlled by a photoconductive cell as in Fig. 20-13. The cell has the characteristics shown in Fig. 20-11. The relay is to be supplied with 10 mA from a 30 V supply when the cell is illuminated with about 200 lm/m^2. Calculate the required series resistance and the level of the dark current. Assume that the coil resistance is much smaller than R_1 and R_C.

Solution

From the characteristics; at 200 lm/m^2, $R_C \approx 1\ \text{k}\Omega$

When the cell is illuminated,

$$I = \frac{E}{R_1 + R_C}$$

or,
$$R_1 = \frac{E}{I} - R_C = \frac{30\ \text{V}}{10\ \text{mA}} - 1\ \text{k}\Omega$$
$$= 2\ \text{k}\Omega \text{ (use } 1.8\ \text{k}\Omega \text{ standard value)}$$

From the characteristics;

when dark, $R_C \approx 100\ \text{k}\Omega$

dark current,
$$I = \frac{E}{R_1 + R_C} = \frac{30\ \text{V}}{1.8\ \text{k}\Omega + 100\ \text{k}\Omega}$$
$$\approx 0.3\ \text{mA}$$

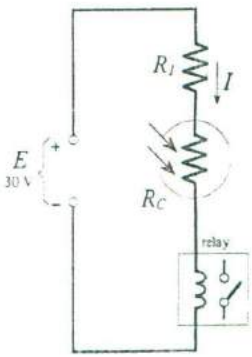


Figure 20-13
Circuit of a relay controlled by a photoconductive cell. The relay is energized when the cell is illuminated.

Photoconductive cells employed to switch transistors *on* and *off* are shown in Fig. 20-14. When cell in Fig. 20-14(a) is dark, the cell resistance (R_C) is high. Consequently, the transistor base is biased above its emitter voltage level, and Q_1 is turned *on*. When the cell is illuminated, its resistance is reduced, and the lower cell resistance in series with R_1 biases the transistor base below its emitter voltage level. Thus, Q_1 is turned *off* when the cell is illuminated.

In Fig. 20-14(b), Q_1 is biased *off* when the cell is dark, because R_C is high. When illuminated, the reduced cell resistance causes Q_1 to be biased *on*.

Example 20-6

The transistor in Fig. 20-14(a) is to be biased *on* when the photoconductive cell is dark, and *off* when it is illuminated. The supply is ±6 V, and the transistor base current is to be 200 μA when *on*. Design the circuit using the photoconductive cell characteristics in Fig. 20-11. Also, determine the minimum light level when the transistor is *off*.

Solution

when dark, $R_C \approx 100\ \text{k}\Omega$

when Q_1 is *on*,

$$V_{RC} = V_{EE} + V_{BE} = 6\ \text{V} + 0.7\ \text{V}$$
$$= 6.7\ \text{V}$$

$$I_{RC} = \frac{V_{RC}}{R_C} = \frac{6.7\ \text{V}}{100\ \text{k}\Omega}$$
$$= 67\ \mu\text{A}$$

$$I_{R1} = I_{RC} + I_B = 67\ \mu\text{A} + 200\ \mu\text{A}$$
$$= 267\ \mu\text{A}$$

$$V_{R1} = V_{CC} - V_B = 6\ \text{V} - 0.7\ \text{V}$$
$$= 5.3\ \text{V}$$

$$R_1 = \frac{V_{R1}}{I_{R1}} = \frac{5.3\ \text{V}}{267\ \mu\text{A}}$$
$$\approx 20\ \text{k}\Omega\ \text{(use 18 k}\Omega\ \text{standard value)}$$

when Q_1 is *off*, $V_{R1} \geq 6\ \text{V}$

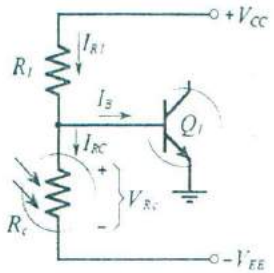
and,

$$I_{R1} = \frac{V_{R1}}{R_1} = \frac{6\ \text{V}}{18\ \text{k}\Omega}$$
$$= 333\ \mu\text{A}$$

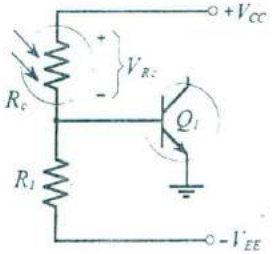
$$R_c = \frac{V_{RC}}{I_{R1}} = \frac{6\ \text{V}}{333\ \mu\text{A}}$$
$$= 18\ \text{k}\Omega$$

From the characteristics;

when $R_C \approx 18\ \text{k}\Omega$, illumination $\approx 7\ \text{lm/m}^2$



(a) Circuit to switch a *BJT off* when a cell is illuminated



(b) Circuit to switch a *BJT on* when a cell is illuminated

Figure 20-14
BJTs controlled by photoconductive cells. The position of the cell in the circuit determines whether the transistor is switched on or off by an increase in illuminance.

Figure 20-15 shows a photoconductive cell used with an op-amp Schmitt trigger circuit (see Section 14-10). When the cell resistance is low (cell illuminated), the voltage across R_1 is higher than the upper trigger point (*UTP*) for the Schmitt. Consequently, the op-amp output is *low* (negative). The output switches to a *high* (positive) level when V_{R1} falls to the Schmitt circuit lower trigger point (*LTP*). This occurs when the cell illumination level falls, causing R_C to rise.

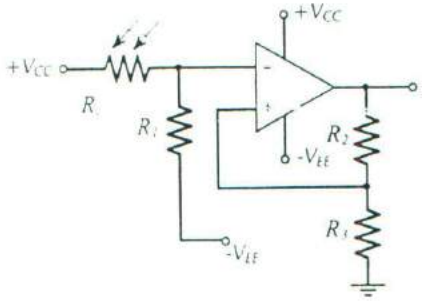


Figure 20-15
Op-amp Schmitt trigger circuit with a photo-conductive cell for light level detection.

The circuit in Fig. 20-16 uses a photoconductive cell to control the current level in an *LED*. The *LED* current is low when the ambient light level is low, because the cell resistance is high. The *LED* current is increased as a result of the decreased resistance of R_C when the ambient light level is high. This increased current gives greater *LED* brightness so that it can be easily seen.

Example 20-7

Design the circuit in Fig. 20-16 for a *LED* current of $I_F \approx 10$ mA at $R_C = 5$ kΩ (light level H_1), and for $I_F \approx 20$ mA at $R_C = 1$ kΩ (light level H_2).

Solution

at H_1,
$$V_{B1} = \frac{V_{CC} \times R_2}{R_{C1} + R_2} = \frac{V_{CC} \times R_2}{5\ \text{k}\Omega + R_2}$$

at H_2,
$$V_{B2} = \frac{V_{CC} \times R_2}{R_{C2} + R_2} = \frac{V_{CC} \times R_2}{1\ \text{k}\Omega + R_2} = 2\,V_{B1}$$

so,
$$\frac{V_{CC} \times R_2}{1\ \text{k}\Omega + R_2} = \frac{2\,V_{CC} \times R_2}{5\ \text{k}\Omega + R_2}$$

giving,
$$R_2 = 3\ \text{k}\Omega \text{ (use 2.2 k}\Omega + 2\ \text{k}\Omega \text{ variable)}$$

$$V_{B1} = \frac{V_{CC} \times R_2}{R_{C1} + R_2} = \frac{12\ \text{V} \times 3\ \text{k}\Omega}{5\ \text{k}\Omega + 3\ \text{k}\Omega}$$
$$= 4.5\ \text{V}$$

$$V_{B2} = 2\,V_{B1} = 9\ \text{V}$$

For $I_C = 10$ mA,
$$R_3 \approx \frac{V_{B1} - V_{BE}}{I_C} = \frac{4.5\ \text{V} - 0.7\ \text{V}}{10\ \text{mA}}$$
$$= 380\ \Omega \text{ (use 390 } \Omega \text{ standard value)}$$

at H_2,
$$I_C \approx \frac{V_{B2} - V_{BE}}{R_3} = \frac{9\ \text{V} - 0.7\ \text{V}}{390\ \Omega}$$
$$= 21.3\ \text{mA}$$

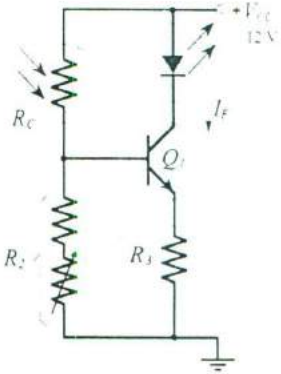


Figure 20-16
Photo-conductive cell circuit for controlling LED current level.

Practise Problems

20-4.1 A relay control circuit as in Fig. 20-13 has $R_1 = 3.3\ k\Omega$, $E = 9\ V$, and a photoconductive cell with the specification in Fig. 20-12. Calculate the maximum and minimum circuit current at a luminous intensity of 10 lx. Also, determine the current at 30 lx, if the cell has the characteristics in Fig. 20-11.

20-4.2 The circuit in Fig. 20-14(b) has $V_{CC} = +12\ V$ and $V_{EE} = -9\ V$. The photoconductive cell has the characteristics in Fig. 20-11. Calculate the R_1 resistance to have Q_1 *on* at a 3 lx illuminance if $I_{B1} \approx 100\ \mu A$.

20-4.3 The op-amp circuit in Fig. 20-15 has $V_{CC} = \pm 15\ V$, $R_1 = 5.6\ k\Omega$, $R_2 = 18\ k\Omega$, and $R_3 = 120\ k\Omega$. The cell characteristics are those in Fig 20-11. Estimate the light levels that cause the output to switch.

20-5 Photodiode and Solar Cell

Photodiode Operation

When a *pn*-junction is reverse biased, a small reverse saturation current flows due to thermally generated holes and electrons being swept across the junction as minority charge carriers, (see Section 1-6). Increasing the junction temperature generates more hole-electron pairs, and so the minority carrier (reverse) current is increased. The same effect occurs if the junction is illuminated, (see Fig. 20-17). Hole-electron pairs are generated by the incident light energy, and minority charge carriers are swept across the junction to produce a reverse current flow. Increasing the junction illumination increases the number of charge carriers generated, and thus increases the level of reverse current. Diodes designed to be sensitive to illumination are known as *photodiodes*.

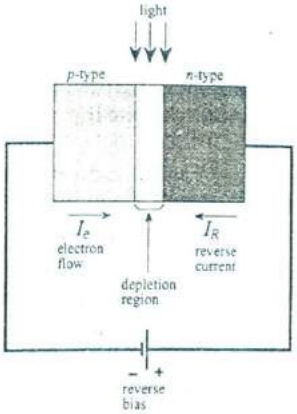


Figure 20-17
A photo-diode has a reverse-biased pn-junction designed to be light sensitive. A minority charge carrier current flows when the junction is illuminated.

Characteristics

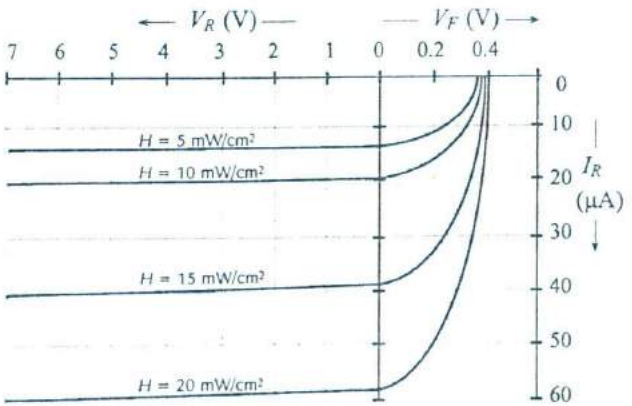


Figure 20-18
Typical photodiode characteristics. The reverse current remains substantially constant for each level of illumination.

Consider the typical photodiode illumination characteristics in Fig. 20-18. When the junction is dark, the *dark current* (I_D) would seem to be zero. Typically, I_D is around 2 nA. A 20 mW/cm² illumination

level produces a reverse current of approximately 60 μA. Increasing the reverse voltage does not increase I_R significantly. So, each characteristic is approximately a horizontal line.

Figure 20-19 shows a simple photodiode circuit using a 2 V reverse bias. (Note the device circuit symbol.) Assuming that D_1 has the characteristics in Fig. 20-18, the current at a 5 mW/cm² illumination level is approximately 13 μA. At 20 mW/cm² the diode current is around 60 μA. The device resistance at each illumination level is readily calculated: (at a 5 mW/cm², R = 2 V/13 μA = 154 kΩ), (at a 20 mW/cm², R = 2 V/60 μA = 33 kΩ). The resistance changed by a factor of approximately 5 from the low to the high illumination level, showing that a photodiode can be employed as a photoconductive device.

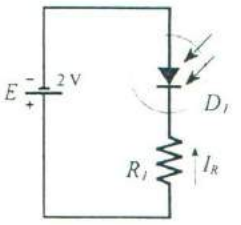


Figure 20-19
Photodiode circuit with a reverse bias voltage.

When the reverse-bias voltage across a photodiode is removed, minority charge carriers continue to be swept across the junction while the diode is illuminated. With an external circuit connected across the diode terminals, the minority carriers flow back to their original sides. The electrons that crossed the junction from *p* to *n* will now flow out through the *n*-terminal and into the *p*-terminal. This means that the device is behaving as a voltage cell, with the *n*-side being the negative terminal and the *p*-side the positive terminal, as illustrated in Fig. 20-20. In fact, a voltage can be measured at the photodiode terminal, positive on the *p*-side and negative on the *n*-side. So, the photodiode is a photovoltaic device as well as a photoconductive device. The characteristics in Figure 20-18 show that, when illuminated, the photodiode actually has to be forward biased to reduce the reverse current to zero.

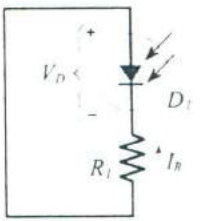


Figure 20-20
An illuminated photodiode without an external bias operates as a photovoltaic device.

It should be noted that V_R and V_F have different scales on the photodiode characteristics shown in Fig. 20-18. A *dc* load line that crosses between the forward and reverse biased regions cannot be drawn on these characteristics. Equal scales must be used for each part of the characteristics to draw such a load line.

Specification

A partial specification for a typical photodiode is shown in Fig. 20-21. The *light current* (I_L) is listed as 10 μA at an illumination level of 5 mW/cm² when the reverse bias is 2 V. This is sometimes defined as a *short-circuit current* (I_{SC}). The *dark current* (I_D) is specified as 2 nA maximum when the reverse voltage is 20 V, and the *open-circuit terminal voltage* (V_{OC}) is given as 350 mV. Note that the typical response time (t_{res}) of 2 ns for a photodiode is very much superior to that for a photoconductive cell. The diode *sensitivity* (S) is the change in diode current produced by a given change in light intensity. The power dissipation, reverse breakdown voltage, and peak output wavelength are also listed.

Typical Photodiode Specification

PD	V_{OC}	$BV_{R(max)}$	$I_{D(max)}$ (dark)	I_L [V_R = 2 V, H = 5 mW/cm²]	t_{res}	S	λP
100 mW	350 mV	100 V	2 nA	10 μA	2 ns	7 μA/mW/cm²	900 nm

Figure 20-21
Partial specification for a low-current photodiode.

Construction

Figure 20-22(a) shows the cross-section of a diffused photo diode. It is seen that a thin heavily-doped *p*-type layer is situated at the top where it is exposed to incident light. The junction depletion region penetrates deeply into the lightly-doped *n*-type layer. This is in contact with a lower heavily-doped *n*-type layer which connects to a metal film contact. A ring-shaped contact is provided at the top of the *p*-type layer. Low-current photodiodes (also called *signal photodiodes*) are usually contained in a *TO*-type can with a lens at the top. [see Fig. 20-22(b)]. Clear plastic encapsulation is also used. [Fig. 20-22(c)].

(a) Cross-section (b) *TO* can-type package (c) Clear plastic encapsulation

Figure 20-22
Photodiode cross-section and typical packages.

Photodiode Applications

Photodiodes can be used as photoconductive devices in the type of circuits discussed in Section 20-4. They can also be used in circuits where they function as photovoltaic devices. Figure 20-23 shows typical photodiode characteristics plotted in the first and second quadrants for convenience. When the device is operated with a reverse voltage, it functions as a photoconductive device. When operating without the reverse voltage, it operates as a photovoltaic device. In some circuits the photodiode can change between the photoconductive mode and the photovoltaic mode.

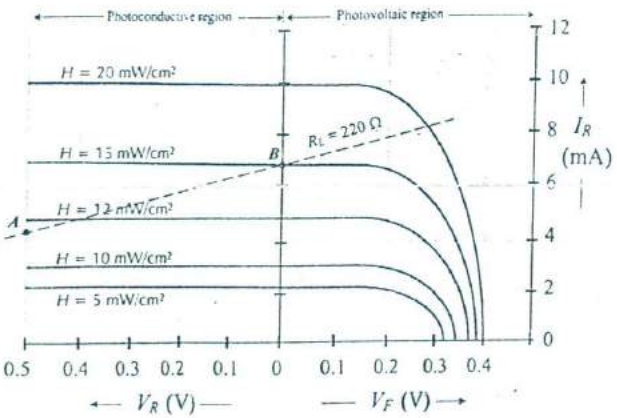


Figure 20-23
Photodiode characteristics have a photoconductive region and a photovoltaic region.

Example 20-8

The circuit in Fig. 20-24 uses a photodiode with the illumination characteristics in Fig. 20-23. Draw the *dc* load line, and determine the diode currents and voltages at light levels of 12, 15 and 20 mW/cm².

Solution

when $V_D = 0.5$ V, $V_{R1} = E - V_D = 1.5\text{ V} - 0.5\text{ V}$

$$= 1\text{ V}$$

$$I_D = \frac{V_{R1}}{R_1} = \frac{1\text{ V}}{220\ \Omega}$$

$$\approx 4.5\text{ mA}$$

Plot point *A* on the characteristics at $I_D = 4.5$ mA and $V_D = 0.5$ V

when $V_D = 0$, $V_{R1} = E = 1.5$ V

so, $$I_D = \frac{E}{R_1} = \frac{1.5\text{ V}}{220\ \Omega}$$

$$= 6.8\text{ mA}$$

Plot point *B* on the characteristics at $V_D = 0$ and $I_D = 6.8$ mA

Draw the dc load line through points *A* and *B*.

From the load line:

at 12 mW/cm², $I_D \approx -5$ mA, $V_D \approx -0.4$ V

at 15 mW/cm², $I_D \approx -6.8$ mA, $V_D \approx 0$ V

at 20 mW/cm², $I_D \approx -8$ mA, $V_D \approx +0.28$ V

Note the V_D polarity change at the highest illumination level.

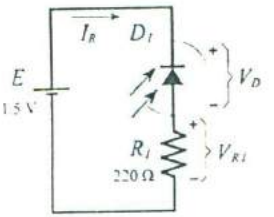


Figure 20-24
Photodiode with a reverse bias and a load resistor.

Solar Cells

The *solar cell*, or *solar energy converter*, is essentially a large photodiode designed to operate solely as a photovoltaic device and to give as much output power as possible. To provide maximum output current, solar cell surface areas are much larger than those of signal photodiodes. Typical solar cell output characteristics are illustrated in Fig. 20-25. Consider the characteristic for a 100 mW/cm² illumination level. If the cell is short-circuited, the output current (I_o) is 50 mA. Because the cell voltage (V_o) is zero at this point, the output power (P_o) is zero. Open-circuiting the cell gives $V_o = 0.55$ V, but $I_o = 0$. So, P_o is again zero. At the *knee* of the characteristic $V_o \approx 0.44$ V and $I_o \approx 45$ mA; giving $P_o \approx 20$ mW. Therefore, for maximum output power, the device must be operated on the knee of the characteristic. As in the case of all other devices, the power must be derated at high temperatures.

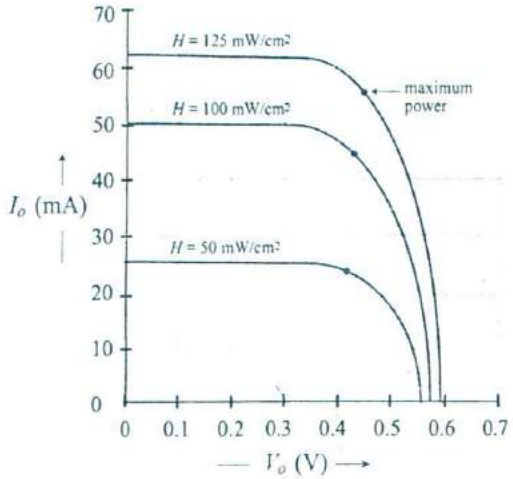


Figure 20-25
Typical solar cell characteristics. The device must be operated at the knee of its characteristic for maximum output power.

Figure 20-26 shows a group of series-parallel connected solar cells operating as a battery charger. Several cells must be series connected to produce the required output voltage, and several of these series-connected groups must be connected in parallel to provide the necessary output current.

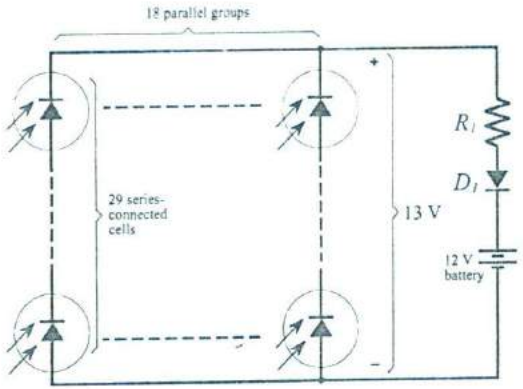


Figure 20-26
Series-parallel arrangement of solar cells connected to function as a solar battery charger.

Example 20-9

An earth satellite has 12 V batteries that supply a continuous current of 0.5 A. Solar cells with the characteristics shown in Fig. 20-25 are employed to keep the batteries charged. If the illumination from the sun for 12 hours in every 24 is 125 mW/cm², determine approximately the total number of cells required.

Solution

From Fig. 20-25, maximum output power at 125 mW/cm² is achieved when each cell is operated at approximately $V_o = 0.45$ V and $I_o = 57$ mA.

Allowing for the voltage drop across the rectifier, a maximum charging voltage of approximately $V_{CH} = 13$ V is required.

Number of series-connected cells,

$$N_S = \frac{V_{CH}}{V_\sigma/\text{cell}} = \frac{13\text{ V}}{0.45\text{ V}}$$
$$\approx 29$$

The charge taken from the batteries over a 24-hour period is

$$Q = I_L \times t = 0.5\text{ A} \times 24\text{ hours}$$
$$= 12\text{ Ah}$$

So, the charge delivered by the solar cells must be 12 Ah.

The solar cells deliver current only while they are illuminated; that is, for 12 hours in every 24. Therefore, the charging current from the solar cells is,

$$I_{CH} = \frac{Q}{t} = \frac{12\text{ Ah}}{12\text{ h}}$$
$$= 1\text{ A}$$

Number of parallel-connected groups of cells,

$$N_P = \frac{I_{CH}}{I_\sigma/\text{cell}} = \frac{1\text{ A}}{57\text{ mA}}$$
$$\approx 18$$

The total number of cells required,

$$N_T = N_P \times N_S = 18 \times 29$$
$$= 522$$

Practise Problems

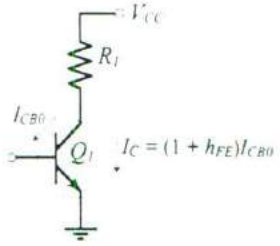
20-5.1 A photodiode with the characteristics in Fig. 20-23 is connected in series with a 330 Ω resistor and a (reverse-biasing) 3 V battery. Draw the *dc* load line for the circuit, and determine the diode voltage at an illumination level of 20 mW/cm².

20-5.2 A solar voltage source is to be designed to produce a 3 V, 20 mA output from a 15 mW/cm² illumination level. Calculate the required number of cells if the available devices have the characteristics shown in Fig. 20-23.

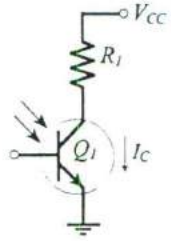
20-6 Phototransistors

Phototransistor (BJT)

A *phototransistor* is similar to an ordinary *BJT*, except that its collector-base junction is constructed like a photodiode. Instead of a base current, the input to the transistor is in the form of illumination at the junction. Consider an ordinary *BJT* with its



(a) *BJT* currents with open-circuited base



(b) Phototransistor circuit

Figure 20-27
In a phototransistor, the collector current depends upon the level of illumination at the CB junction.

base terminal open-circuited, [Fig. 20-27(a)]. The collector-base leakage current (I_{CBO}) acts as a base current, giving a collector current; $I_C = (h_{FE} + 1)\, I_{CBO}$. In the case of the photodiode, it was shown that the reverse saturation current is increased by the light energy at the junction. Similarly, in the phototransistor I_{CBO} is proportional to the collector-base illumination, [Fig. 20-27(b)]. This results in I_C also being proportional to the illumination level.

For a given amount of illumination on a very small area, the phototransistor provides a much larger output current than that available from a photodiode. Thus, the phototransistor is the most sensitive of the two devices. The phototransistor circuit symbol shows a base terminal, and this is often left unconnected, but is sometime used to provide stable bias conditions.

The cross-section in Fig. 20-28 illustrates the construction of a phototransistor. The emitter area is seen to be quite small, to allow incident illumination to pass to the collector-base junction. Phototransistor packages are similar to the photodiode packages in Fig. 20-22, except that three terminals are provided.

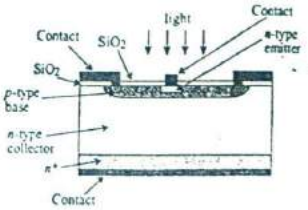


Figure 20-28
Phototransistor cross-section.

Characteristics and Specification

Typical phototransistor output characteristics are shown in Fig. 20-29. These are seen to be similar to *BJT* characteristics except that the base current levels are replaced with illumination levels. A *dc* load line can be drawn on the characteristics in the usual way.

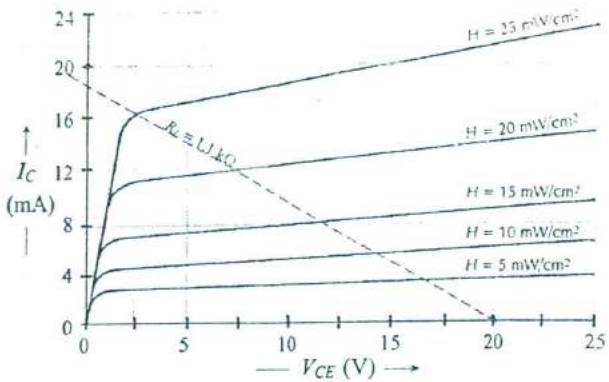


Figure 20-29
The output characteristics for a phototransistor are similar to those of an ordinary BJT except that base current level is replaced by illumination level.

Typical Phototransistor Specification

P_D	$V_{CE(max)}$	$I_{CEO(max)}$ (dark) [V_{CE} = 10 V]	$I_{C(min)}$ [V_{CE} = 5 V] [H = 5 mW/cm²]	t_r	t_f [I_{CE} = 1 mA]	S [H = 5 mW/cm²]	λP (nm)
200 mW	40 V	100 nA	3 mA	5 µs	8 µs	500 µA/mW/cm²	900 nm

Figure 20-30
Partial specification for a phototransistor.

The partial specification for a phototransistor in Fig. 20-30 shows a 3 mA minimum current at 5 mW/cm², and a sensitivity of 500 µA/mW/cm². Comparing this to the photodiode specification

(Fig. 20-21) shows (as stated above) that a phototransistor is very much more sensitive than a photodiode. However, the rise and fall times (typically 5 μs and 8 μs) for a phototransistor are very much slower than the 2 ns response time for a photodiode.

Applications

Two phototransistor applications are shown in Fig. 20-31 and 20-32. The relay in Fig. 20-31 is energized when the incident light on the phototransistor is raised to a particular level. This occurs when the Q_1 emitter current produces sufficient voltage drop across R_2 to forward bias the *BE* junction of Q_2. The relay current falls again when Q_2 turns *off* as the light level decreases.

In Fig. 20-32, SCR_1 remains untriggered while the illumination keeps Q_1 in saturation. If the light fails, Q_1 turns *off* and V_{R3} triggers the *SCR on*. This kind of circuit can be used to switch *on* an emergency lighting system when the normal lighting fails.

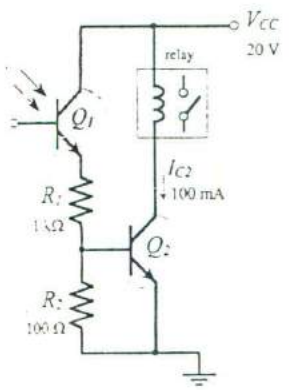


Figure 20-31
Use of a phototransistor to energize a relay when the illumination increases to a predetermined level.

Example 20-10

Transistor Q_1 in the circuit in Fig. 20-31 has the characteristics in Fig. 20-29, and Q_2 has $h_{fl} = 80$. Determine the light level required to energize the relay.

Solution

when Q_2 is *on*, $V_{B2} = V_{BE2} = 0.7$ V

$$I_{R2} = \frac{V_{R2}}{R_2} = \frac{0.7\text{ V}}{100\ \Omega}$$

$$= 7\text{ mA}$$

$$I_{B2} = \frac{I_{C2}}{h_{fl}} = \frac{100\text{ mA}}{80}$$

$$= 1.25\text{ mA}$$

$$I_{E1} = I_{B2} + I_{R2} = 1.25\text{ mA} + 7\text{ mA}$$

$$= 8.25\text{ mA}$$

The *dc* load resistance for Q_1 is,

$$R_l = R_1 + R_2 = 1\text{ k}\Omega + 100\ \Omega$$

$$= 1.1\text{ k}\Omega.$$

Draw the *dc* load line on the characteristics for $R_l = 1.1$ kΩ

At $I_C = 8.25$ mA on the load line,

$$H \approx 15\text{ mW/cm}^2$$

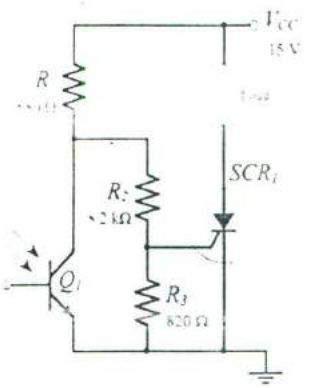


Figure 20-32
Phototransistor circuit for triggering an SCR at low light levels.

Photodarlington

The photodarlington (Fig. 20-33) consists of a phototransistor connected in Darlington arrangement with another transistor. This device is capable of producing much higher output currents

than a phototransistor, and so it has a greater sensitivity to illumination levels than either a phototransistor or a photodiode. With the additional transistor involved, the photodarlington has a considerably longer switching time than a phototransistor.

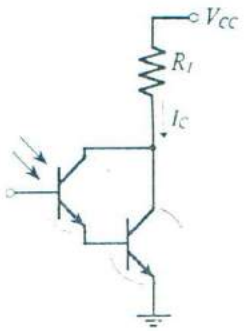
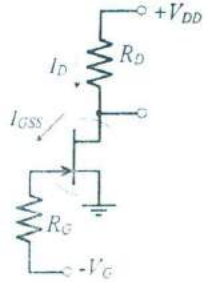


Figure 20-33
A photodarlington is made up of a phototransistor connected in Darlington with another BJT.

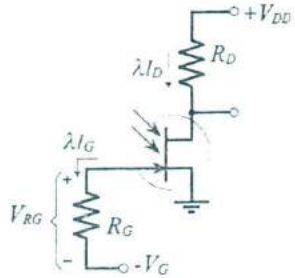
PhotoFET

A *photoFET* is a *JFET* designed to have its gate-channel junction illuminated. The illumination controls the level of the device drain current. Consider the *n*-channel *JFET* and the *photoFET* in Fig. 20-34. The gate-source leakage current (I_{GSS}) is the reverse saturation current at a *pn*-junction. The voltage drop across R_G produced by I_{GSS} is normally too small to affect the *JFET* circuit. In the *photoFET*, the junction reverse current (λI_G) is susceptible to light. Illumination on the junction generates additional minority charge carriers, thus increasing λI_G. This current flows through the bias resistance (R_G) and produces a voltage drop (V_{RG}), as illustrated. If the gate bias voltage ($-V_G$) is just sufficient to bias the device *off* when dark, then when the junction is illuminated, V_{RG} can raise the level of the gate voltage to bias the *photoFET on*.

The external bias voltage ($-V_G$) might be selected at a level that biases the device *on*, so that light level variations cause I_D to increase and decrease. In a *photoFET*, λI_G is termed the *gate current*, and the normal I_{GSS} at the junction is the *dark gate-leakage current*. The light-controlled drain current is designated λI_D.



(a) *JFET* circuit



(b) *PhotoFET* circuit

Figure 20-34
In a photoFET, the gate-channel leakage current depends upon the illumination level. This current produces a voltage drop across the bias resistor to control the gate-source voltage.

Practise Problems

20-6.1 A phototransistor with the characteristics in Fig. 20-29 is connected in series with a resistor $R_1 = 820\ \Omega$ and $V_{CC} = 18$ V. Determine V_{R1} at 5 mW/cm² and 25 mW/cm² illumination levels.

20-6.2 The *SCR* in Fig. 20-32 triggers at $V_G = 0.8$ V and $I_G = 100\ \mu$A. Determine the approximate light level to trigger the *SCR on* if Q_1 has the characteristics in Fig. 20-29.

20-7 Optocouplers

Operation and Construction

An *optocoupler* (*optoelectronic coupler*) is essentially a phototransistor and an *LED* combined in one package. Figure 20-35(a) and (b) shows the typical circuit and terminal arrangement for one such device contained in a *DIL* plastic package. When current flows in the *LED*, the emitted light is directed to the phototransistor, producing current flow in the transistor. The coupler may be operated as a switch, in which case both the *LED* and the phototransistor are normally *off*. A pulse of current through the *LED* causes the transistor to be switched *on* for the duration of the pulse. Linear signal coupling is also possible. Because the coupling is optical, there is a high degree of electrical isolation between the input and output terminals, and so the term *optoisolator* is sometimes used. The output (detector) stage has no

effect on the input, and the electrical isolation allows a low-voltage *dc* source to control high voltage circuits.

The cross-section diagram in Fig. 20-35(c) illustrates the construction of an optocoupler. The emitter and detector are contained in a transparent insulating material that allows the passage of illumination while maintaining electrical isolation.

(a) Optocoupler circuit (b) *DIL* terminals (c) Cross-section

Figure 20-35
An optocoupler is composed of an LED and a phototransistor. The input and output are electrically isolated.

Specification

The partial specification for an optoelectronic coupler in Fig. 20-36 has three parts. The first part specifies the current and voltage conditions for the input (*LED*) stage. The second deals with the output (phototransistor) stage. The third part defines the coupling parameters. The transistor collector current is listed as 5 mA (typical) when its V_{CE} = 10 V and the *LED* has I_F = 10 mA. In this particular case, the ratio of output current to input current is 50%. This is known as the *current transfer ratio* (*CTR*), and for an optoelectronic coupler with a transistor output it can range from 10% to 150%.

Typical Optocoupler Specification

Input Stage

$I_{F(max)}$	$V_{F(max)}$ [I_F = 20 mA]	V_R
60 mA	1.5 V	3 V

Output Stage

$V_{CE(max)}$	$I_{C(max)}$	P_D	$V_{CE(sat)}$	I_{CEO} (dark)
30 V	150 mA	150 mW	0.2 V	50 nA

Coupled

$I_{C(out)}$ [I_F = 10 mA]	$t_{on(max)}$	$t_{off(max)}$	Isolation voltage
5 mA	2.5 μs	4 μs	7500 V

Figure 20-36
The partial specification for an optocoupler is made up of three parts: input, output, and coupling.

Applications

The circuit of an optocoupler in a *dc* or pulse-type coupling application is shown in Fig. 20-37. The diode current is switched *on* and *off* by the action of transistor Q_1 operating from a 24 V supply. Transistor Q_2 is turned *on* into saturation when D_1 is energized. The collector current of Q_2 provides the load (*sinking*) current and the current through resistor R_2. *Pull-up* resistor R_2 is necessary to ensure that the load terminal is held at the 5 V supply level when Q_2 is *off*.

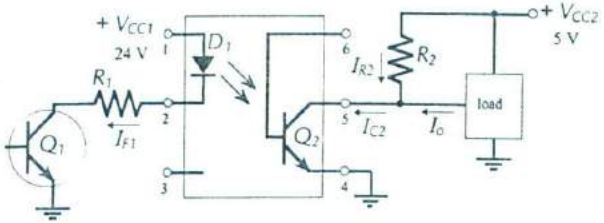


Figure 20-37
Optocoupler used for coupling a signal from a 24 V system to a 5 V system.

Example 20-11

The optocoupler in Fig. 20-37 is required to sink a 2 mA load current when Q_2 is in saturation and $I_{F1} = 10$ mA. The optocoupler has the specification in Fig. 20-36. Determine suitable resistor values.

Solution

From the specification; $I_{C2} = 5$ mA when $I_{FD1} = 10$ mA

$$I_{R2} = I_{C2} - I_o = 5 \text{ mA} - 2 \text{ mA}$$
$$= 3 \text{ mA}$$

$$R_2 = \frac{V_{CC2} - V_{CE(sat)}}{I_{R2}} = \frac{5 \text{ V} - 0.2 \text{ V}}{3 \text{ mA}}$$
$$= 1.6 \text{ k}\Omega \text{ (use } 1.8 \text{ k}\Omega \text{ to ensure } Q_2 \text{ saturation)}$$

$$R_1 = \frac{V_{CC1} - V_{FD1} - V_{CE(sat)}}{I_{FD1}} = \frac{24 \text{ V} - 1.5 \text{ V} - 0.2 \text{ V}}{10 \text{ mA}}$$
$$= 2.23 \text{ k}\Omega \text{ (use } 2.2 \text{ k}\Omega)$$

A linear application of an optocoupler is shown in Fig. 20-38. The 5 V supply provides a *dc* bias current to D_1 via R_2, and the *ac* signal coupled via C_1 and R_1 increases and decreases the diode current. Transistor Q_1 is biased into an *on* state by the direct current through D_1, and its emitter current is increased and decreased by the variation in light level produced by the alternating current in D_1. An output voltage is developed across R_3.

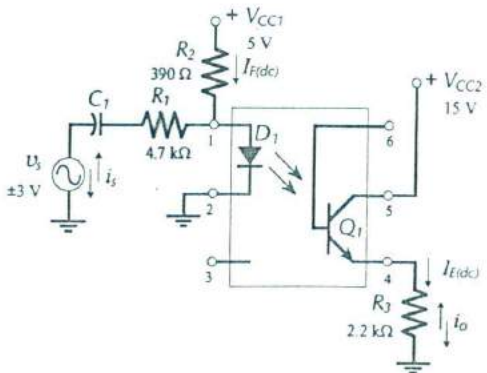
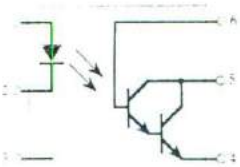


Figure 20-38
Linear signal coupling by means of an optocoupler.

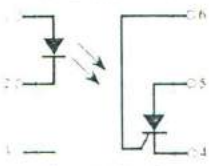
Other Optocouplers

Other types of optocouplers involve different types of output stage. The three types illustrated in Fig. 20-39 are: (a) *Darlington-output* type, (b) *SCR*-output, and (c) *TRIAC*-output. In (a), the photo-darlington output stage provides much higher *CTR* than a *BJT* phototransistor output stage (typically 500%), but it also has a slower response time. The output stages in (b) and (c) are a *light-activated SCR* and a *light-activated TRIAC*, respectively. They are used with the kind of control circuits discussed in Chapter 19, where high electrical isolation between the triggering circuit and the control device is an additional requirement. *CTR* does not apply to *SCR* and *TRIAC* output stages; instead, the *LED* current needed to trigger the thyristor is of interest.

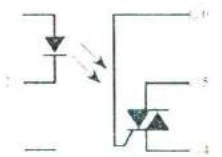
Optocoupler output stages are *not* designed for high load currents. Maximum current levels for Darlington outputs are around 150 mA, and 300 mA is typical for *SCR* and *TRIAC* outputs. When high load currents are to be switched, the optocoupler output stage is used as a trigger circuit for a high power device.



(a) Darlington output



(b) *SCR* output



(c) *TRIAC* output

Figure 20-39
Optocouplers are available with various types of output stage.

Practise Problems

20-7.1 An optocoupler with the specification in Fig. 20-36 is to control a 10 mA relay with a 30 V supply. The input stage is connected via a resistor (R_1) to a 5 V supply. Calculate a suitable resistance for R_1.

20-7.2 Analyze the circuit in Fig. 20-38 to determine the *dc* bias current through D_1, and the *ac* signal current peaks. Also, calculate the maximum and minimum *dc* and *ac* output voltage levels. The optocoupler used has a diode with $V_F = 1.5$ V, and a *CTR* ranging from 20% to 70%.

Chapter-20 Review Questions

Section 20-1

20-1 State measurement units for luminous flux and luminous intensity. Using diagram, explain flux per solid angle.

20-2 Define: Candela, Lumen, and foot candle.

Section 20-2

20-3 Sketch diagrams to show the operation and construction of an *LED*. Briefly explain.

20-4 For an *LED*, state typical values of forward current, forward voltage, reverse breakdown voltage.

20-5 Draw circuit diagrams showing *LEDs* used to indicate (a) a *dc* supply voltage switched *on*, (b) a *high* output level from an op-amp. Explain each circuit.

20-6 The current level in an *LED* is to be controlled by use of a *BJT*. Sketch two possible circuits, and explain the operation of each.

20-7 An op-amp is to be used to control the current level in an *LED*. Draw a suitable circuit diagram and explain its operation.

Section 20-3

20-8 Sketch a seven-segment *LED* display. Explain common-anode and common-cathode connections. State total current requirements for an *LED* four numeral, seven-segment display.

20-9 Using illustrations, explain the operation of liquid-crystal cells. Discuss the difference between reflective-type and transmittive-type cells.

20-10 Sketch a seven-segment *LCD* and show the waveforms involved in controlling the cells. Explain.

Section 20-4

20-11 Sketch the typical construction and illumination characteristics for a photoconductive cell. Explain its operation.

20-12 Draw circuit diagrams to show how a photoconductive cell can be used for: (a) biasing a *pnp* transistor *off* when the cell is illuminated, (b) biasing an *npn* transistor *on* when the cell is illuminated. Explain how each circuit operates.

20-13 Draw circuit diagrams to show a photoconductive cell used for: (a) triggering an op-amp Schmitt trigger circuit, (b) energizing a relay when the cell is illuminated. Explain the operation of each circuit.

Section 20-5

20-14 Sketch the cross-section of a typical photodiode and explain its operation. Sketch typical photodiode characteristics and discuss their shape.

20-15 For photodiode, define; dark current, light current, and sensitivity. State typical values for each quantity.

20-16 Explain how a solar cell differs from a photodiode. Sketch typical solar cell characteristics, and discuss the best operating point on the characteristics.

20-17 Sketch the circuit diagram for an array of solar cells employed as a battery charger. Briefly explain.

Section 20-6

20-18 Sketch characteristics for a phototransistor, and explain how the device operates.

20-19 Draw a circuit diagram to show how a phototransistor can be used to energize a relay when the incident illumination is increased to a given level. Explain the circuit operation.

20-20 Modify the circuit drawn for Question 20-19 to have the relay energized until the illumination is increased to a given level. Explain.

20-21 Draw a circuit diagram for phototransistor control of an *SCR*: to have the *SCR* trigger *on* when the incident illumination falls to a low level. Explain how the circuit operates.

20-22 Sketch a circuit diagram for a photodarlington. Compare the performance of photodarlingtons to phototransistors.

20-23 Sketch a circuit diagram to show the operation of a photo*FET* circuit. Briefly explain the principle of the device.

Section 20-7

20-24 Draw the circuit diagram of an optocoupler with a *BJT* output stage. Also, sketch a cross-section to show the construction of an optocoupler. Explain the device operation.

20-25 Discuss the most important parameters of optocouplers.

20-26 Draw a circuit diagram to show how an optocoupler can use a pulse signal from a low-voltage source to control a circuit with a high-voltage supply, or vice versa. Explain how the circuit operates.

20-27 Draw a circuit diagram to show how an optocoupler can be used to pass a linear signal between two circuits with different supply voltages. Explain how the circuit operates.

20-28 Sketch circuit diagrams for optocouplers with Darlington, *SCR*, and *TRIAC* outputs. Briefly discuss each optocoupler.

Chapter-20 Problems

Section 20-1

20-1 A total luminous flux striking a 4 cm^2 photocell at 7 m from a lamp is to be 80 mlm. Determine the required energy output from the lamp in watts.

20-2. Calculate the total luminous flux striking the surface of a solar cell located 4.5 m from a lamp with a 509 W output. The surface area of the solar cell is 5 cm^2.

20-3 Calculate the frequency of the light output from red, yellow, and green *LEDs* with the following peak wavelengths: 635 nm, 583 nm, 565 nm.

Section 20-2

20-4 An *LED* with I_F = 20 mA current and V_F = 1.4 V is to indicate when a 25 V supply is switched *on*. Sketch a suitable circuit and make all necessary calculations.

20-5 Two series-connected *LEDs* are to be controlled by a *2N3903* transistor with a 12 V supply and V_B = 5 V. The diode current is to be approximately 15 mA. Design a suitable circuit.

20-6 An op-amp Schmitt trigger circuit with V_{CC} = ±15 V is to have the state of its output indicated by *LEDs*. A green *LED* is to indicate *high*, and a red *LED* is to indicate *low*. Design the circuit for 10 mA diode currents. Include reverse-voltage protection diodes in series with each *LED*.

20-7 The *BJT-LED* circuit in Fig. 20-5(a) has: V_B = 5 V, V_{CC} = 20 V, and $h_{FE(min)}$ = 40 for Q_1. Design the circuit to give a 20 mA *LED* current with V_F = 2 V.

Section 20-3

20-8 Calculate the maximum power used by a three-and-a-half digit seven-segment *LED* display with a 5 V supply and 10 mA *LED* currents. Also, determine the power dissipated in each *LED* series resistor, if the *LEDs* have V_F = 1.4 V.

20-9 Determine the maximum power consumed by a three-and-a-half digit seven-segment *LCD* display with a 15 V peak square-wave supply and 1 μA *LCD* segment currents.

Section 20-4

20-10 A *pnp BJT* is to be biased *on* when the level of illumination on a photoconductive cell is greater than 100 lx, and *off* when the cell is dark. A ±5 V supply is to be used, and the *BJT* collector current is to be 10 mA when *on*. Design a suitable circuit to use a *BJT* with h_{FE} = 50 and a photoconductive cell with the characteristics in Fig. 20-11.

20-11 An inverting Schmitt trigger circuit has V_{CC} = ±12 V and *UTP*/*LTP* = ±5 V. The Schmitt output is to switch positively when the illumination level exceeds 30 lx on a photoconductive cell with the characteristics in Fig. 20-11. Design the circuit, and estimate the light level that causes the output to switch negatively.

20-12 A photoconductive cell with the characteristics in Fig. 20-11 is connected in series with an 820 Ω resistor and a 12 V supply. Determine the illumination level when the circuit current is approximately 6.5 mA, and when it is 1.1 mA.

20-13 A photoconductive cell circuit for controlling the current in an *LED* (as in Fig. 20-16) has: V_{CC} = 9 V, R_2 = 3.3 kΩ, R_3 = 270 Ω. The photoconductive cell has a dark resistance of 100 kΩ, and R_C = 3 kΩ at 10 lx. Determine the *LED* current at light levels of 3 lx and 30 lx.

20-14 The circuit in Fig. 20-14(a) has V_{CC} = ±5 V, R_1 = 12 kΩ, and a photoconductive cell with the specification in Fig. 20-12. Calculate the transistor maximum and minimum base voltage at 10 lx.

Section 20-5

20-15 A photodiode with the illumination characteristics in Fig. 20-23 is connected in series with a resistance and a 1 V reverse bias supply. The diode is to produce a +0.2 V output when illuminated with 20 mW/cm^2. Calculate the required series resistance value, and determine the device voltage and current at a 15 mW/cm^2 illumination level.

20-16 A photodiode with the characteristics in Fig. 20-23 is connected in series with a 1.2 V reverse bias supply and a 100 Ω resistance. Determine the resistance offered by the photodiode at illumination levels of 15 mW/cm^2 and 20 mW/cm^2.

20-17 Two photodiodes that each have a 100 Ω series resistor are connected to a 0.5 V reverse bias supply. A voltmeter is connected to measure the voltage difference between the diode cathodes. Assuming that each photodiode has the characteristics illustrated in Fig. 20-23, determine the voltmeter reading when the illumination level is 10 mW/cm^2 on one diode and 15 mW/cm^2 on the other.

20-18 Six photodiodes with the characteristics in Fig. 20-23 are connected in series. Determine the maximum output current and voltage at illumination levels of 15 mW/cm^2 and 12 mW/cm^2.

20-19 A rural telephone system uses 6 V rechargeable batteries which supply an average current of 50 mA. The batteries are recharged from an array of solar cells, each with the characteristics in Fig. 20-25. The average level of sunshine is 50 mW/cm^2 for 10 hours of each 24 hour period. Calculate the number of solar cells required.

20-20 The roof of a house has an area of 200 m^2 and is covered with solar cells which are each 2 cm x 2 cm. If the cells have the output characteristics shown in Fig. 20-25, determine how they should be connected to provide an output voltage of approximately 120 V. Take the average daytime level of illumination as 100 mW/cm^2. If the sun shines for an average of 12 hours in every 24 hours, calculate the energy in kilowatt-hours generated by the solar cells each day.

Section 20-6

20-21 The phototransistor circuit in Fig. 20-27(b) has a 25 V supply, and the device has the output characteristics in Fig. 20-29. Determine the collector resistance required to give V_{CE} = 10 V when the illumination level is 20 mW/cm^2.

20-22 Estimate V_{CE} for the circuit in Problem 20-21 at a 5 mW /cm^2 illumination level. If the phototransistor has the specification in Fig. 20-30, calculate the V_{CE} variation produced by a ±0.5 mW/cm^2 illumination change.

20-23 A phototransistor with the characteristics in Fig. 20-29 is connected in series with a 600 Ω relay coil. The coil current is to be 8 mA when the illumination level is 15 mW/cm^2. Determine the required supply voltage. Also, estimate the coil current at 10 mW/cm^2.

20-24 A phototransistor circuit for controlling an *SCR* (as in Fig. 20-32) is to be designed. The *SCR* has triggering conditions of $V_G = 0.7$ V and $I_G = 50$ μA, and the phototransistor has the specification in Fig. 20-30. Calculate suitable resistor values if the *SCR* is to switch *on* when the light level drops to 5 mW/cm^2. The supply voltage is $V_{CC} = 12$ V.

Section 20-7

20-25 An optocoupler with the specification in Fig. 20-36 is to control a 12 mA load that has a 6 V supply. The input is a 10 V square wave connected via a resistor (R_1). Determine a suitable resistance for R_1.

20-26 A 25 V, 0.5 W lamp is to be switched *on* and *off* by an *BJT* circuit with $V_{CC} = 9$ V and $I_C = 6$ mA. Design a suitable optocoupler circuit and estimate the required *CTR*.

20-27 An optocoupler circuit has its input connected via a 820 Ω resistor (R_1) to a pulse source. Its output transistor has a 5 V collector supply and a 470 Ω emitter resistor (R_2). The gate-cathode terminals of an *SCR* are connected across R_2. The *SCR* requires $V_G = 1.1$ V and $I_G = 500$ μA for triggering. If the optocoupler has *CTR* = 40%, calculate the required amplitude of the pulse input to trigger the *SCR*.

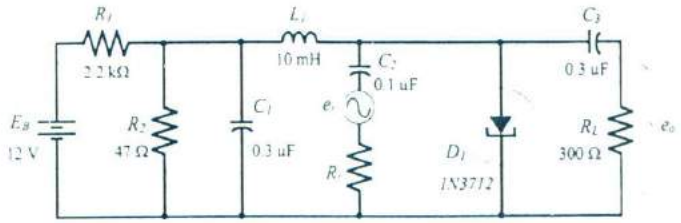
20-28 A optocoupler linear circuit, as in Fig. 20-38, has: $V_{CC1} = 15$ V, $V_{CC2} = 25$ V, $v_s = \pm 0.1$ V, $R_1 = 100$ Ω, $R_2 = 1.2$ kΩ, $R_3 = 1.5$ kΩ. Calculate the *dc* and *ac* output voltages, and the overall voltage gain. The optocoupler has *CTR* = 30%.

20-29 An optocoupler switching circuit, as in Fig. 20-37, has: $V_{CC1} = 18$ V, $V_{CC2} = 3$ V, $R_1 = 1.8$ kΩ, $R_2 = 820$ Ω, and $I_o = 1$ mA. Analyze the circuit to determine I_{F1}, I_{C2}, and *CTR*.

Practise Problem Answers

20-1.1 100 W
20-1.2 5.13×10^{14} Hz
20-1.3 0.73 mlx, 0.29 μlm
20-2.1 220 Ω, 8.4 V
20-2.2 270 Ω, 390 Ω
20-3.1 1.84 mW
20-4.1 422 μA, 968 μA, 1.2 mA
20-4.2 33 kΩ + 2.2 kΩ
20-4.3 30 lx, 15 lx
20-5.1 +0.19 V
20-5.2 48
20-6.1 2.5 V, 13.9 V
20-6.2 13 mW/cm^2
20-7.1 150 Ω
20-7.2 9 mA, ±638 μA, (3.96 V to 13.9 V), (±0.27 V to ±0.98 V)

Chapter 21
Miscellaneous Devices



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Objectives

You will be able to:

1. *Explain the construction and operation of voltage variable capacitor diodes (VVCs).*
2. *Sketch typical VVC voltage/capacitance characteristics, draw the equivalent circuit, and discuss typical VVC parameters.*
3. *Design and analyze resonance circuits using VVCs for frequency tuning.*
4. *Discuss the construction and operation of thermistors, sketch typical thermistor resistance/temperature characteristics, and discuss typical thermistor parameters.*
5. *Calculate thermistor resistance at various temperature levels from the data sheet information.*
6. *Design and analyze circuit using thermistors for temperature level detecting.*
7. *Explain the construction and operation of tunnel diodes.*
8. *Sketch typical forward and reverse characteristics for a tunnel diode, explain their shape, and identify the important points and regions of the characteristics.*
9. *Draw tunnel diode piecewise linear characteristics from data sheet information.*
10. *Design and analyze tunnel diode parallel amplifier circuits.*

Introduction

Three major devices are examined in this chapter: *voltage variable capacitance diodes (VVCs)*, *thermistors*, and *tunnel diodes*. *VVCs* are *pn*-junction devices designed to produce substantial junction capacitance change when the reverse bias voltage is adjusted. They can be applied to tune resonant circuits over a range of frequencies. The resistance of a thermistor changes significantly with change in temperature, so its major application is control of circuits that must respond to temperature change. The tunnel diode is a two-terminal negative-resistance device that can be employed as an oscillator, an amplifier, or a switch.

21-1 Voltage Variable Capacitors

VVC Operation

Voltage-variable capacitor diodes (*VVCs*) are also known as *varicaps*, *varactors*, and as *tuning diodes*. Basically, a *VVC* is a reverse biased diode, and its capacitance is the junction capacitance. Recall that the width of the depletion region at a *pn*-junction depends upon the reverse bias voltage, (Fig. 21-1). A large reverse bias produces a wide depletion region, and a small reverse bias gives a narrow depletion region. The depletion region acts as a dielectric between two conducting plates, so the junction behaves as a capacitor. The depletion layer capacitance (C_{pn}) is proportional to the junction area and inversely proportional to the width of the depletion region. Because the depletion region width is proportional to the reverse bias voltage, C_{pn} is inversely proportional to the reverse bias voltage. This is not a direct proportionality; instead C_{pn} is proportional to $1/V^n$, where V is the reverse bias voltage, and n depends upon doping density.

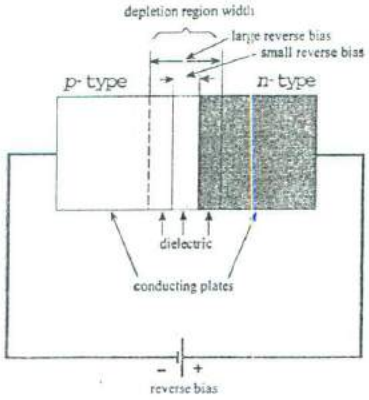
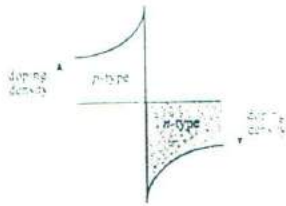


Figure 21-1
A voltage variable capacitance (VVC) is essentially a reverse-biased pn-junction. Increasing the reverse voltage widens the depletion region and reduces the capacitance.

Figure 21-2 shows the doping profiles for two types of *VVC* classified as *abrupt junction* and *hyperabrupt junction* devices. In the abrupt junction *VVC*, the semiconductor material is uniformly doped, and it changes abruptly from *p*-type to *n*-type at the

junction. The hyperabrupt junction device has the doping density increased close to the junction. This increasing density produces a narrower depletion region, and so it results in a larger junction capacitance. It also causes the depletion region width to be more sensitive to bias voltage variations, thus it produces the largest capacitance change for a given voltage variation. *VVCs* are packaged just like ordinary low-current diodes.

(a) Abrupt junction

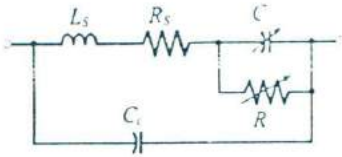


(b) Hyperabrupt junction

Figure 21-2
Doping profiles for abrupt junction and hyperabrupt junction VVCs.

Equivalent Circuit

The complete equivalent circuit for a VVC is shown in Fig. 21-3(a), and a simplified version is given in Fig. 21-3(b). In the complete circuit, the junction capacitance (C_J) is shunted by the junction reverse leakage resistance (R_J). The resistance of the semiconductor material is represented by R_S, the terminal inductance is L_S, and the capacitance of the terminals (or the device package) is C_C. Because L_S is normally very small and R_J is very large, the equivalent circuit can be simplified [Fig 21-3(b)] to R_S in series with C_T, where C_T is the sum of the junction and terminal capacitances, ($C_T = C_J + C_C$). The *Q*-factor for a VVC can be as high as 600 at a 50 MHz frequency. However, *Q*-factor varies with bias voltage and frequency, so it is used only as a figure of merit for comparing the performance of different *VVCs*.



(a) Complete equivalent circuit

(b) Simplified equivalent circuit

Figure 21-3
The complete equivalent circuit of a VVC has five components. The simplified circuit is made up of the semiconductor resistance R_S and the total (junction + terminal) capacitance C_T.

Typical VVC Specification

C_T V_R = 1 V, f = 1 MHz min	C_T V_R = 1 V, f = 1 MHz max	C_1 / C_{10} f = 1 MHz	Q V_R = 1 V, f = 1 MHz	$V_{R(max)}$	$I_{R(max)}$	$I_{F(max)}$
400 pF	600 pF	14	200	15 V	100 nA	200 mA

Figure 21-4
Partial specification for a voltage-variable capacitor diode (VVC).

Specification and Characteristics

A wide selection of nominal *VVC* capacitances is available, ranging approximately from 6 pF to 700 pF. The *capacitance tuning ratio* (*TR*) is the ratio of C_T at a small reverse voltage to C_T at a large reverse voltage. In the partial specification for a *VVC* shown in Fig. 21-4, the tuning ratio is listed as C_1/C_{10}. This is the ratio of the device capacitance at 1 V reverse bias to that at a 10 V reverse bias. Using the 400 pF minimum capacitance (C_T) listed for a 1 V bias, the capacitance is changed to 400 pF/14 when the bias is 10 V. The specification also lists the *Q*-factor, as well as maximum reverse voltage, reverse leakage current, and the maximum forward current that can be passed when the device is forward biased.

A typical graph of capacitance (C_T) versus reverse bias voltage (V_R) for a hyperabrupt junction *VVC* is reproduced in Fig. 21-5 together with the *VVC* circuit symbol. It is seen that C_T varies (approximately) from 500 pF to 25 pF when V_R is changed from 1 V to 10 V. It should be noted from the specification in Fig. 21-4 that the nominal capacitance has a large tolerance (400 pF to 600 pF), and this must be taken into account when using the C_T/V_R graphs.

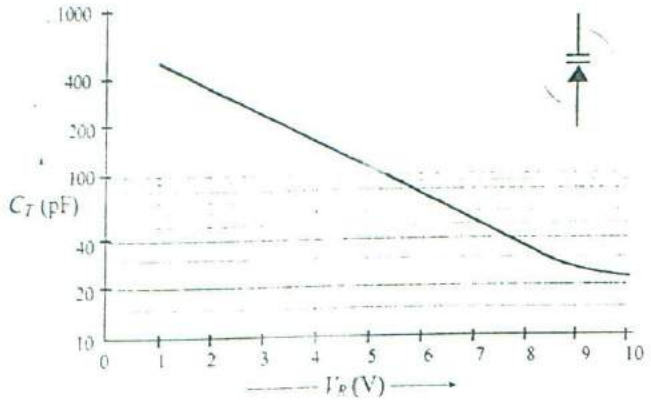


Figure 21-5
Capacitance/voltage characteristics for a hyperabrupt junction VVC.

Applications

The major application of *VVCs* is as tuning capacitors to adjust the frequency of resonance circuits. An example of this is the circuit shown in Fig. 21-6. This is an amplifier with a tuned circuit load. The amplifier produces an output at the resonance frequency of the tuned circuit. The *VVC* provides the capacitance (C_T) of the resonant circuit, and this can be altered by adjusting the diode (reverse) bias voltage (V_D). So, the resonance frequency of the circuit can be varied. C_1 is a coupling capacitor with a capacitance much larger than that of the *VVC*, and R_2 limits the *VVC* forward current in the event that it becomes forward biased.

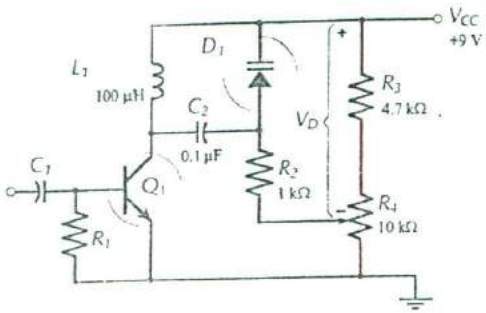


Figure 21-6
Amplifier stage with an LC tank circuit load. The resonance frequency of the LC circuit can be varied by adjusting the VVC reverse bias voltage.

Example 21-1

Determine the maximum and minimum resonance frequency for the circuit in Fig. 21-6. Assume that D_1 has the C_T/V_R characteristic in Fig. 21-5.

Solution

$$V_{D(min)} = \frac{V_{CC} \times R_3}{R_3 + R_4 + R_5} = \frac{9\text{ V} \times 4.7\text{ k}\Omega}{4.7\text{ k}\Omega + 5\text{ k}\Omega + 4.7\text{ k}\Omega}$$
$$= 2.9\text{ V}$$

$$V_{D(max)} = \frac{V_{CC}(R_3 + R_4)}{R_3 + R_4 + R_5} = \frac{9\text{ v} \times (4.7\text{ k}\Omega + 5\text{ k}\Omega)}{4.7\text{ k}\Omega + 5\text{ k}\Omega + 4.7\text{ k}\Omega}$$
$$\approx 6.1\text{ V}$$

From Fig. 21-5, at $V_D = 2.9$ V, $C_T \approx 250$ pF

$$f_{(min)} = \frac{1}{2\pi\sqrt{(L\,C_T)}} = \frac{1}{2\pi\sqrt{(100\,\mu\text{H} \times 250\text{ pF})}}$$
$$\approx 1\text{ MHz}$$

From Fig. 21-5, at $V_D = 6.1$ V, $C_T \approx 70$ pF

$$f_{(min)} = \frac{1}{2\pi\sqrt{(L\,C_T)}} = \frac{1}{2\pi\sqrt{(100\,\mu\text{H} \times 70\text{ pF})}}$$
$$\approx 1.9\text{ MHz}$$

Practise Problems

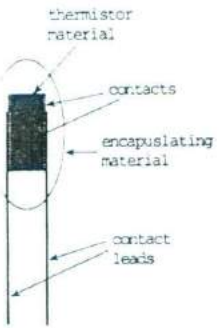
21-1.1 A tuned amplifier circuit as in Fig. 21-6 is to have a resonance frequency adjustable from 1.5 MHz to 2.5 MHz. A 12 V supply is used, the inductor (L_1) is 80 μH, and the *VVC* (D_1) has the characteristics in Fig. 21-5 and the specification in Fig 21-4. Determine suitable resistance values for R_3, R_4, and R_5.

21-2 Thermistors

Thermistor Operation

The word *thermistor* is a combination of thermal and resistor. A thermistor is a resistor with definite thermal characteristics. Most thermistors have a negative temperature coefficient (*NTC*), but positive temperature coefficient (*PTC*) devices are also available. Thermistors are widely applied for measurement and control of temperature, liquid level, gas flow, etc.

Silicon and germanium are not normally used for thermistor manufacture, because larger and more predictable temperature coefficients are available with metallic oxides. Various mixtures of manganese, nickel, cobalt, copper, iron, and uranium are pressed into desired shapes and sintered (or baked) at high temperature to form thermistors. Electrical connections are made either by including fine wires during the shaping process, or by silvering the surfaces after sintering, [see Fig. 21-7(a)]. Thermistors are made in the shape of beads, probes, discs, washers, etc. [Fig. 21-7(b)]. Beads may be glass-coated or enclosed in evacuated or gas-filled glass envelopes for protection against corrosion.



(a) Thermistor construction

(b) Some thermistor shapes

Figure 21-7
Thermistor are resistors that are very sensitive to temperature.

Characteristics and Specifications

The typical thermistor resistance/temperature characteristic in Fig. 21-8 shows that the device resistance (R) decreases substantially when its temperature is raised. At 0°C, $R \approx 1.5\ k\Omega$; and at 60°C, $R \approx 70\ \Omega$. Current flow through a thermistor causes power dissipation that can raise its temperature and change its resistance. This could introduce errors in the thermistor application, so device currents are normally kept to a minimum.

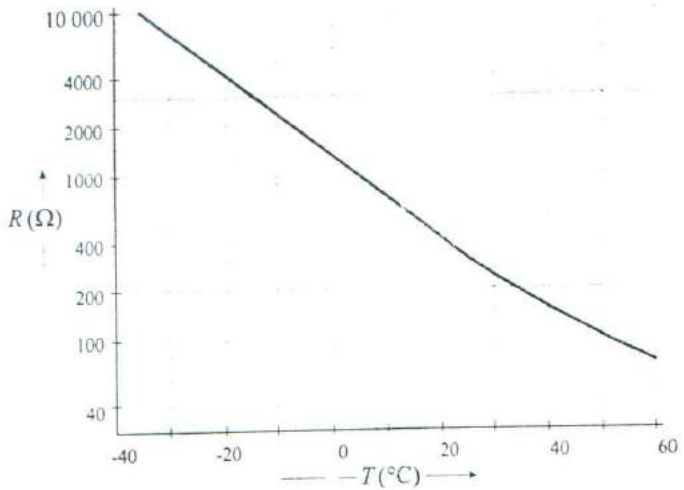


Figure 21-8
Typical resistance/temperature characteristics for a negative temperature coefficient (NTC) thermistor.

Figure 21-9 shows partial specifications for two thermistors with widely differing resistance values. Both devices have the resistance specified at 25°C as the *zero power resistance*. This, of course, means that there must be zero power dissipation in the thermistor to give this resistance value. The *dissipation constant* is the device power dissipation that can raise its temperature through 1°C. The dissipation constant in both cases is specified as *1 mW/°C in still air*, and *8 mW/°C in moving liquid*. Thus, a thermistor located in still air conditions could have its temperature increased by 1°C if it has 1 mW of power dissipation.

Typical Thermistor Specifications

Thermistor	Zero power resistance at 25°C	Resistance ratio 25°C/125°C	β (0 to 50°C)	Maximum working temperature	Dissipation constant
44002A	300 Ω	15.15	3118	100°C	1 mW/°C in still air 8 mW/°C in moving liquid
44008	30 kΩ	29.15	3810	150°C	

Figure 21-9
Partial specifications for two thermistors, one with a 300 Ω 25°C resistance, and the other with a 30 kΩ 25°C resistance.

An indication of how much the thermistor resistance changes is given by the *resistance ratio at 25/125°C*. Clearly, with this ratio specified as 15.15, the resistance at 25°C is divided by 15.15 to determine the resistance at 125°C. Note that both devices have

maximum working temperatures listed. The resistance change with temperature is also defined by the constant *Beta* (β), this time for the range 0°C to 50°C. This constant is used in an equation that relates resistance values at different temperatures:

$$\ln \frac{R_1}{R_2} = \beta \left(\frac{1}{T_1} - \frac{1}{T_2}\right) \qquad \textbf{(21-1)}$$

In Eq. 21-1, R_1 is the resistance at temperature T_1, and R_2 is the resistance T_2. It is important to note that T_1 and T_2 are *absolute* (or *Kelvin*) temperature values, (°C + 273) K.

Example 21-2

Calculate the resistance of the 300 Ω thermistor specified in Fig. 21-9 at temperatures of 20°C and 30°C.

Solution

For T = 20°C: $T_1 = 25°C + 273 = 298\ K$

and $T_2 = 20°C + 273 = 293\ K$

from Eq. 21-1, $R_2 = \dfrac{R_1}{e^{\beta(1/T_1 - 1/T_2)}} = \dfrac{300\ \Omega}{e^{3118(1/298 - 1/293)}}$

$= 358\ \Omega$

For T = 30°C: $T_1 = 25°C + 273 = 298\ K$

and $T_2 = 30°C + 273 = 303\ K$

from Eq. 21-1, $R_2 = \dfrac{R_1}{e^{\beta(1/T_1 - 1/T_2)}} = \dfrac{300\ \Omega}{e^{3118(1/298 - 1/303)}}$

$= 252\ \Omega$

Applications

Figure 21-10 shows a thermistor connected as a feedback resistor in an inverting amplifier circuit. (Note the device circuit symbol.) In this case, the thermistor is supplied with a constant current determined by R_1 and V_i. The output voltage is directly proportional to the thermistor resistance, and so V_o varies with temperature change.

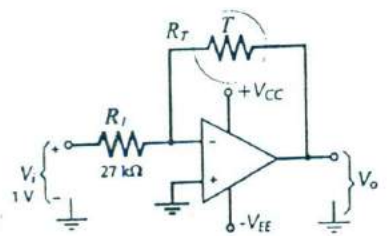


Figure 21-10
Use of an inverting amplifier to produce a constant current through a thermistor.

The circuit in Fig. 21-11 illustrates how a thermistor can be used for triggering a Schmitt circuit at a predetermined temperature. This could be air temperature, or the temperature of a liquid, or perhaps the temperature of some type of heating appliance. When the thermistor resistance (R_T) is increased to by the device temperature decrease, the Schmitt input voltage is raised to the upper trigger point, causing the output to switch negatively.

Example 21-3

Calculate V_i for the Schmitt circuit in Fig. 21-11 at 25°C and at 28°C if the thermistor is the 300 Ω device specified in Fig. 21-9.

Solution

at 25°C, $R_T = 300\ \Omega$,

$$V_i = \frac{V_{CC} \times R_T}{R_1 + R_T} = \frac{5\ \text{V} \times 300\ \Omega}{47\ \text{k}\Omega + 300\ \Omega}$$

$$= 31.7\ \text{mV}$$

For $T = 28$°C: $T_1 = 25°\text{C} + 273 = 298\ \text{K}$

and $T_2 = 28°\text{C} + 273 = 301\ \text{K}$

from Eq. 21-1, $R_2 = \frac{R_1}{\mathcal{E}^{\beta \cdot T_1 \cdot T_2}} = \frac{300\ \Omega}{\mathcal{E}^{3118 \cdot 1\,298 \cdot 1\,301}}$

$$= 270\ \Omega$$

$$V_i = \frac{V_{CC} \times R_T}{R_1 + R_T} = \frac{5\ \text{V} \times 270\ \Omega}{47\ \text{k}\Omega + 270\ \Omega}$$

$$= 28.6\ \text{mV}$$

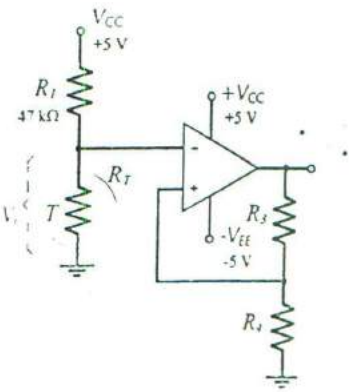


Figure 21-11
Schmitt trigger circuit using a thermistor input stage for temperature level detection.

Practise Problems

21-2.1 Calculate the output voltage from the circuit in Fig. 21-10 at 25°C and 28°C, if the 30 kΩ thermistor specified in Fig. 21-9 is used.

21-2.2 If the Schmitt circuit in Fig. 21-11 has $UTP = 1$ V, calculate a suitable resistance value for R_T for the circuit to trigger at 18°C. The thermistor used is the 300 Ω device specified in Fig. 21-9.

21-3 Tunnel Diodes

Tunnel Diode Operation

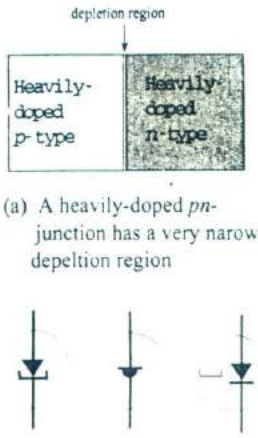
A *tunnel diode* (sometimes called an *Esaki diode* after its inventor, Leo Esaki) is a two-terminal *negative resistance* device that can be employed as an amplifier, an oscillator, or a switch. Recall from Ch. 1 that the width of the depletion region at a *pn*-junction

depends upon the doping density of the semi-conductor material. Lightly doped material has a wide depletion region, while heavily doped material has a narrow region. A tunnel diode uses very heavily doped semiconductor material, so the depletion region is extremely narrow. This is illustrated in Fig. 21-12 along with three frequently-used tunnel diode circuit symbols.

The depletion region is an insulator because it lacks charge carriers, and usually charge carriers can cross it only when the external bias is large enough to overcome the barrier potential. However, because the depletion region in a tunnel diode is so narrow, it does not constitute a large barrier to electron flow. Consequently, a small forward or reverse bias (not large enough to overcome the barrier potential) can give charge carriers sufficient energy to cross the depletion region. When this occurs, the charge carriers are said to be *tunnelling* through the barrier.

When a tunnel diode junction is reverse biased, (negative on the *p*-side, positive on the *n*-side), substantial current flow occurs due to the tunnelling effect, (electrons moving from the *p*-side to the *n*-side). Increasing levels of reverse bias voltage produce more tunnelling and a greater reverse current. So, as shown in Fig. 21-13, the reverse characteristic of a tunnel diode is linear, just like that of a resistor.

A forward biased tunnel diode initially behaves like a reverse biased device. Electron tunnelling occurs from the *n*-side to the *p*-side, and the forward current (I_F) continues to increase with increasing levels of forward voltage (E_F). Eventually, a peak level of tunnelling is reached, and then further increase in E_F actually causes I_F to decrease. (See the forward characteristic in Fig. 21-13.) The decrease in I_F with increasing E_F continues until the normal process of current flow across a forward biased junction begins to take over when the bias voltage becomes large enough to overcome the barrier potential. I_F now commences to increase with increasing levels of E_F, so that the final portion of the tunnel diode forward characteristics is similar to that for an ordinary *pn*-junction. The shape of the tunnel diode characteristics can be explained in terms of energy band diagrams for the semiconductor material.



(a) A heavily-doped *pn*-junction has a very narow depeltion region

(b) Tunnel diode circuit symbols

Figure 21-12
A tunnel diode has a heavily-doped pn-junction which results in a very narrow depletion region.

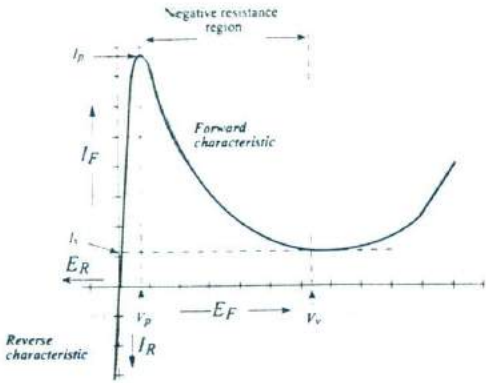


Figure 21-13
Tunnel diode characteristics. The current increases to a peak level (I_P) as the forward bias is increased, then falls off to a valley current (I_V) with increasing bias voltage.

Characteristics and Parameters

Consider the typical tunnel diode forward characteristics shown in Fig. 21-14. The *peak current* (I_p) and *valley current* (I_v) are easily identified on the forward characteristic as the maximum and minimum levels of I_F prior to the junction being completely forward biased. The peak voltage (V_p) is the level of forward bias voltage (E_F) corresponding to I_p, and the *valley voltage* (V_v) is the E_F level at I_v. V_F is the forward voltage drop when the device is completely forward biased. The dashed line at the bottom of the forward characteristic shows the characteristic for an ordinary forward biased diode. It is seen that this joins the tunnel diode characteristic as V_F is approached.

When a voltage is applied to a resistance, the current normally increases as the applied voltage is increased. Between I_p and I_v on the tunnel diode characteristic, I_F actually decreases as E_F is increased. So, this region of the characteristic is named the *negative resistance region*, and the *negative resistance* (R_D) of the tunnel diode is its most important property.

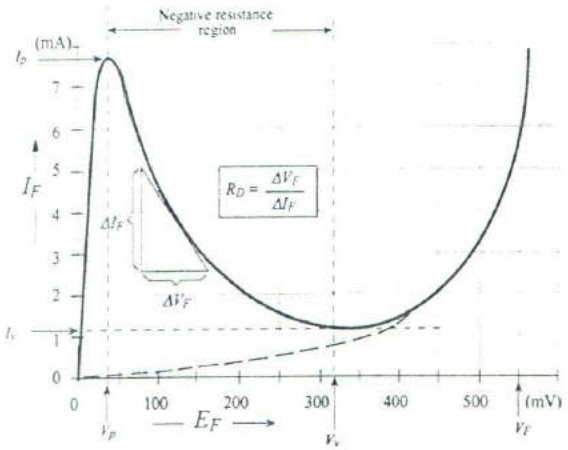


Figure 21-14
Typical forward characteristic for a tunnel diode. Note that the negative resistance region exists between forward bias voltages levels of approximately 50 mV and 325 mV.

The negative resistance value can be determined as the reciprocal of the slope of the characteristic in the negative resistance region. From Fig. 21-14, the negative resistance is $R_D = \Delta V_F/\Delta I_F$, and the *negative conductance* is $G_D = \Delta I_F/\Delta V_F$. If R_D is measured at different points on the negative resistance portion of the characteristic, slightly different values will be obtained at each point because the slope is not constant. Therefore, R_D is usually specified at the center of the negative resistance region. Figure 21-15 lists typical tunnel diode parameters.

Typical Tunnel Diode Parameters

I_p (mA)	V_p (mV)	I_v (mA)	V_v (mV)	V_F (V)	R_D (Ω)
1 to 100	50 to 200	0.1 to 5	350 to 500	0.5 to 1	-10 to -200

Figure 21-15
Tunnel diode specification data showing the range of parameters.

It is shown in Ch. 2 that a straight-line approximation of diode characteristics can sometimes be conveniently employed. For a tunnel diode, the *piecewise linear characteristics* can usually be constructed from data provided by the device manufacturer.

Example 21-4

Construct the piecewise linear characteristics and determine R_D for a *1N3712* tunnel diode from the following data: $I_p = 1$ mA, $I_v = 0.12$ mA, $V_p = 65$ mV, $V_v = 350$ mV, and $V_F = 500$ mV at $I_F = I_p$.

Solution

Refer to Fig. 21-16.

Plot *point 1* at, $I_p = 1$ mA and $V_p = 65$ mV

Plot *point 2* at, $I_v = 0.12$ mA and $V_v = 350$ mV

Draw the first portion of the characteristic from the zero point to *point 1*. Draw the negative resistance portion between *points 1* and *2*.

Plot *point 3* at, $I_F = I_p$ and $V_F = 500$ mV

Draw the final portion of the characteristics at the same slope as the line between *point 0* and *point 1*.

Draw the horizontal part of the characteristic from *point 2* to the final portion.

$$R_D = \frac{\Delta E_F}{\Delta I_F} = \frac{350 \text{ mV} - 65 \text{ mV}}{-(1 \text{ mA} - 0.12 \text{ mA})}$$

$$= -324\ \Omega$$

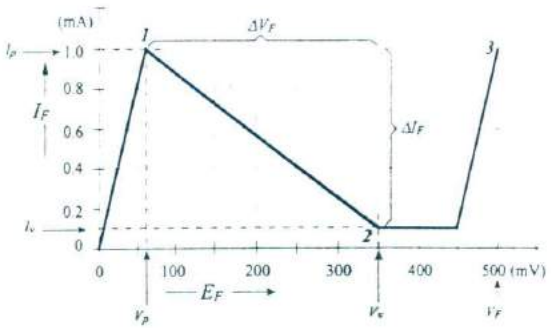


Figure 21-16
Piecewise linear characteristics for a tunnel diode drawn from information provided on the device specification.

Parallel Amplifier

For operation as an amplifier, a tunnel diode must be biased to the center of its negative resistance region. Figure 21-17(a) shows the basic circuit of a tunnel diode *parallel amplifier*. Load resistor R_L is connected in parallel with diode D_1 and supplied with current from voltage source E_B and signal source e_s. Figure 21-17(b) uses the

tunnel diode piecewise linear characteristics to show the *dc* conditions of the diode when the signal voltage is zero ($e_s = 0$), and when $e_s = \pm 100$ mV. Operation of the circuit is explained by the analysis in Ex. 21-5, which also demonstrates that a parallel amplifier has current gain but no voltage gain.

Example 21-5

Assuming that E_B and e_s have zero source resistance, calculate the current gain and voltage gain for the tunnel diode parallel amplifier in Fig. 21-17(a). The device piecewise linear characteristics are given in Fig. 21-17(b).

Solution

When $e_s = 0$;

$$E_{DQ} = E_B = 200 \text{ mV} \quad \text{[point } Q \text{ on Fig. 21-17(b)]}$$

at the Q point, $I_{DQ} = 2$ mA

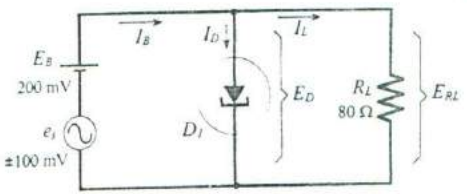
also, $E_{RLQ} = E_B = 200$ mV

$$I_{RLQ} = \frac{E_{RL}}{R_L} = \frac{200 \text{ mV}}{80\ \Omega}$$

$$= 2.5 \text{ mA}$$

$$I_{BQ} = I_{RL} + I_D = 2.5 \text{ mA} + 2 \text{ mA}$$

$$= 4.5 \text{ mA}$$



(a) Basic parallel amplifier circuit

When $e_s = +100$ mV;

$$E_B + e_s = 200 \text{ mV} + 100 \text{ mV} = 300 \text{ mV}$$

$$E_D = E_{RL(A)} = 300 \text{ mV} \quad \text{[point } A \text{ on Fig. 21-17(b)]}$$

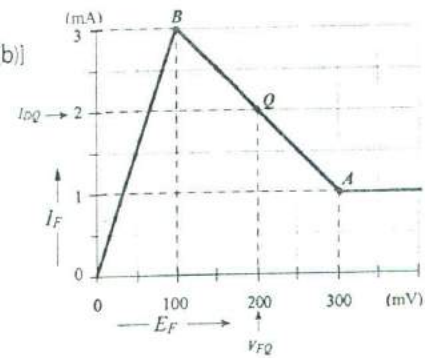
and, $I_{D(A)} = 1$ mA

also, $$I_{RL(A)} = \frac{E_{RL(A)}}{R_L} = \frac{300 \text{ mV}}{80\ \Omega}$$

$$= 3.75 \text{ mA}$$

$$I_{B(A)} = I_{RL(A)} + I_{D(A)} = 3.75 \text{ mA} + 1 \text{ mA}$$

$$= 4.75 \text{ mA}$$



(b) Circuit current and voltage levels

When $e_s = -100$ mV;

$$E_B + e_s = 200 \text{ mV} - 100 \text{ mV} = 100 \text{ mV}$$

$$E_D = E_{RL(B)} = 100 \text{ mV} \quad \text{[point } B \text{ on Fig. 21-17(b)]}$$

and, $I_{D(B)} = 3$ mA

also, $$I_{RL(B)} = \frac{E_{RL(B)}}{R_L} = \frac{100 \text{ mV}}{80\ \Omega}$$

$$= 1.25 \text{ mA}$$

Figure 21-17
A basic tunnel diode parallel amplifier has a load resistance in parallel with the diode, and the (series-connected) bias and signal sources applied directly to the diode and load.

$$I_{B(B)} = I_{RL(B)} + I_{D(B)} = 1.25 \text{ mA} + 3 \text{ mA}$$
$$= 4.25 \text{ mA}$$

total load current change,

$$\Delta I_{RL} = I_{RL(A)} - I_{RL(B)} = 3.75 \text{ mA} - 1.25 \text{ mA}$$
$$= 2.5 \text{ mA}$$

total signal current change,

$$\Delta I_B = I_{B(A)} - I_{B(B)} = 4.75 \text{ mA} - 4.25 \text{ mA}$$
$$= 0.5 \text{ mA}$$

current gain, $$A_i = \frac{\Delta I_{RL}}{\Delta I_B} = \frac{2.5 \text{ mA}}{0.5 \text{ mA}}$$
$$= 5$$

voltage gain, $$A_v = \frac{\Delta E_{RL}}{e_s} = \frac{\pm 100 \text{ mV}}{\pm 100 \text{ mV}}$$
$$= 1$$

The current gain equation for a tunnel diode parallel amplifier can be shown to be,

$$A_i = \frac{R_D}{R_D - R_L} \qquad (21\text{-}2)$$

Note that R_D is already taken as negative in Eq. 21-2, so that only the absolute value should be used in calculating A_i. For R_D = 100 Ω and R_L = 80 Ω, as in Ex. 21-5,

$$A_i = \frac{100}{100 \Omega - 80 \Omega} = 5$$

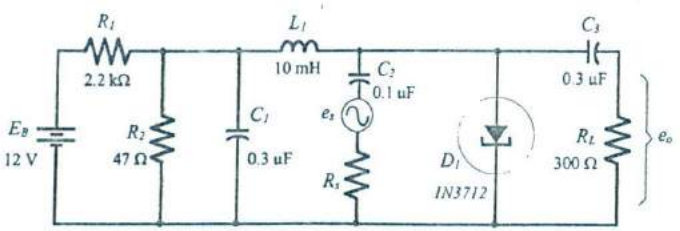


Figure 21-18
In a practical parallel amplifier circuit the load and signal source are capacitor-coupled to the tunnel diode.

From Eq. 21-2, it is seen that (when $R_L << R_D$, $A_i \approx 1$), (when $R_L >> R_D$, $A_i < 1$), and (when $R_L = R_D$, $A_i = \infty$). A current gain of infinity means that the circuit is likely to oscillate. For maximum stable current gain, R_L should be selected just slightly less than R_D.

Figure 21-18 shows the circuit of a practical tunnel diode parallel amplifier. The signal voltage e_s and load resistor R_L are capacitor-

coupled to the diode, while *dc* bias is provided by source voltage E_B and voltage divider R_1 and R_2. Inductor L_1 and capacitor C_1 isolate the bias supply from *ac* signals.

A tunnel diode *series amplifier* can be constructed. In this case the device is connected in series with the load, and voltage amplification is obtained instead of current amplification. Oscillators and switching circuits can also be constructed using tunnel diodes.

Practise Problems

21-3.1 Draw the *dc* and ac equivalent circuits for the tunnel diode parallel amplifier in Fig. 21-18. Also, draw the *dc* load line on the device piecewise linear characteristics in Fig. 21-16. Determine the bias conditions and calculate the current gain. The inductor has a 35 Ω winding resistance.

Chapter-21 Review Questions

Section 21-1

21-1 Using illustrations, explain the operation of a *VVC* diode. Sketch the doping profile at abrupt and hyperabrupt junctions, and explain the difference between the two.

21-2 Sketch the equivalent circuit for a *VVC*. Explain the origin of each component and show how the circuit may be simplified.

21-3 List the most important *VVC* parameters and state typical parameter values.

21-4 Sketch a circuit to show a typical *VVC* application. Briefly explain.

Section 21-2

21-5 Sketch typical resistance/temperature characteristics for a thermistor, and discuss the thermistor operation.

21-6 List the most important parameters for a thermistor, and state typical parameter values.

21-7 Sketch a circuit diagram to show how a thermistor can be used to control a Schmitt trigger circuit. Explain the circuit operation.

21-8 Draw a diagram to show how a thermistor might be used to compensate for V_{BE} variations (due to temperature change) in an emitter current biased *BJT* circuit.

Section 21-3

21-9 Discuss the difference between a tunnel diode and an ordinary *pn*-junction diode. Explain what is meant by *tunnelling*.

21-10 Sketch typical forward and reverse characteristics for a tunnel diode. Discuss the shape of the characteristics, and identify the regions and important points on the characteristics.

21-11 List the most important parameters for a tunnel diode, and state typical parameter values.

21-12 Sketch the basic circuit of a tunnel diode parallel amplifier, explain its operation, and write the equation for amplifier current gain.

21-13 Sketch a practical tunnel diode parallel amplifier circuit, and discuss the function of each component.

Chapter-21 Problems

Section 21-1

21-1 A tuner amplifier circuit similar to Fig. 21-6 has V_{CC} = 15 V and the following component values: L_1 = 80 μH, R_3 = 1 kΩ, R_4 = 10 kΩ, and R_5 = 4.7 kΩ. Assuming that D_1 has the C_T/V_R characteristic in Fig. 21-5, determine the maximum and minimum resonance frequency for the circuit.

21-2 If the *VVC* in the circuit in Problem 21-1 is replaced with the *VVC* specified in Fig. 21-4. Calculate the highest and lowest possible resonance frequency for the circuit.

21-3 A tuned amplifier circuit as in Fig. 21-6 is to have its resonance frequency adjustable from 0.8 MHz to 1.2 MHz. Determine suitable resistance values for R_3, R_4, and R_5 if V_{CC} = 18 V, L_1 = 100 μH, and the *VVC* characteristics are those in Fig. 21-5.

21-4 Determine the bias voltage for the *VVC* in Problem 21-3 to give a 1 MHz resonance frequency.

21-5 The *VVC* in the circuit in Problem 21-1 is replaced with another one that gives a resonance frequency ranging from 900 kHz to 3.5 MHz. Specify the new *VVC* in terms of its capacitance and tuning ratio from 1 V to 10 V.

Section 21-2

21-6 A thermistor with a 1 kΩ resistance at 25°C has β specified as 3395. Calculate the thermistor resistance at 5°C and at 35°C temperatures.

21-7 Calculate the temperature of the 30 kΩ thermistor specified in Fig. 21-9 when its resistance is measured as 24.5 kΩ.

21-8 A thermistor circuit as in Fig. 21-10 has V_i = -1 V and R_1 = 22 kΩ. Calculate the output voltage at 25°C and 35°C if the thermistor is the 30 kΩ device specified in Fig. 21-9.

21-9 The 300 Ω thermistor specified in Fig. 21-9 is connected in series with a 1.5 kΩ resistor (R_1) and a 12 V supply.

Determine the voltage drop across R_1 at temperatures of 22°C, 28°C, and 31°C.

Section 21-3

21-10 A tunnel diode is specified as having $I_p = 6$ mA, $V_p = 50$ mV, $I_v = 0.5$ mA, $V_v = 400$ mV, and $V_F = 550$ mV at $I_F = I_p$. Construct the piecewise linear characteristics for the device, and determine its negative resistance value.

21-11 Construct the piecewise linear characteristics for a *1N3715* from the following data: $I_p = 2.2$ mA, $I_v = 0.21$ mA, $V_p = 65$ mV, $V_v = 355$ mV, and $V_F = 510$ mV at $I_F = I_p$. Also, determine R_D for the device.

21-12 A parallel amplifier uses the tunnel diode specified in Problem 21-10 and a load resistance of 47 Ω. Calculate the circuit current gain.

21-13 A *1N3715* is to be connected as a parallel amplifier. Using the piecewise linear characteristics drawn for Problem 21-11, draw an appropriate *dc* load line and determine suitable values for R_L, E_B, and e_s. Also, calculate the current gain.

21-14 A practical tunnel diode parallel amplifier circuit as in Fig. 21-18 has the following components: $E_B = 5$ V, $R_1 = 220$ Ω, $R_2 = 12$ Ω, $C_1 = 0.5$ μF, $R_w = 0.5$ Ω, $L_1 = 20$ mH, $C_2 = 0.2$ μF, $C_3 = 0.5$ μF and $R_L = 75$ Ω. The tunnel diode used has $I_p = 5$ mA, $V_p = 50$ mV, $I_v = 1$ mA, and $V_v = 400$ mV. Construct the piecewise linear characteristics, draw the *dc* load line, and calculate the circuit current gain.

Practise Problem Answers

21-1.1 39 kΩ, 35 kΩ, 47 kΩ

21-2.1 -1.1 V, -0.98 V

21-2.2 1.5 kΩ

21-3.1 0.57 mA, 204 mV, 13.5