Index

active areas 47, 51
AND plane 72–3, 89, 113, 137
and-or-not function 68
architecture 4, 104, 129–32
arithmetic and logic unit 104, 111, 114
aspect ratio 21, 30, 32, 41, 65, 67
asynchronous control 109
asynchronous timing 80, 114
automatic routing 107

beat time 109, 113, 114
bipolar technology 2–3
body effect 13, 22, 29, 37, 38
bonding pads 147
buffer circuits 40–4
buffer gate chain 41–2, 116, 117–18, 135
buffering 41, 73, 116, 117, 139
built-in self-test 119, 121–4
buried contact 47, 50, 60, 62, 131
butting contact 51, 59–60, 61

capacitance estimation 54–5, 139
capacitance parameters 54
cascadable binary counter 129
cell approach to design 107–8, 138
cell boundary 141
cell conventions 141
channel 10–13
characteristic approximation 27–8
charge sharing 92, 96–8, 99–102
circuit design 5–6, 64, 136–9
circuit load 18, 23
clock generation 115–18, 135
clock skew 118, 133
clocked load 91, 96
CMOS
  cell 107
  design rules 58, 60–2
  fabrication 50–1
  inverter 30–5
  logic family 2, 3
  pass gate 39–40
  pass transistor array 70
  pull-up circuit 39, 67, 77–8
  programmable logic array 77–8
combinational logic 64, 88
complex logic function 68, 108, 145
computer aided computer design 64, 77
contact cuts 47, 50, 51, 60–2, 141, 145
control logic 5, 104, 108–14, 134, 137, 143
controllability 127–8
current capability 25, 31, 41, 43, 65

data architecture 104, 111, 127
data pipeline 88–9, 124
data-selection circuit *see* multiplexor
decoding 94
depletion implant 47, 58, 61
depletion region 11–13
depletion transistor 12, 23–4, 47, 58
design approaches 3–4, 105–8
design area 132, 143
design hierarchy 4, 127
design process 4–6, 127–50
design rules 58–62
digital switch 18, 30
drain region 9, 47, 50, 51, 58
driver switch 30, 38
driver transistor 21, 32
drop-ins 53
D-type flip flop 81–2, 86–7, 132–3
dynamic circuit 2, 37, 65, 78
dynamic flip flop 86–92, 132–3
dynamic logic *see* dynamic circuit
dynamic memory cell 94, 96–103

edge times 25–9, 30, 32, 41
electrical checks 147
electrical parameters 53–5
electron mobility 15, 18, 32, 67
enhancement transistor 12, 13, 18, 23, 24, 47, 59
etch 46
exclusive-or gate 119, 134
exhaustive testing 119

fabrication process 47–51
falling edge time 25–6, 29, 31–2, 37, 67
fan-in 66
fan-out 139
fault diagnosis 121, 124, 128
fixed control logic 109–11
flip flop
  clocked 80, 81
  cross-coupled inverters 78, 98, 100
  D-type 81–2, 86–7, 132–3
  dynamic 86–92, 132–3
  edge triggered 80, 83
  hold time 80
  J-K 83–5, 91, 133, 138
  level triggered 80, 81, 86
  master 83
  master-slave 84–5, 109, 115, 119, 121, 130
  partial switching 80
  Set–Reset 79–80, 117
  set-up time 80
  slave 83
  toggle 83
floor plan 131, 141, 144
formal control 108
full custom design 3, 106–7, 127
functional testing 5, 53, 139, 150

gate capacitance 12, 25, 54, 86
gate delay 2, 42, 64
gated clocks 109, 113, 115, 133
geometric layout 6, 45, 47, 50, 141
geometric patterns 45, 147
ground line 47, 50, 141, 145
ground pad 44, 147, 148

'hand-crafted' design 106, 127
hole mobility 18, 32, 67

input capacitance 29, 41, 54, 65, 67, 74
input pads 44, 147
input register 89, 95
integrated circuits 1
interconnection delay 55, 57
interconnections 6, 107, 143–7
interfacing 106, 107
inversion 10–13
inverter
  CMOS 30–5
  edge times 25–9, 32
  NMOS depletion load 23–4
  NMOS enhancement load 21–3
  principle of 18
  ratioless 30, 38–9, 91
  resistor load 20–1
  restoring 37, 86
inverter ratio 23, 24, 141

J-K flip flop 83–5, 91, 133, 138

large scale integration 1
layer patterning 46
layout checking 6, 58, 147
leakage current 22, 31, 36, 87
load capacitance *see* output capacitance
load switch 30, 38
logic cells 3, 107, 138
logic conventions 7
logic design 5, 64, 132–6
logic family 2, 3, 65, 107

mask 6, 45
material growth 45–6
medium scale integration 1
memory element 64–5, 78
microprogrammed control 111–13, 119
minimum frequency of operation 37, 65, 87
minimum geometry transistor 32, 36, 38, 67, 70, 78, 91
MOS
  logic family 2, 3
  process 45–7
  technology 2–3
multiplexor 70, 113, 121, 128, 133–4, 137, 141

nand gate 65–6
n-channel transistor 8
NMOS design rules 58–62
NMOS logic
  inverters 20–4, 38–9, 91–2
  pass transistor 36–8, 86, 89, 91, 98, 99, 132–3
  pass transistor array 70–2, 136

NMOS logic (cont'd)
pass transistor chain 37, 39, 72
programmable logic array 73–4, 91
random logic 65–9, 136–8
NMOS processing 47–50
NMOS transistor
characteristic 13–17
characteristic approximation 27–8
conduction 10–11
depletion 12, 24
enhancement 12, 18, 24
structure 8–10
noise margin 21, 24
non-overlapping timing pulses 38, 83, 87, 114–16, 130
nor array 73
nor gate 67
not gate *see* inverter
n-type semiconductor 9
n-well CMOS 50, 62

observability 121, 127
OR plane 72–3, 113–14
output capacitance 23, 25, 36, 37, 38, 41, 54–5, 65, 67, 74, 92
output pads 44, 147
output register 89, 95

packaging 53, 148
parallel-to-serial data conversion 87, 128
parametric testing 53, 147
parasitic transistors 45, 50
partitioning 4, 74, 106, 119, 127
pass transistor
CMOS 39–40, 70
NMOS 36–8, 70, 86, 89, 91, 98, 99, 132–3
pass transistor array 70–2, 136
pass transistor chain 37, 39, 72
patterning levels 45
p-channel transistor 12–13
peripheral cells 107
phased clocks *see* non-overlapping timing pulses
pinch-off point 16–17
placement 6, 141–3
PMOS transistor
characteristic 17–18
conduction 12–13
enhancement 13, 30
structure 12
polysilicon gate 8, 12, 47, 50, 51, 58
portability of layouts 62
positive logic 7
power dissipation 2, 30, 33, 70, 74
power line 47, 50, 141, 145
power pad 44, 147, 148
pre-charging 39, 77–8, 96, 100
primitive logic functions 1, 67, 107, 134, 138
priority encoder 73–4, 112
process design rules 58–62
process tolerances 53, 55, 58, 147
processing faults 52–3
programmable logic array 72–8, 89–91, 113–14, 136–8
propagation delay *see* gate delay
pseudo random number generator 119, 121, 124
p-type semiconductor 9
p-type silicon substrate 9, 47, 51
pull-down branch 68, 81, 84, 137
pull-down circuit 65, 67, 77, 79
pull-up circuit 39, 65, 67, 77, 86
p-well CMOS 50, 62

race hazards 114
random access memory 94–103, 105, 113
random logic 64, 65–9, 72, 74, 136–8
ratioed design 29, 96
ratioless design 30, 96
ratioless inverters 30–5, 38–9, 91–2
read only memory 113–14
refreshing 65, 94, 96
resistance parameters 54
resistive mode *see* resistive region
resistive region 14–15, 17, 21, 22, 23, 27, 31, 32
restoring invertor 37, 86
ring counter 115
rising edge time 23, 25–9, 31–2, 36, 43, 67

saturated mode *see* saturated region
saturated region 16–18, 22, 24, 25, 27, 31, 33
saturation current 17, 18
scaling 56–7
scan path 121, 122
self-aligned process 50, 51
self-test 119, 121–4
semi-custom design 3–4, 107–8

sense amplifier 100–3
sequential logic 64–5
serial-to-parallel data conversion 87, 128
shift register 87, 92, 109, 115, 119, 121, 122, 127–9, 132
signature analysis 119–21
silicon technology 1–2
silicon wafer 45
simulation 5, 6, 139
small scale integration 1
source region 9, 47, 50, 51, 58
speed 2, 18, 29
speed–power product 2, 72, 74
standard cells 108
static circuit 65
static flip flops 78–86
static memory cell 98–9
stick diagrams 6, 62–3, 70, 141
storage element *see* memory element
substrate connection 10, 13, 22, 30–1, 50, 148
superbuffer 42–3, 135, 139
synchronous control 108
synchronous timing 80, 114, 129
system beat time 109, 113, 114
system specification 4, 104, 127–9

test area 53, 131
testability 4, 105, 118–24, 128
threshold voltage 11–13, 17, 18, 22
timing
  circuitry 5, 104, 115–18, 130, 135
  conflicts 80, 114
  logic *see* circuitry *under* timing
  phases 114
  skew 55, 118, 133
transient switching current 30, 33
transistor array 64
transistor isolation 11
transistor parameters 54
transistor symbols 13
transmission gate *see* pass transistor
two-phase non-overlapping clocks *see* non-overlapping timing pulses

uncommitted logic array 3–4, 107–8

very large scale integration 1
voltage controlled switch 36, 65, 70

yield 2, 53, 147