19

Regulated D.C. Power Supply

Introduction

In general, electronic circuits using tubes or transistors require a source of d.c. power. For example, in tube amplifiers, d.c. voltage is needed for plate, screen grid and control grid. Similarly, the emitter and collector bias in a transistor must also be direct current. Batteries are rarely used for the purpose as they are costly and require frequent replacement. In practice, d.c. power for electronic circuits is most conveniently obtained from commercial a.c. lines by using rectifier-filter system, called a *d.c. power supply*.

The rectifier-filter combination constitutes an ordinary d.c. power supply. The d.c. voltage from an ordinary power supply remains constant so long as a.c. mains voltage or load is unaltered. However, in many electronic applications, it is desired that d.c. voltage should remain constant irrespective of changes in a.c. mains or load. Under such situations, *voltage regulating devices* are used with ordinary power supply. This constitutes *regulated d.c. power supply* and keeps the d.c. voltage at fairly constant value. In this chapter, we shall focus our attention on the various voltage regulating circuits used to obtain regulated power supply.

19.1 Ordinary D.C. Power Supply

An ordinary or unregulated d.c. power supply contains a rectifier and a filter circuit as shown in Fig. 19.1. The output from the rectifier is pulsating d.c. These pulsations are due to the presence of a.c. component in the rectifier output. The filter circuit removes the a.c. component so that steady d.c. voltage is obtained across the load.

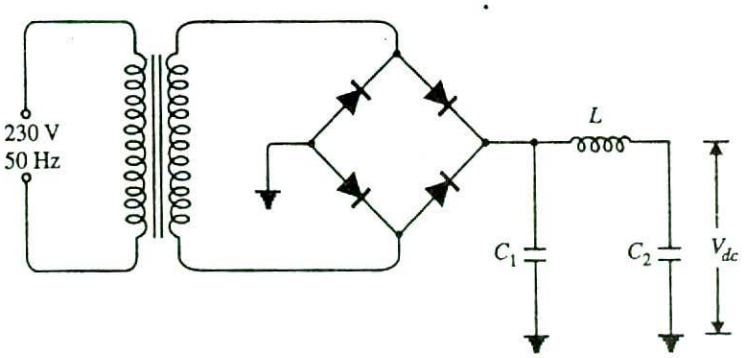


Fig. 19.1

Limitations. An ordinary d.c. power supply has the following drawbacks :

(*i*) The d.c. output voltage changes directly with input a.c. voltage. For instance, a 5% increase in input a.c. voltage results in approximately 5% increase in d.c. output voltage.

(*ii*) The d.c. output voltage decreases as the load current increases. This is due to voltage drop in (*a*) transformer windings (*b*) rectifier and (*c*) filter circuit.

These variations in d.c. output voltage may cause inaccurate or erratic operation or even malfunctioning of many electronic circuits. For example, in an oscillator, the frequency will shift and in transmitters, distorted output will result. Therefore, ordinary power supply is unsuited for many electronic applications and is being replaced by regulated power supply.

19.2 Important Terms

For comparison of different types of power supplies, the following terms are commonly used :

(*i*) **Voltage regulation.** The d.c.voltage available across the output terminals of a given power supply depends upon load current. If the load current I_{dc} is increased by decreasing R_L (See Fig. 19.2), there is greater voltage drop in the power supply and hence smaller d.c. output voltage will be available. Reverse will happen if the load current decreases. The variation of output voltage w.r.t. the amount of load current drawn from the power supply is known as *voltage regulation* and is expressed by the following relation :

$$\% \text{ Voltage regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$$

where V_{NL} = d.c. output voltage at no-load

V_{FL} = d.c. output voltage at full-load

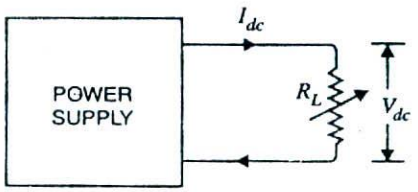


Fig. 19.2

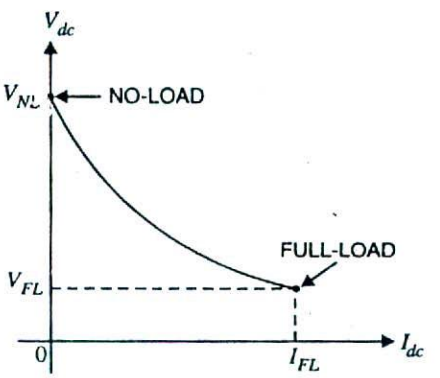


Fig. 19.3

In a well designed power supply, the full-load voltage is only slightly less than no-load voltage *i.e.* voltage regulation approaches zero. Therefore, lower the voltage regulation, the lesser the difference between full-load and no-load voltages and better is the power supply. Power supplies used in practice have a voltage regulation of 1% *i.e.* full-load voltage is within 1% of the no-load voltage. Fig. 19.3 shows the change of d.c. output voltage with load current. This is known as *voltage regulation curve*.

(*ii*) **Minimum load resistance.** The change of load connected to a power supply varies the load current and hence the d.c. output voltage. In order that a power supply gives the rated output voltage and current, there is minimum load resistance allowed. For instance, if a power supply is required to deliver a full-load current I_{FL} at full-load voltage V_{FL}, then,

$$R_{L(min)} = \frac{V_{FL}}{I_{FL}}$$

Thus, if a data sheet specifies that a power supply will give an output voltage of 100V at a maximum rated current of 0.4A, then minimum load resistance you can connect across supply is $R_{min} = 100/0.4 = 250\ \Omega$. If any attempt is made to decrease the value of R_L below this value, the rated d.c. output voltage will not be available.

Example 19.1. *If the d.c. output voltage is 400V with no-load attached to power supply but decreases to 300V at full-load, find the percentage voltage regulation.*

Solution.

$$V_{NL} = 400\ \text{V}; \quad V_{FL} = 300\ \text{V}$$

$$\therefore \quad \%\ \text{Voltage regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100 = \frac{400 - 300}{300} \times 100 = \mathbf{33.33\ \%}$$

Example 19.2. *A power supply has a voltage regulation of 1%. If the no-load voltage is 30V, what is the full-load voltage ?*

Solution. Let V_{FL} be the full-load voltage.

$$\%\ \text{Voltage regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$$

or $$1 = \frac{30 - V_{FL}}{V_{FL}} \times 100$$

$$\therefore \quad V_{FL} = \mathbf{29.7\ V}$$

Example 19.3. *Two power supplies A and B are available in the market. Power supply A has no-load and full-load voltages of 30V and 25V respectively whereas these values are 30V and 29V for power supply B. Which is better power supply ?*

Solution. That power supply is better which has lower voltage regulation.

Power supply A

$$V_{NL} = 30\ \text{V}, \quad V_{FL} = 25\ \text{V}$$

$$\therefore \quad \%\ \text{Voltage regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100 = \frac{30 - 25}{25} \times 100 = 20\%$$

Power supply B

$$V_{NL} = 30\ \text{V}, \quad V_{FL} = 29\ \text{V}$$

$$\therefore \quad \%\ \text{Voltage regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100 = \frac{30 - 29}{29} \times 100 = 3.45\ \%$$

Therefore, power supply B is better than power supply A.

Example 19.4. *Fig. 19.4 shows the regulation curve of a power supply. Find (i) voltage regulation and (ii) minimum load resistance.*

Solution. Referring to the regulation curve shown in Fig. 19.4, it is clear that :

$$V_{NL} = 500\ \text{V}; \quad V_{FL} = 300\ \text{V}$$

$$I_{FL} = 120\ \text{mA}; \quad R_{L\ (min)} = ?$$

(*i*) $$\text{Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$$

$$= \frac{500 - 300}{300} \times 100$$

$$= \mathbf{66.7\ \%}$$

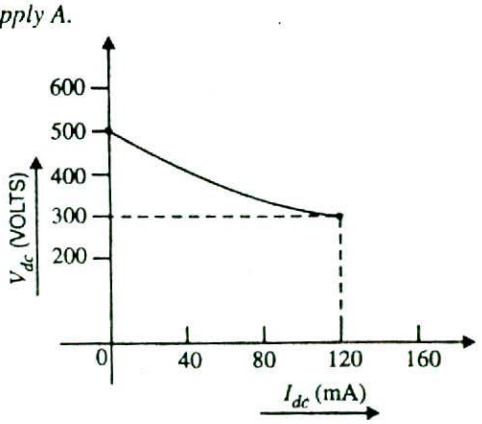


Fig. 19.4

(*ii*) $$R_{L\,(min)} = \frac{V_{FL}}{I_{FL}} = \frac{300\text{ V}}{120\text{ mA}} = 2.5\text{ k}\Omega$$

19.3 Regulated Power Supply

A d.c. power supply which maintains the output voltage constant irrespective of a.c. mains fluctuations or load variations is known as **regulated d.c. power supply.**

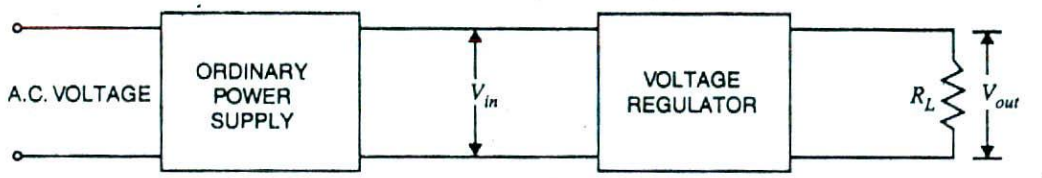


Fig. 19.5

A regulated power supply consists of an ordinary power supply and voltage regulating device. Fig. 19.5 shows the block diagram of a regulated power supply. The output of ordinary power supply is fed to the voltage regulator which produces the final output. The output voltage remains constant whether the load current changes or there are fluctuations in the input a.c. voltage.

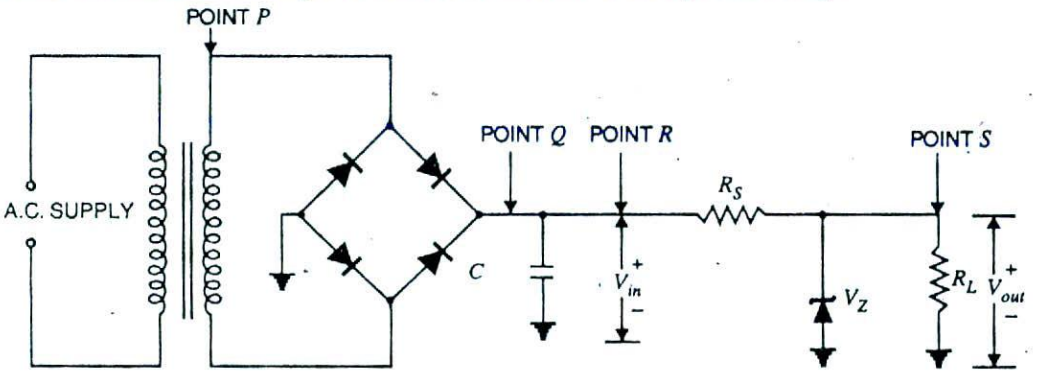


Fig. 19.6

Fig. 19.6 shows the complete circuit of a regulated power supply using zener diode as a voltage regulating device. As you can see, the regulated power supply is a combination of three circuits *viz.*, (*i*) bridge rectifier (*ii*) a capacitor filter C and (*iii*) zener voltage regulator. The bridge rectifier converts the transformer secondary a.c. voltage (point P) into pulsating voltage (point Q). The pulsating d.c. voltage is applied to the capacitor filter. This filter reduces the pulsations in the rectifier d.c. output voltage (point R). Finally, the zener voltage regulator performs two functions. Firstly, it reduces the variations in the filtered output voltage. Secondly, it keeps the output (V_{out}) nearly constant whether the load current changes or there is change in input a.c. voltage. Fig. 19.7 shows the waveforms at various stages of regulated power supply. Note that bridge rectifier and capacitor filter constitute an ordinary power supply. However, when voltage regulating device is added to this ordinary power supply, it turns into a regulated power supply.

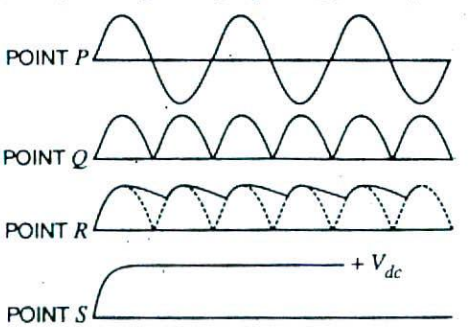


Fig. 19.7

Note. In practice, this type of regulator is rarely used. The primary problem with the simple zener regulator is the fact that the zener wastes a tremendous amount of power. Practical voltage regulators contain a number of discrete and/or integrated active devices. Nevertheless, this circuit gives an idea about the regulated power supply.

Need of Regulated Power Supply

In an ordinary power supply, the voltage regulation is poor *i.e.* d.c. output voltage changes appreciably with load current. Moreover, output voltage also changes due to variations in the input a.c. voltage. This is due to the following reasons :

(*i*) In practice, there are considerable variations in a.c. line voltage caused by outside factors beyond our control. This changes the d.c. output voltage. Most of the electronic circuits will refuse to work satisfactorily on such output voltage fluctuations. This necessitates to use regulated d.c. power supply.

(*ii*) The internal resistance of ordinary power supply is relatively large (> 30 Ω). Therefore, output voltage is markedly affected by the amount of load current drawn from the supply. These variations in d.c. voltage may cause erratic operation of electronic circuits. Therefore, regulated d.c. power supply is the only solution in such situations.

19.4 Types of Voltage Regulators

A device which maintains the output voltage of an ordinary power supply constant irrespective of load variations or changes in input a.c. voltage is known as a *voltage regulator*. A voltage regulator generally employs electronic devices to achieve this objective. There are basic two types of voltage regulators *viz.*, (*i*) series voltage regulator (*ii*) shunt voltage regulator.

The series regulator is placed in series with the load as shown in Fig. 19.8 (*i*). On the other hand, the shunt regulator is placed in parallel with the load as shown in Fig. 19.8 (*ii*). Each type of regulator provides an output voltage that remains constant even if the input voltage varies or the load current changes.

1. For low voltages. For low d.c. output voltages (upto 50V), either zener diode alone or zener in conjunction with transistor is used. Such supplies are called transistorised power supplies. A transistor power supply can give only low stabilised voltages because the safe value of V_{CE} is about 50 V and if it is increased above this value, the breakdown of the junction may occur.

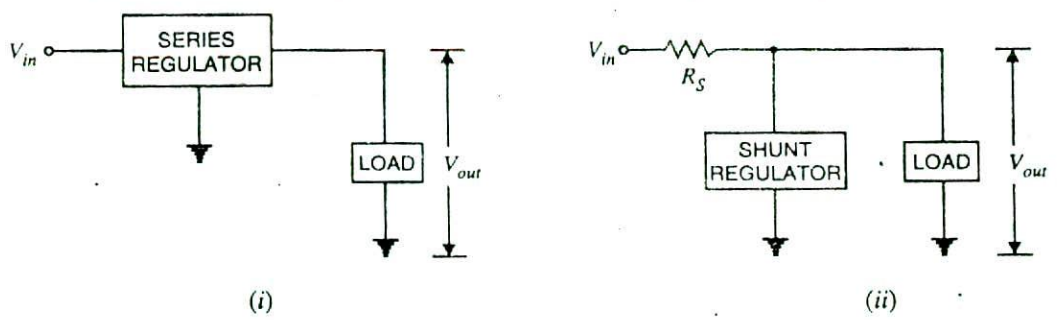


Fig. 19.8

2. For high voltages. For voltages greater than 50 V, glow tubes are used in conjunction with vacuum tube amplifiers. Such supplies are generally called tube power supplies and are extensively used for the proper operation of vacuum valves.

19.5 Zener Diode Voltage Regulator

As discussed in chapter 9, when the zener diode is operated in the breakdown or zener region, the voltage across it is substantially constant for a large change of current through it. This characteristic permits it to be used as a voltage regulator. Fig. 19.9 shows the circuit of a zener diode regulator. As long as input voltage V_{in} is greater than zener voltage V_Z, the zener operates in the breakdown region and maintains constant voltage across the load. The series limiting resistance R_S limits the input current.

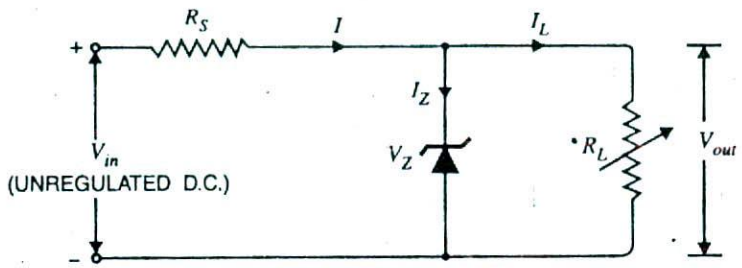


Fig. 19.9

Operation. The zener will maintain constant voltage across the load inspite of changes in load current or input voltage. As the load current increases, the zener current decreases so that current through resistance R_S is constant. As output voltage = $V_{in} - IR_S$, and I is constant, therefore, output voltage remains unchanged. The reverse would be true should the load current decrease. The circuit will also correct for the changes in input voltages. Should the input voltage V_{in} increase, more current will flow through the zener, the voltage drop across R_s will increase but load voltage would remain constant. The reverse would be true should the input voltage decrease.

Limitations. A zener diode regulator has the following drawbacks :

(*i*) It has low efficiency for heavy load currents. It is because if the load current is large, there will be considerable power loss in the series limiting resistance.

(*ii*) The output voltage slightly changes due to zener impedance as $V_{out} = V_Z + I_Z Z_Z$. Changes in load current produce changes in zener current. Consequently, the output voltage also changes. Therefore, the use of this circuit is limited to only such applications where variations in load current and input voltage are small.

Example 19.5. *Fig. 19.10 shows the zener regulator. Calculate (i) current through the series resistance (ii) minimum and maximum load current and (iii) minimum and maximum zener current. Comment on the results.*

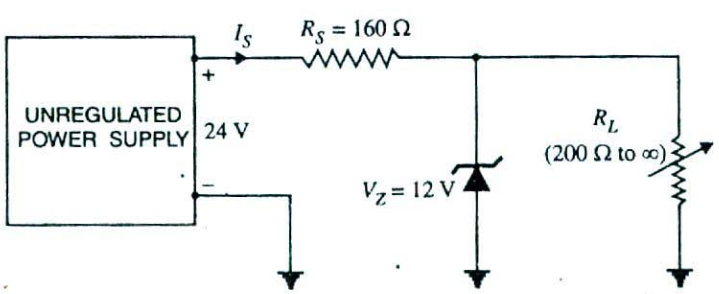


Fig. 19.10

Solution.

(*i*) $$I_S = \frac{V_{in} - V_{out}}{R_S} = \frac{24 - 12}{160} = \frac{12\text{ V}}{160\,\Omega} = \mathbf{75\text{ mA}}$$

(*ii*) The minimum load current occurs when $R_L \to \infty$.

$$\therefore \quad I_{L\,(min)} = \mathbf{0}$$

The maximum load current occurs when $R_L = 200\,\Omega$.

$$\therefore \quad I_{L\,(max)} = \frac{V_{out}}{R_{L(min)}} = \frac{12\text{ V}}{200\,\Omega} = \mathbf{60\text{ mA}}$$

(*iii*) $$I_{Z\,(min)} = I_S - I_{L\,(max)} = 75 - 60 = \mathbf{15\text{ mA}}$$

$$I_{Z\,(max)} = I_S - I_{L\,(min)} = 75 - 0 = \mathbf{75\text{ mA}}$$

Comments. The current I_S through the series resistance R_S is constant. When load current increases from 0 to 60 mA, the zener current decreases from 75 mA to 15 mA, maintaining I_S constant in value. This is the normal operation of zener regulator *i.e.* I_S and V_{out} remain constant inspite of changes in load current or source voltage.

Example 19.6. *A zener regulator has $V_Z = 15$V. The input voltage may vary from 22 V to 40 V and load current from 20 mA to 100 mA. To hold load voltage constant under all conditions, what should be the value of series resistance ?*

Solution. In order that zener regulator may hold output voltage constant under all operating conditions, it must operate in the breakdown region. In other words, there must be zener current for all input voltages and load currents. The worst case occurs when the input voltage is minin um and load current is maximum because then zener current drops to a minimum.

$$\therefore \quad R_{S(max)} = \frac{V_{in(min)} - V_{out}}{I_{L(max)}}$$

$$= \frac{22 - 15}{0.1} = \frac{7\text{ V}}{0.1\text{ A}} = \mathbf{70\,\Omega}$$

19.6. Transistor Series Voltage Regulator

Figure 19.11 shows a simple series voltage regulator using a transistor and zener diode. The circuit is called a series voltage regulator because the load current passes through the series transistor Q_1 as shown in Fig. 19.11. The unregulated d.c. supply is fed to the input terminals and the regulated output is obtained across the load. The zener diode provides the reference voltage.

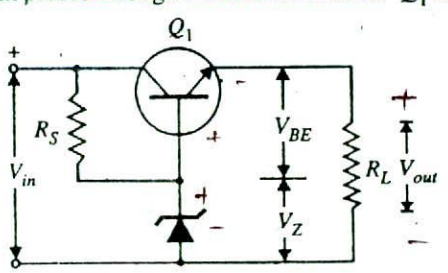


Fig. 19.11

Operation. The base voltage of transistor Q_1 is held to a relatively constant voltage across the zener diode. For example, if 8V zener (*i.e.*, $V_Z = 8$V) is used, the base voltage of Q_1 will remain approximately 8V. Referring to Fig. 19.11,

$$V_{out} = V_Z - V_{BE}$$

(*i*) If the output voltage decreases, the increased base-emitter voltage causes transistor Q_1 to conduct more, thereby raising the output voltage. As a result, the output voltage is maintained at a constant level.

(*ii*) If the output voltage increases, the decreased base-emitter voltage causes transistor Q_1 to conduct less, thereby reducing the output voltage. Consequently, the output voltage is maintained at a constant level.

The advantage of this circuit is that the changes in zener current are reduced by a factor β. Therefore, the effect of zener impedance is greatly reduced and much more stabilised output is obtained

Limitations

(*i*) Although the changes in zener current are much reduced, yet the output is not absolutely constant. It is because both V_{BE} and V_Z decrease with the increase in room temperature.

(*ii*) The output voltage cannot be changed easily as no such means is provided.

Example 19.7. *For the circuit shown in Fig. 19.11, if $V_Z = 10V$, $\beta = 100$ and $R_L = 1000\,\Omega$, find the load voltage and load current. Assume $V_{BE} = 0.5V$ and the zener operates in the breakdown region.*

Solution.

$$\text{Output voltage, } V_{out} = V_Z - V_{BE}$$
$$= 10 - 0.5 = \mathbf{9.5\ V}$$
$$\text{Load current, } I_L = \frac{V_{out}}{R_L} = \frac{9.5\ \text{V}}{1000\,\Omega} = \mathbf{9.5\ mA}$$

Example 19.8. *A series voltage regulator is required to supply a current of 1A at a constant voltage of 6V. If the supply voltage is 10 V and the zener operates in the breakdown region, design the circuit. Assume $\beta = 50$, $V_{BE} = 0.5V$ and minimum zener current = 10 mA.*

Solution. The design steps require the determination of zener breakdown voltage and current limiting resistance R_S. Fig. 19.12 shows the desired circuit of series voltage regulator.

(*i*) *Zener breakdown voltage.* The collector-emitter terminals are in series with the load. Therefore, the load current must pass through the transistor *i.e.*,

$$\text{Collector current, } I_C = 1\ \text{A}$$
$$\text{Base current, } I_B = I_C/\beta = 1\ \text{A}/50 = 20\ \text{mA}$$

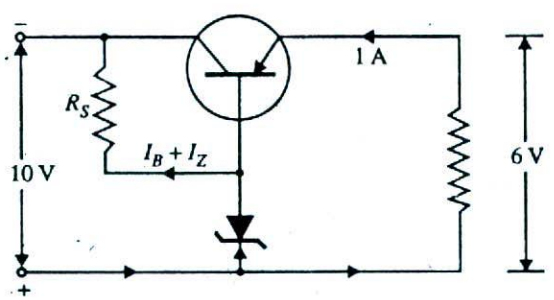


Fig. 19.12

$$\text{Output voltage, } V_{out} = V_Z - V_{BE}$$
or $$6 = V_Z - 0.5$$
$\therefore$ $$V_Z = 6 + 0.5 = \mathbf{6.5\ V}$$

Hence Zener diode of breakdown voltage 6.5V is required.

(*ii*) *Value of R_S*

$$\text{Voltage across } R_S = V_{in} - V_Z = 10 - 6.5 = 3.5\ \text{V}$$
$\therefore$ $$R_S = \frac{\text{Voltage across } R_S}{I_B + I_Z} = \frac{3.5\ \text{V}}{(20+10)\ \text{mA}} = \mathbf{117\,\Omega}$$

Example 19.9. *For the series voltage regulator shown in Fig. 19.13, calculate (i) output voltage and (ii) zener current.*

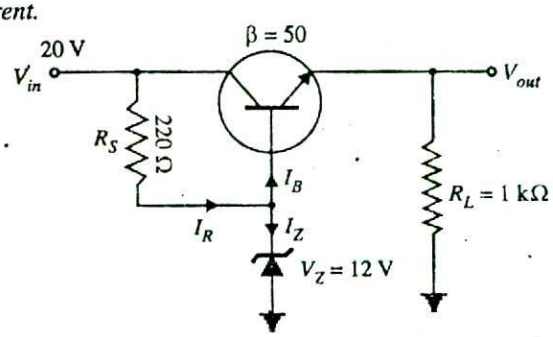


Fig. 19.13

Solution.

(*i*) $V_{out} = V_Z - V_{BE} = 12 - 0.7 = \mathbf{11.3\ V}$

(*ii*) Voltage across $R_S = V_{in} - V_Z = 20 - 12 = 8$ V

Current through R_S, $I_R = \dfrac{8\text{ V}}{220\ \Omega} = 36.4$ mA

Load current, $I_L = \dfrac{V_{out}}{R_L} = \dfrac{11.3\text{ V}}{1\text{ k}\Omega} = 11.3$ mA

Base current, $I_B = \dfrac{I_C}{\beta} = \dfrac{11.3}{50} = 0.226$ mA

$\therefore$ Zener current, $I_Z = I_R - I_B = 36.4 - 0.226 \simeq \mathbf{36\ mA}$

19.7 Series Feedback Voltage Regulator

Fig. 19.14 shows the circuit of series feedback voltage regulator. It employs principles of negative feedback to hold the output voltage almost constant despite changes in line voltage and load current. The transistor Q_2 is called a *pass transistor* because all the load current passes through it. The sample and adjust circuit is the voltage divider that consists of R_1 and R_2. The voltage divider samples the output voltage and delivers a negative feedback voltage to the base of Q_1. The feedback voltage V_F controls the collector current of Q_1.

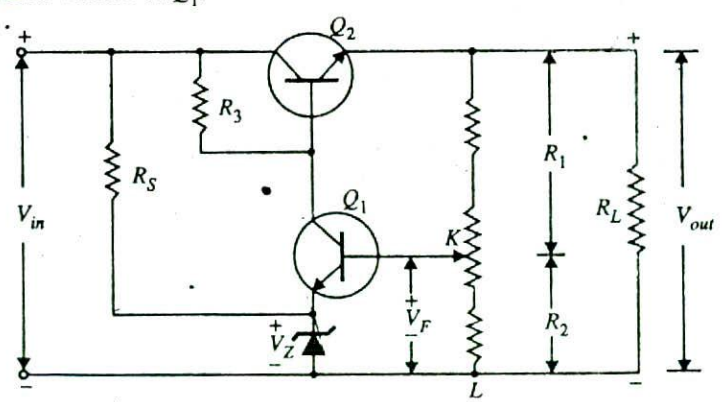


Fig. 19.14

Operation. The unregulated d.c. supply is fed to the voltage regulator. The circuit maintains

constant output voltage irrespective of the variations in load or input voltage. Here is how the circuit operates.

(*i*) Suppose the output voltage increases due to any reason. This causes an increase in voltage across KL (*i.e.*, R_2) as it is a part of the output circuit. This in turn means that more V_F is fed back to the base of transistor Q_1; producing a large collector current of Q_1. Most of this collector current flows through R_3 and causes the base voltage of Q_2 to decrease. This results in less output voltage *i.e.*, increase in voltage is offset. Thus output voltage remains constant.

(*ii*) Similiarly, if output voltage tries to decrease, the feedback voltage V_F also decreases. This reduces the current through Q_1 and R_3. This means more base voltage at Q_2 and more output voltage. Consequently, the output voltage remains at the original level.

Output Voltage. The voltage divider $R_1 - R_2$ provides the feedback voltage.

$$\text{Feedback fraction, } m = \frac{V_F}{V_{out}} = \frac{R_2}{R_1 + R_2}$$

$$\text{Closed loop voltage gain, } A_{CL} = \frac{1}{m} = \frac{R_1 + R_2}{R_2} = 1 + \frac{R_1}{R_2}$$

Now $V_F = V_Z + V_{BE}$

or $m V_{out} = V_Z + V_{BE}$ $(\because V_F = m V_{out})$

or $V_{out} = \dfrac{V_Z + V_{BE}}{m}$

or $V_{out} = A_{CL}(V_Z + V_{BE})$ $(\because 1/m = A_{CL})$

Therefore, the regulated output voltage is equal to closed-loop voltage gain times the sum of zener voltage and base-emitter voltage.

19.8 Short-Circuit Protection

The main drawback of any series regulator is that the pass transistor can be destroyed by excessive load current if the load is accidentally shorted. To avoid such an eventuality, a current limiting circuit is added to a series regulator as shown in Fig. 19.15. A current limiting circuit consists of a transistor (Q_3) and a series resistor (R_4) that is connected between base and emitter terminals.

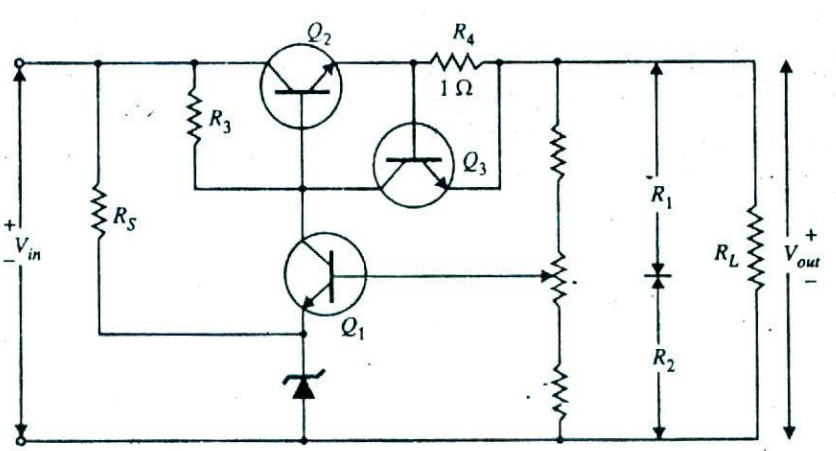


Fig. 19.15

(*i*) When the load current is normal, the voltage across R_4 (= voltage across base-emitter of Q_3) is small and Q_3 is *off. Under this condition, the circuit works as described earlier.

(*ii*) If load current becomes excessive, the voltage across R_4 becomes large enough to turn on Q_3. The collector current of Q_3 flows through R_3, thereby decreasing the base voltage of Q_2. The decrease in base voltage of Q_2 reduces the conduction of pass transistor (*i.e.*, Q_2), preventing any further increase in load current. Thus, the load current for the circuit is limited to about 700 mA.

Example 19.10. *In the series feedback voltage regulator shown in Fig. 19.15, R_1 = 2 k Ω, R_2 = 1 kΩ, V_Z = 6 V and V_{BE} = 0.7 V. What is the regulated output voltage?*

Solution.

$$\text{Feedback fraction, } m = \frac{R_2}{R_1 + R_2} = \frac{1}{2+1} = \frac{1}{3}$$

$$\therefore \quad \text{Closed-loop voltage gain, } A_{CL} = \frac{1}{m} = 3$$

$$\therefore \quad \text{Regulated output voltage, } V_{out} = A_{CL}(V_Z + V_{BE})$$
$$= 3\,(6 + 0.7) = \mathbf{20.1\ V}$$

Example 19.11. *In the series feedback circuit shown in Fig. 19.15, R_1 = 30 kΩ and R_2 = 10 kΩ. What is the closed loop voltage gain?*

Solution. $$\text{Feedback fraction, } m = \frac{R_2}{R_1 + R_2} = \frac{10}{30+10} = \frac{1}{4}$$

$$\therefore \quad \text{Closed-loop voltage gain, } A_{CL} = \frac{1}{m} = \mathbf{4}$$

19.9 Transistor Shunt Voltage Regulator

A shunt voltage regulator provides regulation by shunting current away from the load to regulate the output voltage. Fig. 19.16 shows the circuit of shunt voltage regulator. The voltage drop across series resistance depends upon the current supplied to the load R_L. The output voltage is equal to the sum of zener voltage (V_Z) and transistor base-emitter voltage (V_{BE}) *i.e.*,

$$V_{out} = V_Z + V_{BE}$$

If the load resistance decreases, the current through base of transistor decreases. As a result, less collector current is shunted. Therefore, the load current becomes larger, thereby maintaining the regulated voltage across the load. Reverse happens should the load resistance increase.

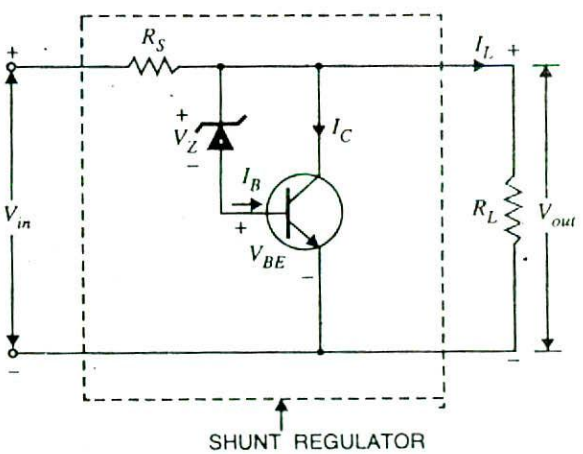


Fig. 19.16

---

* In order that Q_3 is ON, voltage across R_4 must be about 0.7 V. This means that load current then is I_L = 0.7V/ 1 Ω = 700 mA. Therefore, if load current is less than 700 mA, Q_3 is off. If load current is more than 700 mA, Q_3 will be turned on.

Drawbacks. A shunt voltage regulator has the following drawbacks :

(*i*) A large portion of the total current through R_S flows through transistor rather than to the load.

(*ii*) There is considerable power loss in R_S.

(*iii*) There are problems of overvoltage protection in this circuit.

For these reasons, a series voltage regulator is preferred over the shunt voltage regulator.

Example 19.12. *Determine the (i) regulated voltage and (ii) various currents for the shunt regulator shown in Fig. 19.17.*

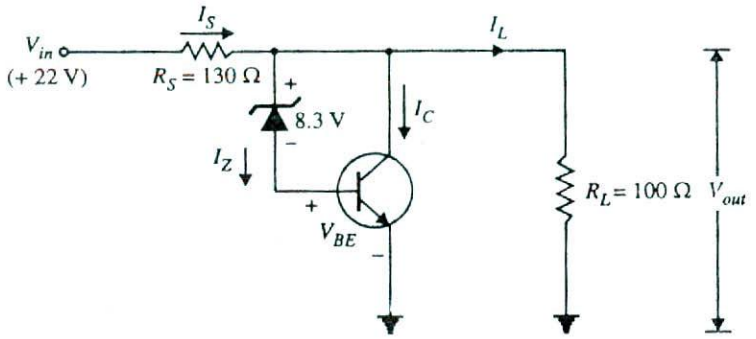


Fig. 19.17

Solution. (*i*) Output voltage, $V_{out} = V_Z + V_{BE} = 8.3 + 0.7 = 9\text{V}$

(*ii*) Load current, $I_L = \dfrac{V_{out}}{R_L} = \dfrac{9\text{ V}}{100\,\Omega} = \mathbf{90\ mA}$

Current through R_S, $I_S = \dfrac{V_{in} - V_{out}}{R_S} = \dfrac{22 - 9}{130} = \dfrac{13\text{ V}}{130\,\Omega} = \mathbf{100\ mA}$

$\therefore$ Collector current, $I_C = I_S - I_L = 100 - 90 = \mathbf{10\ mA}$

19.10 Glow-Tube Voltage Regulator

As discussed in chapter 6, when a glow tube (cold cathode gas diode) is operated in the *normal glow region*, the voltage across the tube remains constant over a wide range of tube current. This characteristic permits it to be used as a voltage regulator. Fig. 19.18 shows the circuit of a glow-tube voltage regulator. The unregulated d.c. input voltage must exceed the striking voltage of the tube. Once the gas in the tube ionises, the voltage across the tube and the load will drop to the ionising voltage. The tube will maintain constant voltage so long as the input d.c. voltage is greater than this value. The resistance R_S is used to limit the input current.

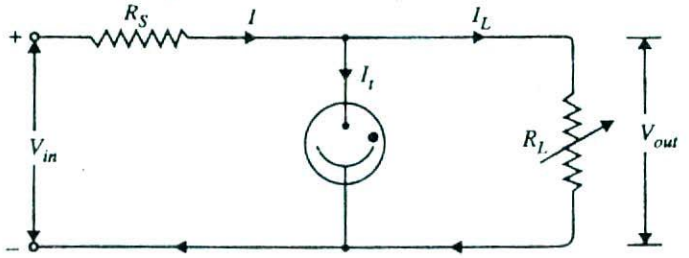


Fig. 19.18

Operation. The glow tube will maintain constant voltage across the load inspite of the changes in load current or input voltage. Now, should the load decrease, the output voltage would tend to increase. The glow tube will draw more current *without any increase in the output voltage. Meanwhile, the drop in load current is offset by the increase in tube current and the current through R_S remains constant. As output voltage = $V_{in} - I R_S$, therefore, output voltage remains unchanged. Similarly, the circuit will maintain constant output voltage if the input voltage changes. Suppose the input voltage decreases due to any reason. This would result in less current flow through the glow tube. Consequently, the voltage drop across R_S decreases, resulting in constant voltage across the load.

19.11 Series Triode Voltage Regulator

Fig. 19.19 shows the circuit of a series triode voltage regulator. It is similar to series transistor regulator except that here triode and glow tube are used instead of transistor and zener diode. The resistance R and glow tube (V.R.) help to maintain constant potential across the load. A potentiometer R_p is connected across the glow tube and its variable point is connected to the grid of the triode.

Operation. The d.c. input V_{in} from the unregulated power supply is fed to the voltage regulator. The circuit will maintain constant output voltage (V_{out}) inspite of changes in load current or input voltage. The output voltage is given by ;

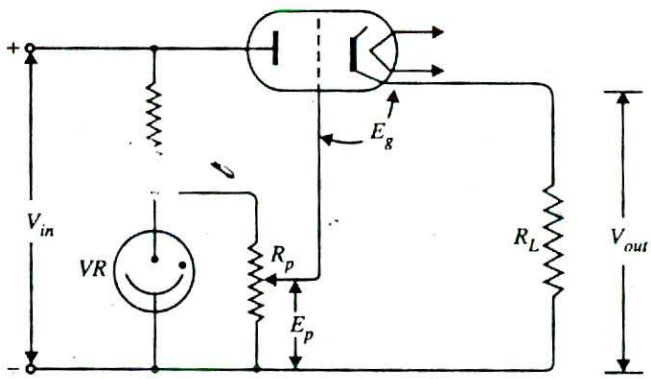


Fig. 19.19

$$V_{out} = E_p + E_g$$

Now, E_p is constant because the glow tube is operating in the normal glow region. Also grid voltage E_g is constant because it hardly depends upon plate current. Therefore, output will remain accurately fixed at one value. Any increase in the output voltage causes greater voltage drop across the limiting resistance R, tending to restore the output voltage to the original value.

19.12 Series Double Triode Voltage Regulator

Fig. 19.20 shows the circuit of a series double triode voltage regulator. Triodes T_1 and T_2 are used as direct coupled feedback amplifier in which output voltage variations are returned as feedback to oppose the input changes. The glow tube VR maintains the cathode of triode T_2 at constant potential w.r.t. ground. The triode T_2 functions as a control tube and obtains bias from the potentiometer R_3. The resistances R_3 and R_4 are range limiting resistors. The capacitor across VR tube helps to minimise the tendency of the circuit to generate audio frequency oscillations.

---

* More current will cause further ionisation, decreasing the tube resistance. Therefore, voltage across the tube remains unchanged.

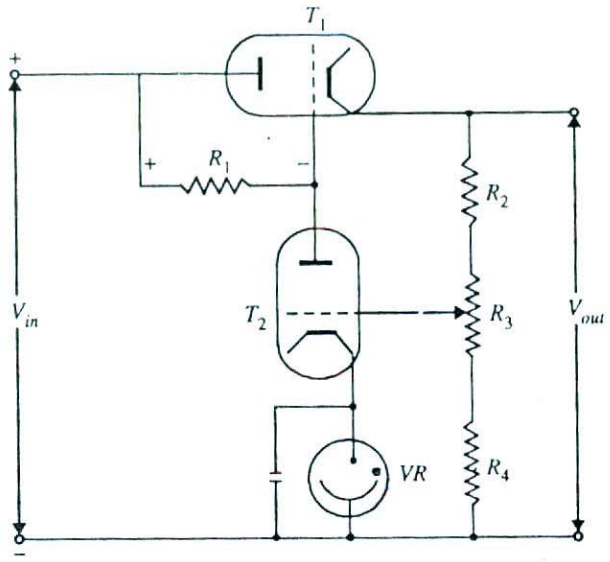


Fig. 19.20

Operation. The unregulated d c. supply is fed to the voltage regulator. The circuit will produce an output voltage (V_{out}) which is independent of changes in input voltage and of changes in the load over a wide range. With a decrease in load or increase in the input voltage, there would be tendency for the voltage across the resistive network R_2, R_3, and R_4 to rise. The result is that voltage on the grid of triode T_2 becomes less negative. The triode T_2 then conducts more current and a greater current flows through R_1 which causes a greater voltage drop across this resistor. The increase in voltage across R_1 will raise the negative potential on the grid of triode T_1. This increases the resistance of T_1 and hence the voltage across it. The rise in voltage across T_1 tends to decrease the output voltage. The reverse would be true should the load increase or input voltage decrease.

Multiple-Choice Questions

1. In an unregulated power supply, if load current increases, the output voltage .....
   (*i*) remains the same
   (*ii*) decreases (*iii*) increases
   (*iv*) none of the above
2. In an unregulated power supply, if input a.c. voltage increases, the output voltage .....
   (*i*) increases (*ii*) decreases
   (*iii*) remains the same
   (*iv*) none of the above
3. A power supply which has a voltage regulation of ..... is unregulated power supply.
   (*i*) 0 % (*ii*) 0.5 %
   (*iii*) 10 % (*iv*) 0.8 %
4. Commercial power supplies have voltage regulation .....
   (*i*) of 10 % (*ii*) of 15 %
   (*iii*) of 25 % (*iv*) within 1 %
5. An ideal regulated power supply is one which has voltage regulation of .....
   (*i*) 0 % (*ii*) 5 %
   (*iii*) 10 % (*iv*) 1 %
6. A zener diode utilises ..... characteristic for voltage regulation.
   (*i*) forward (*ii*) reverse
   (*iii*) both forward and reverse
   (*iv*) none of the above
7. Zener diode can be used as .....
   (*i*) d.c. voltage regulator only
   (*ii*) a.c. voltage regulator only
   (*iii*) both d.c. and a.c. voltage regulator
   (*iv*) none of the above

8. A zener diode is used as a ..... voltage regulating device.
   (*i*) shunt (*ii*) series
   (*iii*) series-shunt (*iv*) none of the above
9. As the junction temperature increases, the voltage breakdown point for zener mechanism .....
   (*i*) is increased (*ii*) is decreased
   (*iii*) remains the same
   (*iv*) none of the above
10. The rupture of co-valent bonds will occur when the electric field is .....
    (*i*) 100 V/cm (*ii*) 0.6 V/cm
    (*iii*) 1000 V/cm
    (*iv*) more than 10^5 V/cm
11. In a 15 V zener diode, the breakdown mechanism will occur by .....
    (*i*) avalanche mechanism
    (*ii*) zener mechanism
    (*iii*) both zener and avalanche mechanism
    (*iv*) none of the above
12. A zener diode that has very narrow depletion layer will breakdown by ..... mechanism.
    (*i*) avalanche (*ii*) zener
    (*iii*) both avalanche and zener
    (*iv*) none of the above
13. As the junction temperature increases, the voltage breakdown point for avalanche mechanism .....
    (*i*) remains the same
    (*ii*) decreases (*iii*) increases
    (*iv*) none of the above
14. Another name for zener diode is ..... diode.
    (*i*) breakdown (*ii*) voltage
    (*iii*) power (*iv*) current
15. Zener diodes are generally made of .....
    (*i*) germanium (*ii*) silicon
    (*iii*) carbon (*iv*) none of the above
16. For increasing the voltage rating, zeners are connected in.....
    (*i*) parallel (*ii*) series-parallel
    (*iii*) series (*iv*) none of the above
17. In a zener voltage regulator, the changes in load current produce changes in .....
    (*i*) zener current (*ii*) zener voltage
    (*iii*) zener voltage as well as zener current
    (*iv*) none of the above
18. A zener voltage regulator is used for ..... load currents.
    (*i*) high (*ii*) very high
    (*iii*) moderate (*iv*) small
19. A zener voltage regulator will cease to act as a voltage regulator if zener current becomes .....
    (*i*) less than load current
    (*ii*) zero
    (*iii*) more than load current
    (*iv*) none of the above
20. If the doping level is increased, the breakdown voltage of the zener .....
    (*i*) remains the same
    (*ii*) is increased (*iii*) is decreased
    (*iv*) none of the above
21. A 30 V zener will have depletion layer width ..... that of 10 V zener.
    (*i*) more than (*ii*) less than
    (*iii*) equal to (*iv*) none of the above
22. The current is a zener diode is limited by .....
    (*i*) external resistance
    (*ii*) power dissipation
    (*iii*) both (*i*) and (*ii*)
    (*iv*) none of the above
23. A 5 m A change in zener current produces a 50 mV change in zener voltage. What is the zener impedance ?
    (*i*) 1 Ω (*ii*) 0.1 Ω
    (*iii*) 100 Ω (*iv*) 10 Ω
24. A certain regulator has a no-load voltage of 6 V and a full-load output of 5.82 V. What is the load regulation ?
    (*i*) 3.09 % (*ii*) 2.87 %
    (*iii*) 5.72 % (*iv*) none of the above
25. What is true about the breakdown voltage in a zener diode ?

(*i*) It decreases when load current increases.

(*ii*) It destroys the diode.

(*iii*) It equals current times the resistance.

(*iv*) It is approximately constant.

26. Which of these is the best description for a zener diode ?

(*i*) It is a diode.

(*ii*) It is a constant-current device.

(*iii*) It is a constant-voltage device.

(*iv*) It works in the forward region.

27. A Zener diode .....

(*i*) is a battery

(*ii*) acts like a battery in the breakdown region

(*iii*) has a barrier potential of 1 V

(*iv*) is forward biased

28. The load voltage is approximately constant when a zener diode is .....

(*i*) forward biased

(*ii*) unbiased

(*iii*) reverse biased

(*iv*) operating in the breakdown region

29. In a loaded zener regulator, which is the largest zener current ?

(*i*) series current (*ii*) zener current

(*iii*) load current (*iv*) none of the above

30. If the load resistance decreases in a zener regulator, then zener current .....

(*i*) decreases (*ii*) stays the same

(*iii*) increases (*iv*) none of the above

31. If the input a.c. voltage to unregulated or ordinary power supply increases by 5 %, what will be the approximate change in d.c. output voltage ?

(*i*) 10 % (*ii*) 20 %

(*iii*) 15 % (*iv*) 5 %

32. If the load current drawn by unregulated power supply increases, the d.c. output voltage .....

(*i*) increases (*ii*) decreases

(*iii*) stays the same (*iv*) none of the above

33. If a power supply has no-load and full-load voltages of 30 V and 25 V respectively, then percentage voltage regulation is .....

(*i*) 10 % (*ii*) 20 %

(*iii*) 15 % (*iv*) none of the above

34. A power supply has a voltage regulation of 1 %. If the no-load voltage is 20 V, what is the full-load voltage ?

(*i*) 19.8 V (*ii*) 15.7 V

(*iii*) 18.6 V (*iv*) 17.2 V

35. Two similar 15 V zeners are connected in series. What is the regulated output voltage?

(*i*) 15 V (*ii*) 7.5 V

(*iii*) 30 V (*iv*) 45 V

36. A power supply can deliver a maximum rated current of 0.5 A at full-load output voltage of 20 V. What is the minimum load resistance that you can connect across the supply?

(*i*) 10 Ω (*ii*) 20 Ω

(*iii*) 15 Ω (*iv*) 40 Ω

37. In a regulated power supply, two similar 15 V zeners are connected in series. The input voltage is 45 V d.c. If each zener has a maximum current rating of 300 mA, what should be the value of series resistance ?

(*i*) 10 Ω (*ii*) 50 Ω

(*iii*) 25 Ω (*iv*) 40 Ω

38. A zener regulator ..... in the power supply.

(*i*) increases the ripple

(*ii*) decreases the ripple

(*iii*) neither increases nor decreases ripple

(*iv*) data insufficient

39. When load current is zero, the zener current will be .....

(*i*) zero (*ii*) minimum

(*iii*) maximum (*iv*) none of the above

40. The zener current will be minimum when .....

(*i*) load current is maximum

(*ii*) load current is minimum

(*iii*) load current is zero

(*iv*) none of the above

Answers to Multiple-Choice Questions

1. (*ii*)	**2.** (*i*)	**3.** (*iii*)	**4.** (*iv*)	**5.** (*i*)
6. (*ii*)	**7.** (*iii*)	**8.** (*i*)	**9.** (*ii*)	**10.** (*iv*)
11. (*i*)	**12.** (*ii*)	**13.** (*iii*)	**14.** (*i*)	**15.** (*ii*)
16. (*iii*)	**17.** (*i*)	**18.** (*iv*)	**19.** (*ii*)	**20.** (*iii*)
21. (*i*)	**22.** (*iii*)	**23.** (*iv*)	**24.** (*i*)	**25.** (*iv*)
26. (*iii*)	**27.** (*ii*)	**28.** (*iv*)	**29.** (*i*)	**30.** (*i*)
31. (*iv*)	**32.** (*ii*)	**33.** (*ii*)	**34.** (*i*)	**35.** (*iii*)
36. (*iv*)	**37.** (*ii*)	**38.** (*ii*)	**39.** (*iii*)	**40.** (*i*)

Chapter Review Topics

1. What do you understand by unregulated power supply ? Draw the circuit of such a supply.
2. What are the limitations of unregulated power supply ?
3. What do you understand by regulated power supply ? Draw the block diagram of such a supply.
4. Write a short note on the need for regulated power supply.
5. Explain the action of a zener voltage regulator with a neat diagram.
6. Write short notes on the following :
   (*i*) Transistor series voltage regulator
   (*ii*) Negative feedback voltage regulator
   (*iii*) Glow tube voltage regulator
7. What are the limitations of transistorised power supplies ?
8. Draw the circuit of a most practical valve operated power supply and explain its working.

Discussion Questions

1. Why do you prefer d.c. power supply to batteries ?
2. How can you improve the regulation of an ordinary power supply ?
3. How does zener maintain constant voltage across load in the breakdown region?
4. Why is ionising potential of glow tube less than striking potential ?
5. What is the practical importance of voltage regulation in power supplies ?

20

Solid-State Switching Circuits

Introduction

In practice, it is often required to make or break an electrical circuit in many operations. In some applications, it is desirable and necessary that this make and break should be very quick and without sparking. The mechanical switches cannot be used for the purpose for two main reasons. Firstly, a mechanical switch has high inertia which limits its speed of operation. Secondly, there is sparking at the contacts during breaking operation which results in the burning of the contacts.

The researches in the past years have revealed that tubes and transistors can serve as switching devices. They can turn ON or OFF power in an electrical circuit at a very high speed without any sparking. Such switches are known as electronic switches. The electronic switches are being extensively used to produce non-sinusoidal waves *e.g.*, square, rectangular, triangular or saw-tooth waves. Solid-state switching circuits are finding increasing applications. For example, solid-state switching circuits are the fundamental components of modern computer systems. In this chapter, we shall confine our attention to transistor as a switch. Once the reader gets acquainted with the switching action of a transistor, he can continue to study digital electronics on his/her own.

20.1 Switching Circuit

A circuit which can turn ON or OFF current in an electrical circuit is known as a **switching circuit.**

A switching circuit essentially consists of two parts *viz.* (*i*) a switch and (*ii*) associated circuitry. The switch is the most important part of the switching circuit. It actually makes or breaks the electrical circuit. The function of associated circuitry is to help the switch in turning ON or OFF current in the circuit. It may be worthwhile to mention here that associated circuitry is particularly used with electronic switches.

20.2 Switch

A switch is a device that can turn ON or OFF current in an electrical circuit. It is the most important part of a switching circuit. The switches can be broadly classified into the following three types :

(*i*) Mechanical switch

(*ii*) Electro-mechanical switch or Relay

(*iii*) Electronic switch

Although the basic purpose of this chapter is to discuss the switching action of a transistor, yet a brief description of mechanical and electromechanical switches is being presented. This will help the reader to understand the importance of transistor as a switch.

20.3 Mechanical Switch

A switch which is operated mechanically to turn ON or OFF current in an electrical circuit is known as a **mechanical switch.**

The familiar example of a mechanical switch is the tumbler switch used in homes to turn ON or OFF power supply to various appliances such as fans, heaters, bulbs etc. The action of a mechanical switch can be beautifully understood by referring to Fig. 20.1 where a load R_L is connected in series with a battery and a mechanical switch S. As long as the switch is open, there is no current in the circuit. When switch is closed, the current flow is established in the circuit. It is easy to see that the whole current flows through the load as well as the switch.

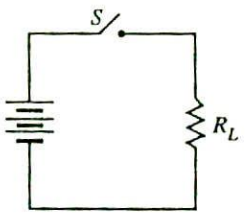


Fig. 20.1

Limitations. A mechanical switch suffers from the following drawbacks :

(*i*) In the closed position, the switch carries the whole of the load current. For a large load current, the switch contacts have to be made heavy to enable them to carry the necessary current without overheating. This increases the size of the switch.

(*ii*) If the load current carried by the circuit is large, there will be sparking at the contacts of the switch during breaking operation. This results in the wear and tear of the contacts.

(*iii*) Due to high inertia of a mechanical switch, the speed of operation is very small.

Due to above limitations, the use of mechanical switches is restricted to situations where switching speed is small and the load current to be handled is not very heavy.

20.4 Electro-mechanical Switch or Relay

It is a mechanical switch which is operated electrically to turn ON or OFF current in an electrical circuit.

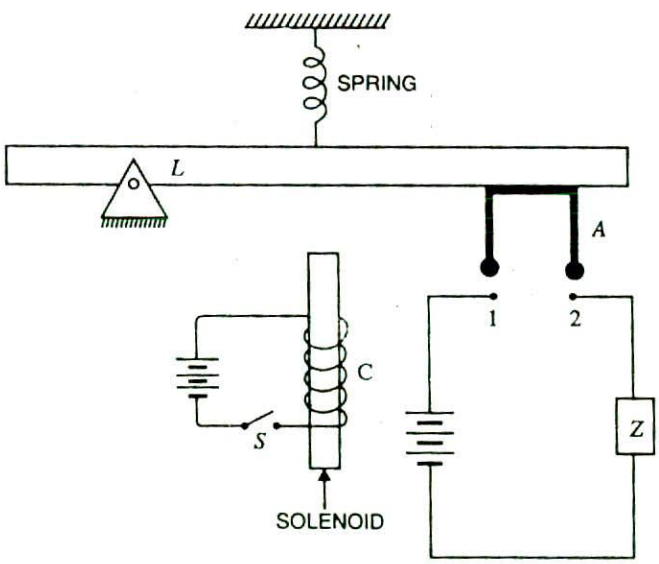


Fig. 20.2

The electro-mechanical switch or relay is an improved form of simple mechanical switch. Fig. 20.2 shows the schematic diagram of a typical relay. It consists of lever L carrying armature A and a

solenoid C. The spring pulls the lever upwards while the solenoid when energised pulls it downwards. The solenoid circuit is so designed that when switch S is closed, the downward pull of the solenoid exceeds the upward pull of the spring.

When the switch S is closed, the lever is pulled downward and the armature A closes the relay contacts 1 and 2. This turns ON current in the circuit. However, when switch S is opened, the solenoid is de-energised and the spring pulls the lever and hence the armature A upwards. Consequently, the relay contacts 1 and 2 are opened and current flow in the circuit is interrupted. In this way, a relay acts as a switch.

Advantages. A relay possesses the following advantages over a simple mechanical switch :

(*i*) The relay or electro-mechanical switch requires a small power for its operation. This permits to control a large power in the load by a small power to the relay circuit. Thus a relay acts as a power amplifier *i.e.* it combines control with power amplification.

(*ii*) The switch in the relay coil carries a small current as compared to the load current. This permits the use of a smaller switch in the relay coil circuit.

(*iii*) The operator can turn ON or OFF power to a load even from a distance. This is a very important advantage when high voltages are to be handled.

(*iv*) There is no danger of sparking as the turning ON or OFF is carried by the relay coil switch which carries a small current.

However, a relay has two principal limitations. First, the speed of operation is very small; less than 5 operations per second. Secondly, a relay has moving parts and hence there is considerable wear and tear.

20.5 Electronic Switches

It is a device which can turn ON or OFF current in an electrical circuit with the help of electronic devices e.g., transistors or tubes.

Electronic switches have become very popular because of their high speed of operation and absence of sparking. A transistor can be used as a switch by driving it back and forth between *saturation* and *cut off*. This is illustrated in the discussion below :

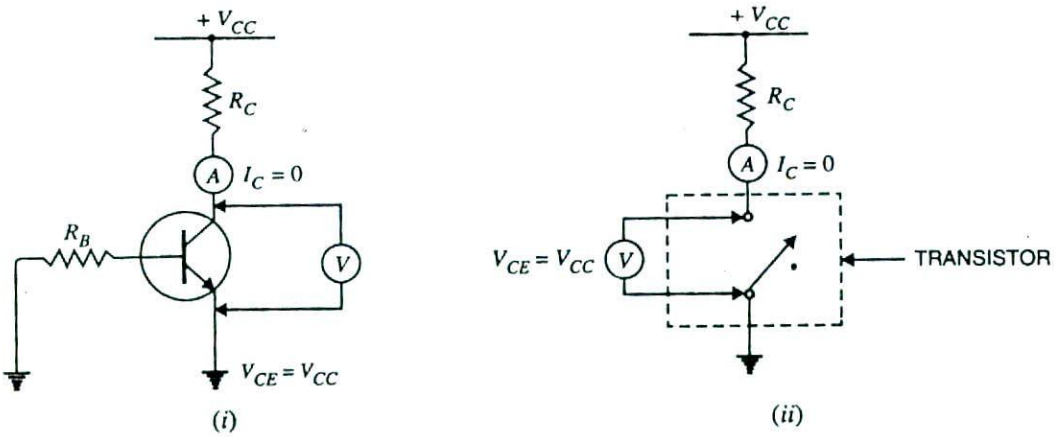


Fig. 20.3

(*i*) When the base input voltage is enough negative, the transistor is cut off and no current flows in collector load [See Fig. 20.3 (*i*)]. As a result, there is no voltage drop acorss R_C and the output

voltage is *ideally V_{CC}. *i.e.*,

$$I_C = 0 \quad \text{and} \quad V_{CE} = V_{CC}$$

This condition is similar to that of an open switch (*i.e.*, OFF state) as shown in Fig. 20.3 (*ii*).

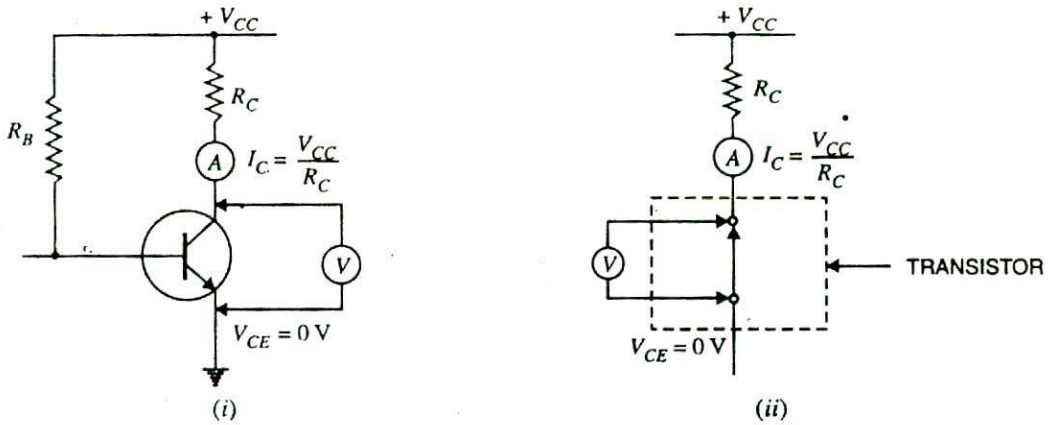


Fig. 20.4

(*ii*) When the input base voltage is positive enough that transistor saturates, then $I_{C(sat)}$ will flow through R_C. Under such conditions, the entire V_{CC} will drop across collector load R_C and output voltage is ideally zero *i.e.*,

$$I_C = I_{C(sat)} = \frac{V_{CC}}{R_C} \quad \text{and} \quad V_{CE} = 0$$

This condition is similar to that of a closed switch (*i.e.*, ON state) as shown in Fig. 20.4 (*ii*).

Conclusion. The above discussion leads to the conclusion that a transistor can behave as a switch under proper conditions. In other words, if the input base voltages are enough negative and positive, the transistor will be driven between *cut off* and *saturation*. These conditions can be easily fulfilled in a transistor circuit. Thus a transistor can act as a switch. Fig. 20.5 shows the switching action of a transistor in terms of dc load line. The point *A* of the load line represents the ON condition while point *B* represents the OFF condition.

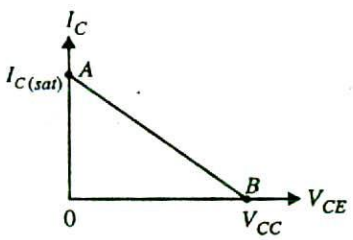


Fig. 20.5

Example 20.1. *Determine the minimum high input voltage (+V) required to saturate the transistor switch shown in Fig. 20.6.*

Solution. Assuming the transistor to be ideal,

$$I_{C(sat)} = V_{CC}/R_C = 10 \text{ V}/1 \text{ k}\Omega = 10 \text{ mA}$$

$$\therefore \quad I_B = \frac{I_{C(sat)}}{\beta} = \frac{10 \text{ mA}}{100} = 0.1 \text{ mA}$$

Now $+V = I_B R_B + V_{BE}$

---

* The collector current will not be zero since a little leakage current always flows even when the base input voltage is negative or zero.

$\therefore$ Output voltage $= V_{CC} - I_{leakage} R_C$. If $I_{leakage} = 0$, then output voltage $= V_{CC}$

$= (0.1 \text{ mA})(47 \text{ k}\Omega) + 0.7$

$= 4.7 + 0.7 = \mathbf{5.4\ V}$

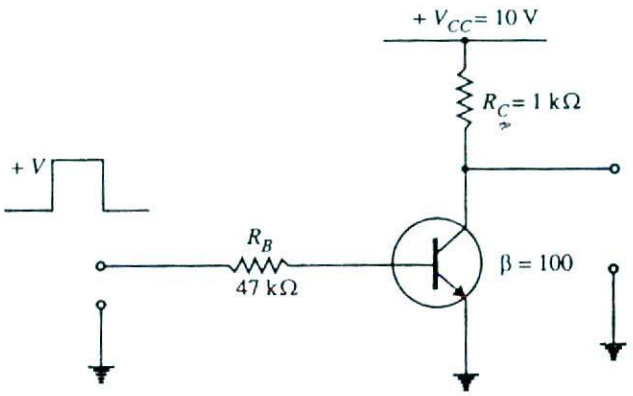


Fig. 20.6

Hence in order to saturate the transistor, we require + 5.4 V.

20.6 Advantages of Electronic Switches

The following are the advantages of transistor switch over other types of switches :

(*i*) It has no moving parts and hence there is little wear and tear. Therefore, it gives noiseless operation.

(*ii*) It has smaller size and weight.

(*iii*) It gives troublefree service because of solid state.

(*iv*) It is cheaper than other switches and requires little maintenance.

(*v*) It has a very fast speed of operation say upto 10^9 operations per second. On the other hand, the mechanical switches have a small speed of operation *e.g.* less than 5 operations in a second.

20.7. Important Terms

So far we have considered the transistor to be an ideal one. An ideal transistor has $V_{CE} = V_{CC}$ (or $I_C = 0$) in the OFF state and $V_{CE} = 0$ (or $I_C = I_{C(sat)}$) in the ON state. However, such ideal conditions are not realised in practice. In a practical transistor, the output voltage is neither V_{CC} in the OFF state nor it is zero in the ON state. While designing a transistor switching circuit, these points must be taken into consideration.

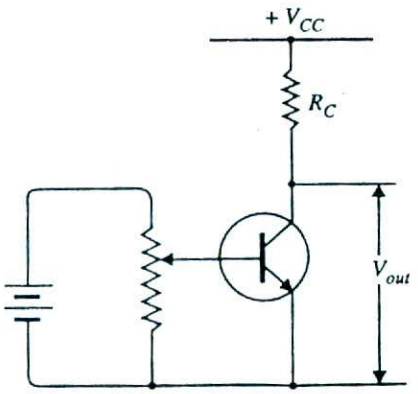


Fig. 20.7

(*i*) **Collector leakage current.** When the input circuit is reverse biased or input voltage is zero, a small current (a few μA) flows in the collector. This is known as collector leakage current and is due to the minority carriers. The value of this leakage current is quite large in *Ge* transistors, but in modern silicon transistors, the value of leakage current is low enough to be ignored.

(*ii*) **Saturation collector current.** *It is the maximum collector current for a particular load in a transistor.*

Consider an *npn* transistor having a load R_C in its collector circuit as shown in Fig. 20.7. As the

input forward bias is increased, the collector current I_C also increases because $I_C = \beta I_B$. However, with the increase in I_C, the voltage drop across R_C increases. This results in the *decrease of V_{CE}. When V_{CE} drops to knee voltage (V_{knee}), any further increase in collector current is not possible since β decreases sharply when V_{CE} falls below knee voltage. This maximum current is known as saturation collector current.

$$\therefore \quad \text{Saturation collector current, } I_{C(sat)} = \frac{V_{CC} - V_{knee}}{R_C}$$

20.8 Switching Transistors

A transistor which is used as a switch is known as a **switching transistor.**

In general, switching transistor is fabricated by the same process as an ordinary transistor except that it has special design features to reduce switch-off time and saturation voltage. It is so arranged in the circuit that either maximum current (called saturation collector current) flows through the load or minimum current (called collector leakage current) flows through the load. In other words, a switching transistor has two states *viz.* (*i*) ON state or when collector saturation current flows through the load (*ii*) OFF state or when collector leakage current flows through the load. In the discussion that follows transistor means the switching transistor.

20.9 Switching Action of a Transistor

The switching action of a transistor can also be explained with the help of output characteristics. Fig. 20.8 shows the output characteristics of a typical transistor for a *CE* configuration. The load line is drawn for load R_C and collector supply V_{CC}. The characteristics are arranged in three regions : OFF, ON or saturation and active regions.

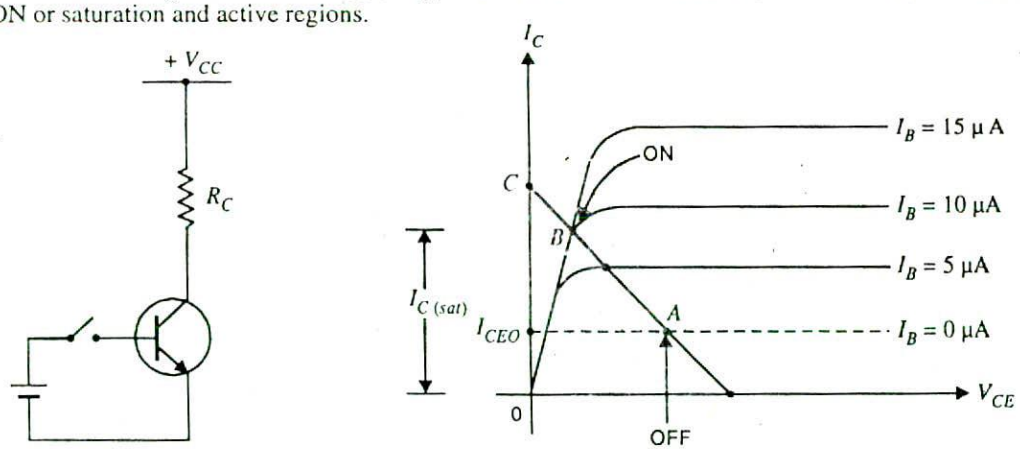


Fig. 20.8

(*i*) **OFF region.** When the input base voltage is zero or negative, the transistor is said to be in the OFF condition. In this condition, $I_B = 0$ and the collector current is equal to the collector leakage current I_{CEO}. The value of I_{CEO} can be obtained from the characteristics if we know V_{CE}.

$$\text{Power loss} = \text{Output voltage} \times \text{Output current}$$

As already noted, in the OFF condition, the output voltage = V_{CC} since voltage drop in the load due to I_{CEO} is negligible.

$$\therefore \quad \text{Power loss} = V_{CC} \times I_{CEO}$$

---

* $V_{CE} = V_{CC} - I_C R_C$

Since I_{CEO} is very small as compared to full-load current that flows in the ON condition, power loss in the transistor is quite small in the OFF condition. It means that the transistor has a high efficiency as a switch in the OFF condition.

(*ii*) **ON or saturation region.** When the input voltage is made so much positive that saturation collector current flows, the transistor is said to be in the ON condition. In this condition, the saturation collector current is given by ;

$$I_{C(sat)} = \frac{V_{CC} - V_{knee}}{R_C}$$

$$\text{Power loss} = \text{Output voltage} \times \text{Output current}$$

The output voltage in the ON condition is equal to V_{knee} and output current is $I_{C(sat)}$.

$$\therefore \quad \text{Power loss} = V_{knee} \times I_{C(sat)}$$

Again the efficiency of transistor as a switch in the ON condition is high. It is because the power loss in this condition is quite low due to small value of V_{knee}.

(*iii*) **Active region.** *It is the region that lies between OFF and ON conditions.*

The OFF and ON regions are the stable regions of operation. The active region is the unstable (or transient) region through which the operation of the transistor passes while changing from OFF state to the ON state. Thus referring to Fig. 20.8, the path *AB* is the active region. The collector current increases from I_{CEO} to $I_{C(sat)}$ along the path *AB* as the transistor is switched ON. However, when the transistor is switched OFF, the collector current decreases from $I_{C(sat)}$ to I_{CEO} along *BA*.

20.10 Multivibrators

An electronic circuit that generates square waves (or other non-sinusoidals such as rectangular, saw-tooth waves) is known as a ***multivibrator.**

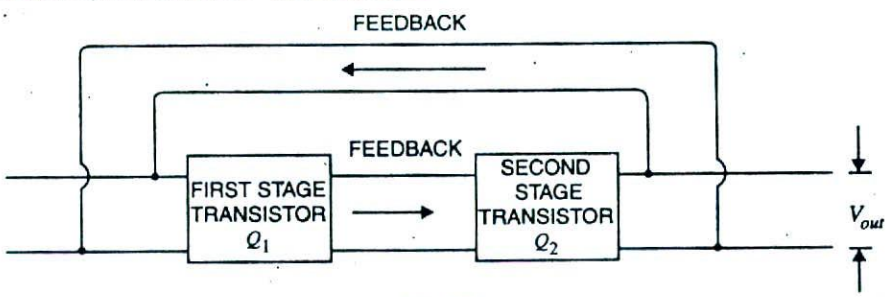


Fig. 20.9

A multivibrator is a switching circuit which depends for operation on positive feedback. It is basically a two-stage amplifier with output of one fedback to the input of the other as shown in Fig. 20.9.

The circuit operates in two states (*viz* ON and OFF) controlled by circuit conditions. Each amplifier stage supplies feedback to the other in such a manner that will drive the transistor of one stage to saturation (ON state) and the other to cut off (OFF state).

After a certain time controlled by circuit conditions, the action is reversed *i.e.* saturated stage is driven to cut off and the cut off stage is driven to saturation. The output can be taken across either stage and may be rectangular or square wave depending upon the circuit conditions.

Fig. 20.9 shows the block diagram of a multivibrator. It is a two-stage amplifier with 100%

* The name multivibrator is derived from the fact that a square wave actually consists of a large number of (fourier series analysis) sinusoidals of different frequencies.

positive feedback. Suppose output is taken across the transistor Q_2. At any particular instant, one transistor is ON and conducts $I_{C(sat)}$ while the other is OFF. Suppose Q_2 is ON and Q_1 is OFF. The collector current in Q_2 will be $I_{C(sat)}$ as shown in Fig. 20.10. This condition will prevail for a time (bc in this case) determined by circuit conditions. After this time, transistor Q_2 is cut off and Q_1 is turned ON. The collector current in Q_2 is now I_{CEO} as shown. The circuit will stay in this condition for a time de. Again Q_2 is turned ON and Q_1 is driven to cut off. In this way, the output will be a square wave.

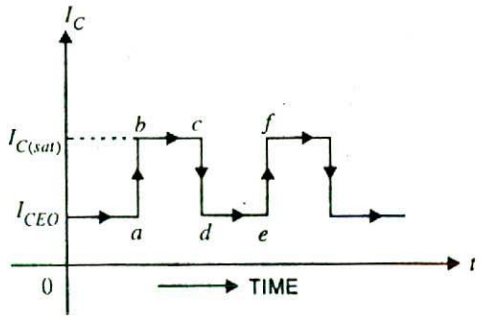


Fig. 20.10

20.11 Types of Multivibrators

A multivibrator is basically a two-stage amplifier with output of one fedback to the input of the other. At any particular instant, one transistor is ON and the other is OFF. After a certain time depending upon the circuit components, the stages reverse their conditions – the conducting stage suddenly cuts off and the non-conducting stage suddenly starts to conduct. The two possible states of a multivibrator are :

	ON	OFF
First State	Q_1	Q_2
Second State	Q_2	Q_1

Depending upon the manner in which the two stages interchange their states, the multivibrators are classified as :

(*i*) Astable or free running multivibrator

(*ii*) Monostable or one-shot multivibrator

(*iii*) Bi-stable or flip-flop multivibrator.

Fig. 20.11 shows the input/output relations for the three types of multivibrators.

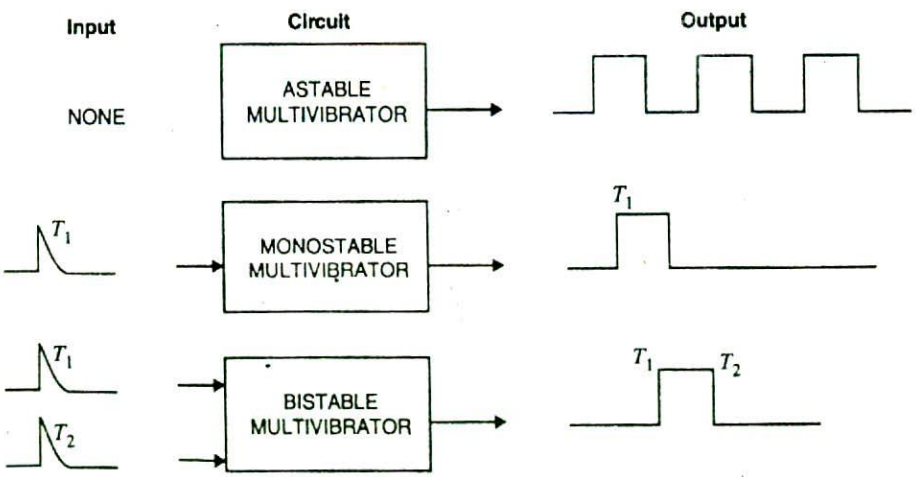


Fig. 20.11

(*i*) The astable or free running multivibrator alternates automatically between the two states and remains in each for a time dependent upon the circuit constants. Thus it is just an oscillator since it requires no external pulse for its operation. Of course, it does require a source of d.c. power. Because it continuously produces the square-wave output, it is often referred to as a *free running multivibrator.*

(*ii*) The monostable or one-shot multivibrator has one state stable and one quasi-stable (*i.e.* half-stable) state. The application of input pulse triggers the circuit into its quasi-stable state, in which it remains for a period determined by circuit constants. After this period of time, the circuit returns to its initial stable state, the process is repeated upon the application of each trigger pulse. Since the monostable multivibrator produces a single output pulse for each input trigger pulse, it is generally called *one-shot multivibrator.*

(*iii*) The bistable multivibrator has both the two states stable. It requires the application of an external triggering pulse to change the operation from either one state to the other. Thus one pulse is used to generate half-cycle of square wave and another pulse to generate the next half-cycle of square wave. It is also known as a *flip-flop multivibrator* because of the two possible states it can assume.

20.12 Transistor Astable Multivibrator

A multivibrator which generates square waves of its own (i.e. without any external triggering pulse) is known as an **astable** *or* **free running multivibrator.**

The *astable multivibrator has no stable state. It switches back and forth from one state to the other, remaining in each state for a time determined by circuit constants. In other words, at first one transistor conducts (*i.e.* ON state) and the other stays in the OFF state for some time. After this period of time, the second transistor is automatically turned ON and the first transistor is turned OFF. Thus the multivibrator will generate a square wave output of its own. The width of the square wave and its frequency will depend upon the circuit constants.

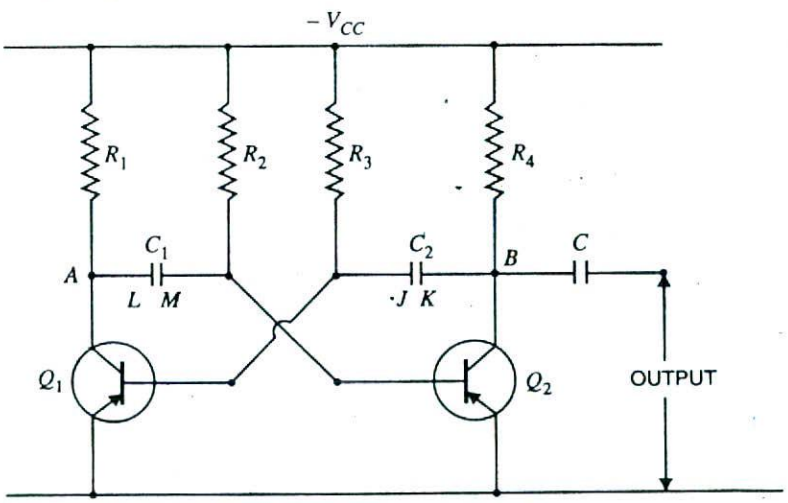


Fig. 20.12

Circuit details. Fig. 20.12 shows the circuit of a typical transistor astable multivibrator using two identical transistors Q_1 and Q_2. The circuit essentially consists of two symmetrical *CE* amplifier stages, each providing a feedback to the other. Thus collector loads of the two stages are equal *i.e.*

* A means not. Hence astable means that it has no stable state.

$R_1 = R_4$ and the biasing resistors are also equal *i.e.* $R_2 = R_3$. The output of transistor Q_1 is coupled to the input of Q_2 through C_1 while the output of Q_2 is fed to the input of Q_1 through C_2. The square wave output can be taken from Q_1 or Q_2.

Operation. When V_{CC} is applied, collector currents start flowing in Q_1 and Q_2. In addition, the coupling capacitors C_1 and C_2 also start charging up. As the characteristics of no two transistors (*i.e.* β, V_{BE}) are *exactly* alike, therefore, one transistor, say Q_1, will conduct more rapidly than the other. The rising collector current in Q_1 drives its collector more and more positive. The increasing positive output at point A is applied to the base of transistor Q_2 through C_1. This establishes a reverse bias on Q_2 and its collector current starts decreasing. As the collector of Q_2 is connected to the base of Q_1 through C_2, therefore, base of Q_1 becomes more negative *i.e.* Q_1 is more forward biased. This further increases the collector current in Q_1 and causes a further decrease of collector current in Q_2. This series of actions is repeated until the circuit drives Q_1 to saturation and Q_2 to cut off. These actions occur very rapidly and may be considered practically instantaneous. The output of Q_1 (ON state) is approximately zero and that of Q_2 (OFF state) is approximately V_{CC}. This is shown by *ab* in Fig. 20.13.

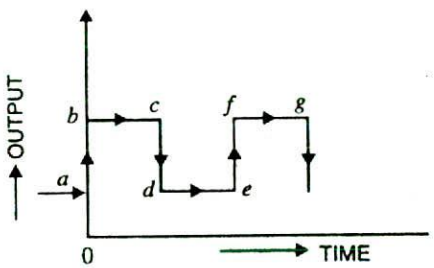


Fig. 20.13

When Q_1 is at saturation and Q_2 is cut off, the full voltage V_{CC} appears across R_1 and voltage across R_4 will be zero. The charges developed across C_1 and C_2 are sufficient to maintain the saturation and cut off conditions at Q_1 and Q_2 respectively. This condition is represented by time interval *bc* in Fig. 20.13. However, the capacitors will not retain the charges indefinitely but will discharge through their respective circuits. The discharge path for C_1, with plate L negative and Q_1 conducting, is $LAQ_1V_{CC}R_2M$ as shown in Fig. 20.14 (*i*).

The discharge path for C_2, with plate K negative and Q_2 cut off, is KBR_4R_3J as shown in Fig. 20.14 (*ii*). As the resistance of the discharge path for C_1 is lower than that of C_2, therefore, C_1 will discharge more rapidly.

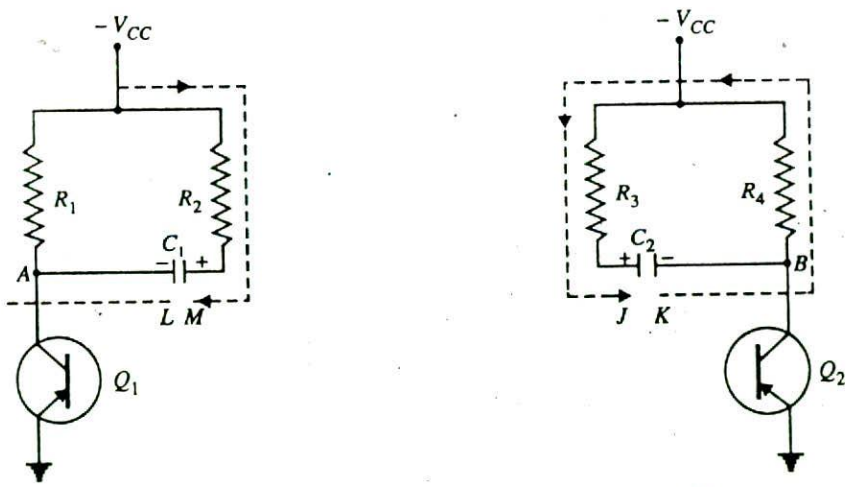


Fig. 20.14

As C_1 discharges, the base bias at Q_2 becomes less positive and at a time determined by R_2 and C_1, forward bias is re-established at Q_2. This causes the collector current to start in Q_2. The increasing positive potential at collector of Q_2 is applied to the base of Q_1 through the capacitor C_2. Hence the base of Q_1 will become more positive *i.e.* Q_1 is reverse biased. The decrease in collector current in Q_1 sends a negative voltage to the base of Q_2 through C_1, thereby causing further increase in the collector current of Q_2. With this set of actions taking place, Q_2 is quickly driven to saturation and Q_1 to cut off. This condition is represented by *cd* in Fig. 20.13. The period of time during which Q_2 remains at saturation and Q_1 at cut off is determined by C_2 and R_3.

ON or OFF time. The time for which either transistor remains ON or OFF is given by :

ON time for Q_1 (or OFF time for Q_2) is

$$T_1 = 0.694\, R_2 C_1$$

OFF time for Q_1 (or ON time for Q_2)

$$T_2 = 0.694\, R_3 C_2$$

Total time period of the square wave is

$$T = T_1 + T_2 = 0.694\,(R_2 C_1 + R_3 C_2)$$

As $R_2 = R_3 = R$ and $C_1 = C_2 = C$,

$$\therefore \quad T = 0.694\,(RC + RC) \simeq 1.4\, RC \text{ seconds}$$

Frequency of the square wave is

$$f = \frac{1}{T} \simeq \frac{0.7}{RC} \text{ Hz}$$

It may be noted that in these expressions, R is in ohms and C in farad.

Example 20.2. *In the astable multivibrator shown in Fig. 20.12, $R_2 = R_3 = 10\ k\Omega$ and $C_1 = C_2 = 0.01\ \mu F$. Determine the time period and frequency of the square wave.*

Solution.

Here $R = 10\ k\Omega = 10^4\ \Omega$; $C = 0.01\ \mu F = 10^{-8}$ F

Time period of the square wave is

$$T = 1.4\, RC = 1.4 \times 10^4 \times 10^{-8} \text{ second}$$
$$= 1.4 \times 10^{-4} \text{ second} = 1.4 \times 10^{-4} \times 10^3 \text{ m sec}$$
$$= \mathbf{0.14\ m\ sec}$$

Frequency of the square wave is

$$f = \frac{1}{T \text{ in second}} \text{ Hz} = \frac{1}{1.4 \times 10^{-4}} \text{ Hz}$$
$$= 7 \times 10^3 \text{ Hz} = \mathbf{7\ kHz}$$

20.13 Transistor Monostable Multivibrator

A multivibrator in which one transistor is always conducting (i.e. in the ON state) and the other is non-conducting (i.e. in the OFF state) is called a **monostable multivibrator.**

A *monostable multivibrator has only one state stable. In other words, if one transistor is conducting and the other is non-conducting, the circuit will remain in this position. It is only with the application of external pulse that the circuit will interchange the states. However, after a certain time, the circuit will automatically switch back to the original stable state and remains there until another pulse is applied. Thus a monostable multivibrator cannot generate square waves of its own like an

* Mono means single.

astable multivibrator. Only external pulse will cause it to generate the square wave.

Circuit details. Fig. 20.15 shows the circuit of a transistor monostable multivibrator. It consists of two similar transistors Q_1 and Q_2 with equal collector loads *i.e.* $R_1 = R_4$. The values of V_{BB} and R_5 are such as to reverse bias Q_1 and keep it at cut off. The collector supply V_{CC} and R_2 forward bias Q_2 and keep it at saturation. The input pulse is given through C_2 to obtain the square wave. Again output can be taken from Q_1 or Q_2.

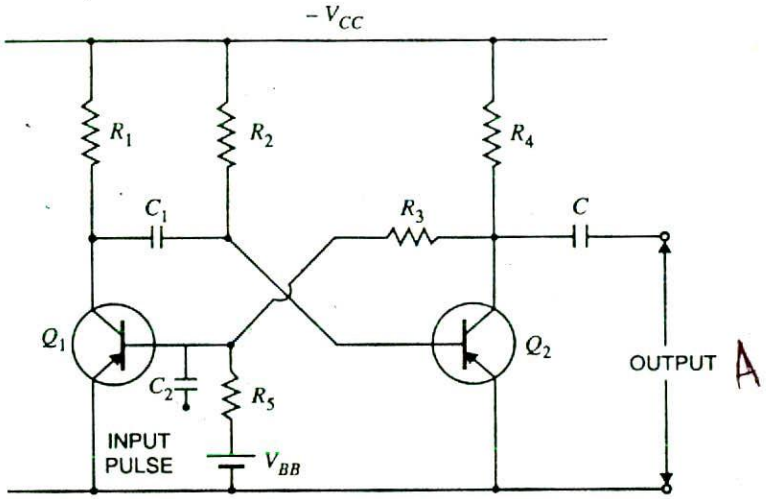


Fig. 20.15

Operation. With the circuit arrangement shown, Q_1 is at cut off and Q_2 is at saturation. This is the stable state for the circuit and it will continue to stay in this state until a triggering pulse is applied at C_2. When a negative pulse of short duration and sufficient magnitude is applied to the base of Q_1 through C_2, the transistor Q_1 starts conducting and positive potential is established at its collector. The positive potential at the collector of Q_1 is coupled to the base of Q_2 through capacitor C_1. This decreases the forward bias on Q_2 and its collector current decreases. The increasing negative potential on the collector of Q_2 is applied to the base of Q_1 through R_3. This further increases the forward bias on Q_1 and hence its collector current. With this set of actions taking place, Q_1 is quickly driven to saturation and Q_2 to cut off.

With Q_1 at saturation and Q_2 at cut off, the circuit will come back to the original stage (*i.e.* Q_2 at saturation and Q_1 at cut off) after some time as explained in the following discussion. The capacitor C_1 (charged to approximately V_{CC}) discharges through the path $R_2 V_{CC} Q_1$. As C_1 discharges, it sends a voltage to the base of Q_2 to make it less positive. This goes on until a point is reached when forward bias is re-established on Q_2 and collector current starts to flow in Q_2. The step by step events already explained occur and Q_2 is quickly driven to saturation and Q_1 to cut off. This is the stable state for the circuit and it remains in this condition until another pulse causes the circuit to switch over the states.

20.14 Transistor Bistable Multivibrator

A multivibrator which has both the states stable is called a **bistable multivibrator.**

The bistable multivibrator has both the states stable. It will remain in whichever state it happens to be until a trigger pulse causes it to switch to the other state. For instance, suppose at any particular instant, transistor Q_1 is conducting and transistor Q_2 is at cut off. If left to itself, the bistable multivibrator will stay in this position forever. However, if an external pulse is applied to the circuit in such a way

that Q_1 is cut off and Q_2 is turned on, the circuit will stay in the new position. Another trigger pulse is then required to switch the circuit back to its original state.

Circuit details. Fig. 20.16 shows the circuit of a typical transistor bistable multivibrator. It consists of two identical *CE* amplifier stages with output of one fed to the input of the other. The feedback is coupled through resistors (R_2, R_3) shunted by capacitors C_1 and C_2. The main purpose of capacitors C_1 and C_2 is to improve the switching characteristics of the circuit by passing the high frequency components of the square wave. This allows fast rise and fall times and hence distortionless square wave output. The output can be taken across either transistor.

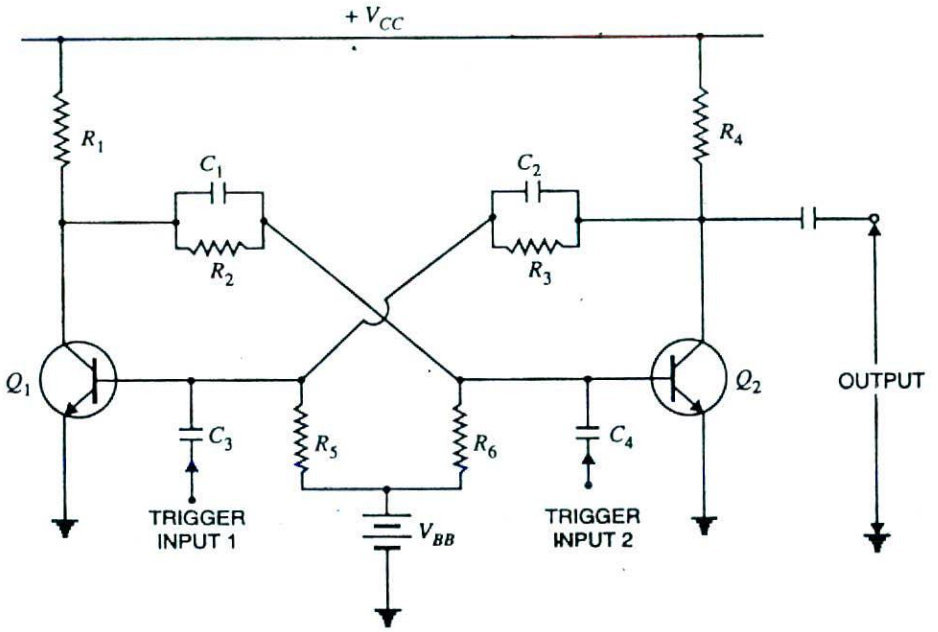


Fig. 20.16

Operation. When V_{CC} is applied, one transistor will start conducting slightly ahead of the other due to some differences in the characteristics of the transistors. This will drive one transistor to saturation and the other to cut off in a manner described for the astable multivibrator. Assume that Q_1 is turned ON and Q_2 is cut OFF. If left to itself, the circuit will stay in this condition. In order to switch the multivibrator to its other state, a trigger pulse must be applied. A negative pulse applied to the base of Q_1 through C_3 will cut it off or a positive pulse applied to the base of Q_2 through C_4 will cause it to conduct.

Suppose a negative pulse of sufficient magnitude is applied to the base of Q_1 through C_3. This will reduce the forward bias on Q_1 and cause a decrease in its collector current and an increase in collector voltage. The rising collector voltage is coupled to the base of Q_2 where it forward biases the base-emitter junction of Q_2. This will cause an increase in its collector current and decrease in collector voltage. The decreasing collector voltage is applied to the base of Q_1 where it further reverse biases the base-emitter junction of Q_1 to decrease its collector current. With this set of actions taking place, Q_2 is quickly driven to saturation and Q_1 to cut off. The circuit will now remain stable in this state until a negative trigger pulse at Q_2 (or a positive trigger pulse at Q_1) changes this state.

20.15 Differentiating Circuit

A circuit in which output voltage is directly proportional to the derivative of the input is known as a **differentiating circuit.**

$$\text{Output} \propto \frac{d}{dt}(\text{Input})$$

A differentiating circuit is a simple RC series circuit with output taken across the resistor R. The circuit is suitably designed so that output is proportional to the derivative of the input. Thus if a d.c. or constant input is applied to such a circuit, the output will be zero. It is because the derivative of a constant is zero.

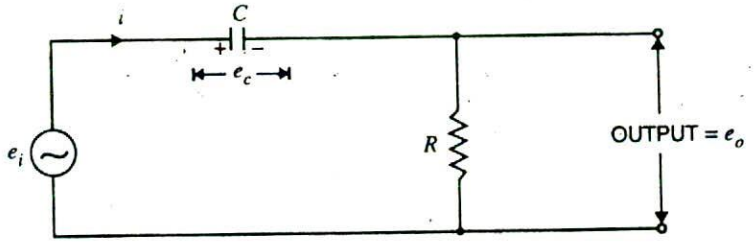


Fig. 20.17

Fig. 20.17 shows a typical differentiating circuit. The output across R will be the derivative of the input. It is important to note that merely using voltage across R does not make the circuit a differentiator; it is also necessary to set the proper circuit values. In order to achieve good differentiation, the following two conditions should be satisfied :

(*i*) The time constant RC of the circuit should be much smaller than the time period of the input wave.

(*ii*) The value of X_C should be 10 or more times larger than R at the operating frequency.

Fulfilled these conditions, the output across R in Fig. 20.17 will be the derivative of the input.

Let e_i be the input alternating voltage and let i be the resulting alternating current. The charge q on the capacitor at any instant is

$$q = C e_c$$

Now
$$i = \frac{dq}{dt} = \frac{d}{dt}(q) = \frac{d}{dt}(C e_c)$$

or
$$i = C \frac{d}{dt}(e_c)$$

Since the capacitive reactance is very much larger than R, the input voltage can be considered equal to the capacitor voltage with negligible error *i.e.* $e_c = e_i$.

$$\therefore \quad i = C \frac{d}{dt}(e_i)$$

Output voltage, $e_o = i R$

$$= RC \frac{d}{dt}(e_i)$$

$$\therefore \propto \frac{d}{dt}(e_i) \qquad (\because RC \text{ is constant})$$

$$\therefore \quad \text{Output voltage} \propto \frac{d}{dt}(\text{Input})$$

Output waveforms. The output waveform from a differentiating circuit depends upon the time constant and shape of the input wave. Three important cases will be considered.

(*i*) **When input is a square wave.** When the input fed to a differentiating circuit is a square wave, output will consist of sharp narrow pulses as shown in Fig. 20.18. During the *OC* part of input wave, its amplitude changes abruptly and hence the differentiated wave will be a sharp narrow pulse as shown in Fig. 20.18. However, during the constant part *CB* of the input, the output will be zero because the derivative of a constant is zero.

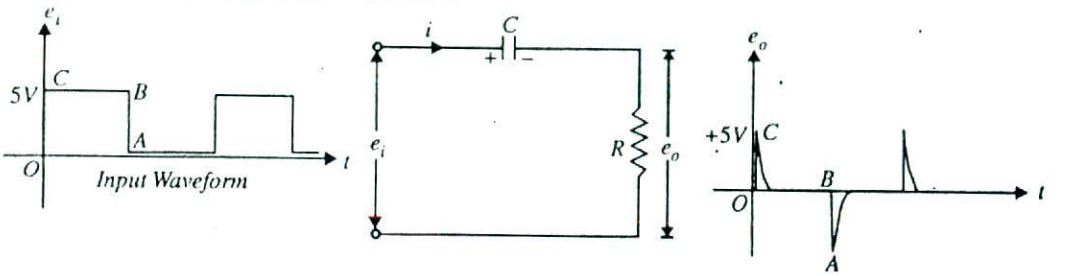


Fig. 20.18

Let us look at the physical explanation of this behaviour of the circuit. Since time constant *RC* of the circuit is very small *w.r.t* time period of input wave and $X_C >> R$, the capacitor will become fully charged during the early part of each half-cycle of the input wave. During the remainder part of the half cycle, the output of the circuit will be zero because the capacitor voltage (e_c) neutralises the input voltage and there can be no current flow through *R*. Thus we shall get sharp pulse at the output during the start of each half-cycle of input wave while for the remainder part of the half-cycle of input wave, the output will be zero. In this way, a symmetrical output wave with sharp positive and negative peaks is produced. Such pulses are used in many ways in electronic circuits *e.g.* in television transmitters and receivers, in multivibrators to initiate action etc.

(*ii*) **When input is a triangular wave.** When the input fed to a differentiating circuit is a triangular wave, the output will be a rectangular wave as shown in Fig. 20.19. During the period *OA* of the input wave, its amplitude changes at a constant rate and, therefore, the differentiated wave has a constant value for each constant rate of change. During the period *AB* of the input wave, the change is less abrupt so that the output will be a very narrow pulse of rectangular form. Thus when a triangular wave is fed to a differentiating circuit, the output consists of a succession of rectangular waves of equal or unequal duration depending upon the shape of the input wave.

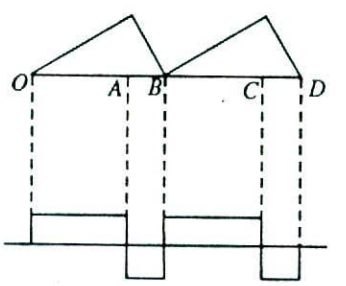


Fig. 20.19

(*iii*) **When input is a sine wave.** A sine wave input becomes a cosine wave and a cosine wave input becomes an inverted sine wave at the output.

Example 20.3. (*i*) *What is the effect of time constant of an RC circuit on the differentiated wave?*

(*ii*) *Sketch the output waveform from the differentiating circuit when input is square wave for* $T = 100\ RC$, $T = 10\ RC$, $T = RC$.

Solution.

(*i*) In an *RC* differentiating circuit, the output voltage is taken across *R* and the wave form of the output depends upon the time constant of the circuit. The circuit will function as a differentiator if the product *RC* is many times smaller than the time period of the input wave.

(*ii*) **Square wave input.** Fig. 20.20 shows the input square wave fed to a differentiating circuit. Fig. 20.21 shows the output waveforms for different values of time period of the input wave.

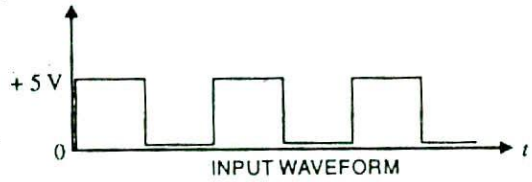


Fig. 20.20

It may be noted that *RC* coupling circuit is the same as a differentiating circuit except that it has a long time constant–in excess of 5 *RC*. Therefore, a coupling circuit does not noticeably differentiate the input wave.

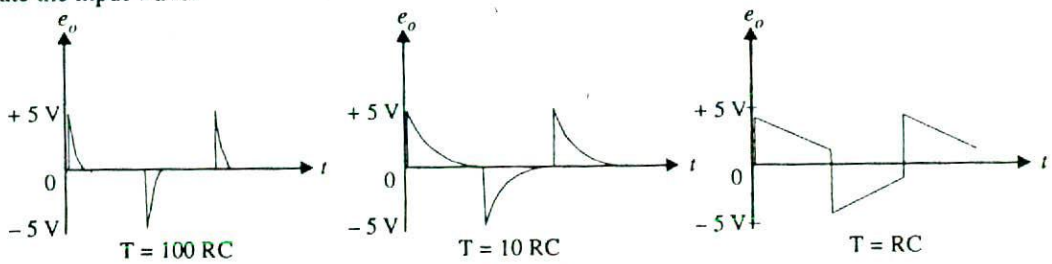


Fig. 20.21

Example 20.4. *In a differentiating circuit, R = 10 kΩ and C = 2.2 μF. If the input voltage goes from 0 V to 10 V at a constant rate in 0.4 s, determine the output voltage.*

Solution.

$$e_o = RC\frac{d}{dt}(e_i) = RC\frac{de_i}{dt}$$ ... See Art. 20.15

Here $R = 10\,\text{k}\Omega$; $C = 2.2\,\mu\text{F}$; $\frac{de_i}{dt} = \frac{10-0}{0.4} = 25\ \text{V/s}$

$\therefore$ $e_o = (10\times10^3)\times(2.2\times10^{-6})\times25 = \mathbf{0.55\ V}$

20.16 Integrating Circuit

A circuit in which output voltage is directly proportional to the integral of the input is known as an **integrating circuit** *i.e.*

$$\text{Output} \propto \int \text{Input}$$

An integrating circuit is a simple *RC* series circuit with output taken across the capacitor *C* as shown in Fig. 20.22. It may be seen that *R* and *C* of the differentiating circuit have changed places. In order that the circuit renders good integration, the following conditions should be fulfilled :

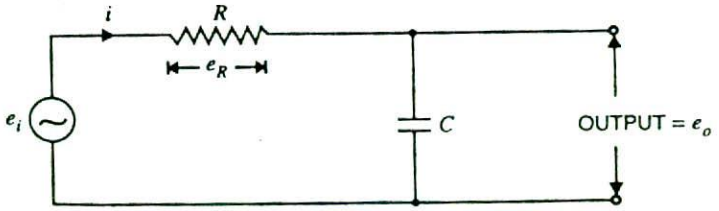


Fig. 20.22

(*i*) The time constant RC of the circuit should be very large as compared to the time period of the input wave.

(*ii*) The value of R should be 10 or more times larger than X_C.

Let e_i be the input alternating voltage and let i be the resulting alternating current. Since R is very large as compared to capacitive reactance X_C of the capacitor, it is reasonable to assume that voltage across R (*i.e.* e_R) is equal to the input voltage *i.e.*

$$e_i = e_R$$

Now
$$i = \frac{e_R}{R} = \frac{e_i}{R}$$

The charge q on the capacitor at any instant is

$$q = \int i\, dt$$

$$\text{Output voltage, } e_o = \frac{q}{C} = \frac{\int i\, dt}{C}$$

$$= \frac{\int \frac{e_i}{R} dt}{C} \qquad \left(\because i = \frac{e_i}{R}\right)$$

$$= \frac{1}{RC} \int e_i\, dt$$

$$\propto \int e_i\, dt \qquad (\because RC \text{ is constant})$$

$$\therefore \qquad \text{Output voltage} \propto \int \text{Input}$$

Output waveforms. The output waveform from an integrating circuit depends upon time constant and shape of the input wave. Two important cases will be discussed :

(*i*) **When input is a square wave.** When the input fed to an integrating circuit is a square wave, the output will be a triangular wave as shown in Fig. 20.23 (*i*). As integration means summation, therefore, output from an integrating circuit will be the sum of all the input waves at any instant. This sum is zero at A and goes on increasing till it becomes maximum at C. After this, the summation goes on decreasing to the onset of negative movement CD of the input.

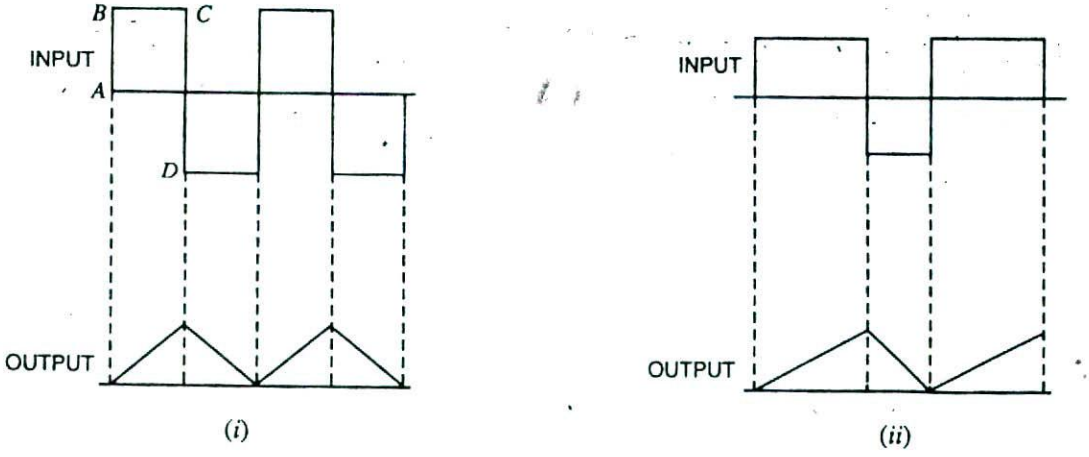


Fig. 20.23

(*ii*) **When input is rectangular wave.** When the input fed to an integrating circuit is a rectangular wave, the output will be a triangular wave as shown in Fig. 20.23 (*ii*).

20.17 Important Applications of Diodes

We have seen that diodes can be used as rectifiers. Apart from this, diodes have many other applications. However, we shall confine ourselves to the following two applications of diodes :

(*i*) as a clipper (*ii*) as a clamper

A clipper (or limiter) is used to clip off or remove a portion of an a.c. signal. The half-wave rectifier is basically a clipper that eliminates one of the alternations of an a.c. signal.

A clamper (or *dc* restorer) is used to restore or change the *dc* reference of an *ac* signal. For example, you may have a 10 V_{pp} *ac* signal that varies equally above and below 2 V *dc*.

20.18 Clipping Circuits

The circuit with which the waveform is shaped by removing (or clipping) a portion of the applied wave is known as a **clipping circuit.**

Clippers find extensive use in radar, digital and other electronic systems. Although several clipping circuits have been developed to change the wave shape, we shall confine our attention to diode clippers. These clippers can remove signal voltages above or below a specified level. The important diode clippers are (*i*) positive clipper (*ii*) biased clipper (*iii*) combination clipper.

(*i*) **Positive clipper.** A positive clipper is that which removes the positive half-cycles of the input voltage. Fig. 20.24 shows the typical circuit of a positive clipper using a diode. As shown, the output voltage has all the positive half-cycles removed or clipped off.

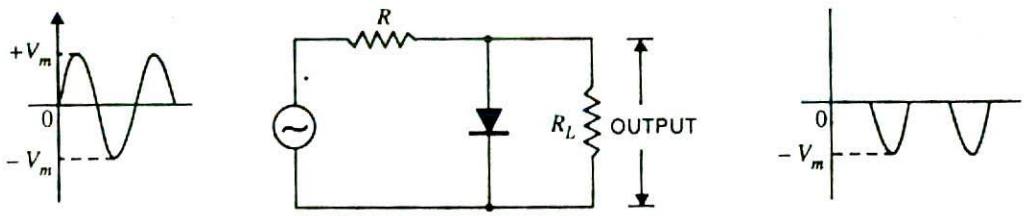


Fig. 20.24

The circuit action is as follows. During the positive half cycle of the input voltage, the diode is forward biased and conducts heavily. Therefore, the voltage across the diode (which behaves as a short) and hence across the load R_L is zero. Hence *output voltage during positive half-cycles is zero.

During the negative half-cycle of the input voltage, the diode is reverse biased and behaves as an open. In this condition, the circuit behaves as a voltage divider with an output given by ;

$$\text{Output voltage} = -\frac{R_L}{R + R_L} V_m$$

Generally, R_L is much greater than R.

$$\therefore \quad \text{Output voltage} = -V_m$$

It may be noted that if it is desired to remove the negative half-cycle of the input, the only thing to be done is to reverse the polarities of the diode in the circuit shown in Fig. 20.24. Such a clipper is then called a *negative clipper.*

(*ii*) **Biased clipper.** Sometimes it is desired to remove a small portion of positive or negative

* It may be noted that all the input voltage during this half-cycle is dropped across R.

half-cycle of the signal voltage. For this purpose, biased clipper is used. Fig. 20.25 shows the circuit of a biased clipper using a diode with a battery of V volts. With the polarities of battery shown, a portion of each positive half-cycle will be clipped. However, the negative half-cycles will appear as such across the load. Such a clipper is called *biased positive clipper.*

The circuit action is as follows. The diode will conduct heavily so long as input voltage is greater than $+V$. When input voltage is greater than $+V$, the diode behaves as a short and the output equals $+V$. The output will stay at $+V$ so long as the input voltage is greater than $+V$. During the period the input voltage is less than $+V$, the diode is reverse biased and behaves as an open. Therefore, most of the input voltage appears across the output. In this way, the biased positive clipper removes input voltage above $+V$.

During the negative half-cycle of the input voltage, the diode remains reverse biased. Therefore, almost entire negative half-cycle appears across the load.

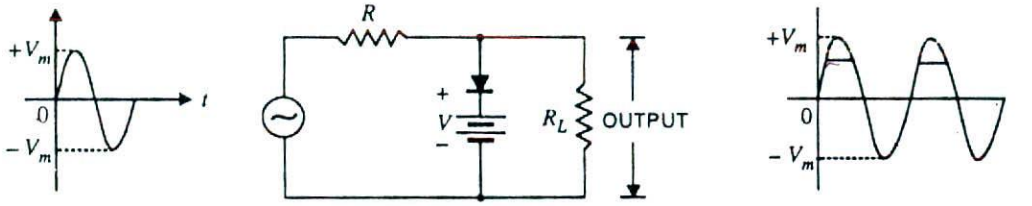


Fig. 20.25

If it is desired to clip a portion of negative half-cycles of input voltage, the only thing to be done is to reverse the polarities of diode or battery. Such a circuit is then called a *biased negative clipper.*

(iii) Combination clipper. It is a combination of biased positive and negative clippers. With a combination clipper, a portion of both positive and negative half-cycles of input voltage can be removed or clipped as shown in Fig. 20.26.

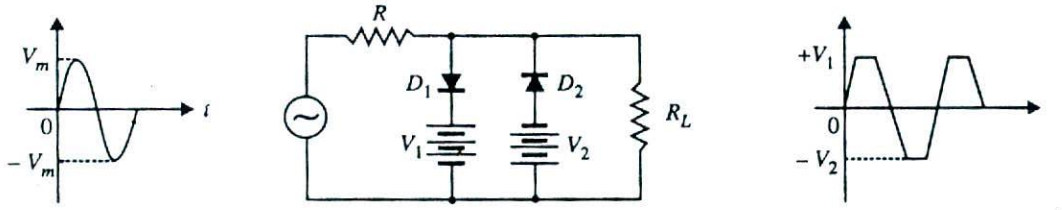


Fig. 20.26

The circuit action is as follows. When positive input voltage is greater than $+V_1$, diode D_1 conducts heavily while diode D_2 remains reverse biased. Therefore, a voltage $+V_1$ appears across the load. This output stays at $+V_1$ so long as the input voltage exceeds $+V_1$. On the other hand, during the negative half-cycle, the diode D_2 will conduct heavily and the output stays at $-V_2$ so long as the input voltage is greater than $-V_2$. Note that $+V_1$ and $-V_2$ are less than $+V_m$ and $-V_m$ respectively.

Between $+V_1$ and $-V_2$ neither diode is on. Therefore, in this condition, most of the input voltage appears across the load. It is interesting to note that this clipping circuit can give square wave output if V_m is much greater than the clipping levels.

Example 20.5. *For the negative series clipper shown in Fig.20.27, what is the peak output voltage from the circuit ?*

Solution. When the diode is connected in series with the load, it is called a series clipper. Since

it is a negative clipper, it will remove negative portion of input a.c. signal.

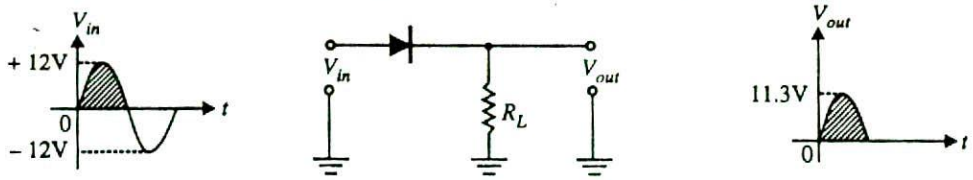


Fig. 20.27

During the positive half-cycle of input signal, the dioide is forward biased. As a result, the diode will conduct. The output voltage is

$$V_{out\,(peak)} = V_{in\,(peak)} - 0.7 = 12 - 0.7 = \mathbf{11.3\ V}$$

During the negative-half cycle of input signal, the diode is reverse biased and consequently it will not conduct. Therefore $V_{out} = 0$. Note that under this condition, the entire input voltage will appear across the diode.

Example 20.6. *The negative shunt clipper shown in Fig. 20.28 (i) has a peak input voltage of + 10 V. What is the peak output voltage from this circuit ?*

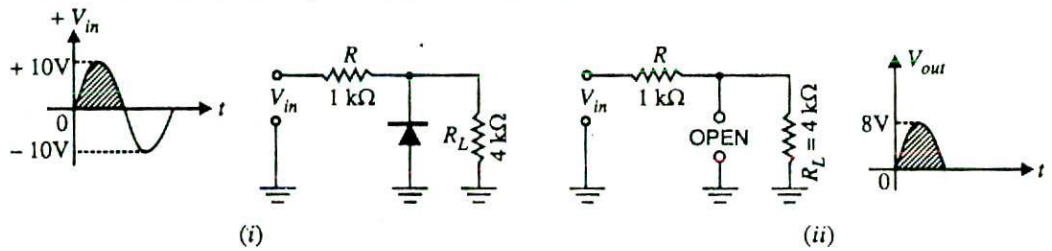


Fig. 20.28

Solution. When the diode is connected in parallel with the load, it is called a shunt clipper. During the positive half-cycle of input ac signal, the diode is reverse biased and it will behave as an open. This is shown in Fig. 20.28 (*ii*). With diode as an open,

$$V_{out\,(peak)} = \text{Peak voltage across } R_L$$

$$= \frac{R_L}{R + R_L} V_{in\,(peak)} = \frac{4}{1+4} \times 10 = \mathbf{8\ V}$$

Note that peak output voltage is somewhat less than the peak input voltage.

Example 20.7. *In example 20.6, what will be the output voltage and voltage across R when the input voltage is –10 V ?*

Solution. During the negative half cycle of input signal, the diode is forward biased. Therefore, diode can be replaced by its simplified equivalent circuit as shown in Fig. 20.29. Since load is connected in parallel with the diode,

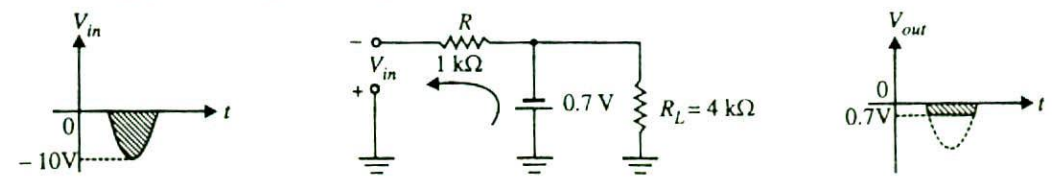


Fig. 20.29

$$\therefore \quad V_{out} = -0.7 \text{ V}$$

$$\text{Voltage across } R, \; V_R = (-10) - (-0.7) = -10 + 0.7 = -9.3 \text{ V}$$

Example 20.8. *The positive shunt clipper shown in Fig. 20.30 has the input waveform as indicated. Determine the value of V_{out} for each of the input alternations.*

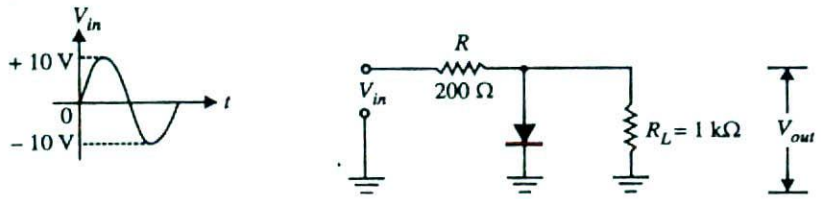


Fig. 20.30

Solution.

Positive half-cycle. During the positive half-cycle of the input ac signal, the diode is forward biased. Therefore, diode can be replaced by its simplified equivalent circuit as shown in Fig. 20.31. Since the load is connected in parallel with the diode,

$$\therefore \quad V_{out} = 0.7 \text{ V}$$

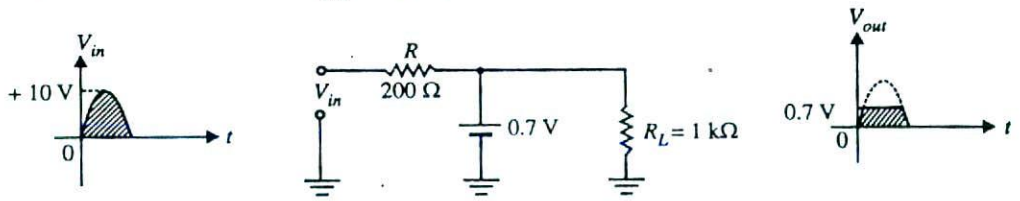


Fig. 20.31

Negative half-cycle. During the negative half-cycle of the input a.c. signal, the diode is reverse biased and it conducts no current. Therefore, the diode will behave as an open as shown in Fig. 20.32.

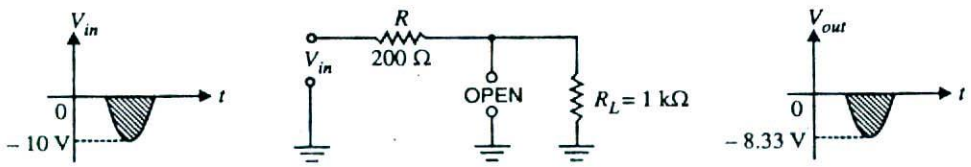


Fig. 20.32

$$\therefore \quad V_{out\,(peak)} = \frac{R_L}{R + R_L} V_{in\,(peak)}$$

$$= \left(\frac{1000}{200 + 1000} \right) (-10 \text{ V}) = -8.33 \text{ V}$$

Again the peak output voltage is somewhat less than the peak input voltage.

Example 20.9. *In Fig. 20.30, what is the purpose of using the series resistance R ?*

Solution. The purpose of series resistance R is to protect the diode from damage. Let us explain this point. Suppose the series resistance R is not in the circuit. The circuit then becomes as shown in Fig. 20.33.

During the positive half-cycle of the input signal, the diode is forward biased. Since series resistance R is not present, it is easy to see that the diode will short the signal source to the ground. As a result, excessive current will flow through the diode as well as through the signal source. This large current may damage/destroy either the diode or the signal source.

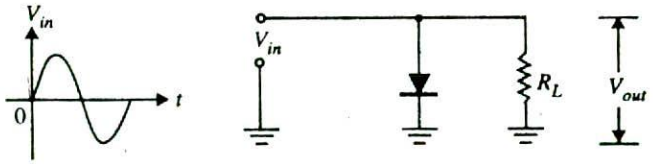


Fig. 20.33

Note. The series resistance R protects the diode and signal source when diode is forward biased. However, the presence of this resistance affects the output voltage to a little extent. It is because in a practical clipper circuit, the value of R is much lower than R_L. Consequently, output voltage will be approximately equal to V_{in} when the diode is reverse biased.

20.19 Applications of Clippers

There are numerous clipper applications and it is not possible to discuss all of them. However, in general, clippers are used to perform one of the following two functions :

(*i*) Changing the shape of a waveform

(*ii*) Circuit transient protection

(*i*) **Changing the shape of waveform.** Clippers can alter the shape of a waveform. For example, a clipper can be used to convert a sine wave into a rectangular wave, square wave etc. They can limit either the negative or positive alternation or both alternations of an a.c. voltage.

(*ii*) **Circuit Transient protection.** *Transients can cause considerable damage to many types of circuits *e.g.*, a digital circuit. In that case, a clipper diode can be used to prevent the transient form reaching that circuit.

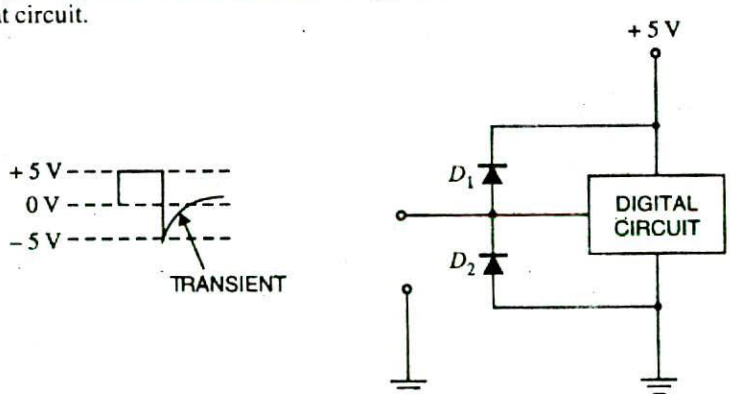


Fig. 20.34

Fig. 20.34 shows the protection of a typical digital circuit against transients by the diode clipper. When the transient shown in Fig. 20.34 occurs on the input line, it causes diode D_2 to be forward biased. The diode D_2 will conduct; thus shorting the transient to the ground. Consequently, the input of the circuit is protected from the transient.

---

* A transient is a sudden current or voltage rise that has an extremely short duration.

20.20 Clamping Circuits

A circuit that places either the positive or negative peak of a signal at a desired d.c. level is known as a **clamping circuit.**

Fig. 20.35

A clamping circuit (or a clamper) essentially adds a *d.c* component to the signal. Fig. 20.35 shows the key idea behind clamping. The input signal is a sine wave having a peak-to-peak value of 10 V. The clamper adds the *d.c.* component and pushes the signal upwards so that the negative peaks fall on the zero level. As you can see, the waveform now has peak values of +10 V and 0 V.

It may be seen that the shape of the original signal has not changed; only there is vertical shift in the signal. Such a clamper is called a *positive clamper*. The negative clamper does the reverse i.e. it pushes the signal downwards so that the positive peaks fall on the zero level.

The following points may be noted carefully :

(*i*) The clamping circuit does not change the peak-to-peak or r.m.s value of the waveform. Thus referring to Fig. 20.35 above, the input wave form and clamped output have the same peak-to-peak value *i.e.*, 10 V in this case. If you measure the input voltage and clamped output with an a.c. voltmeter, the readings will be the same.

(*ii*) A clamping circuit changes the peak and average values of a waveform. This point needs explanation. Thus in the above circuit, it is easy to see that input waveform has a peak value of 5 V and average value over a cycle is zero. The clamped output varies between 10 V and 0 V. Therefore, the peak value of clamped output is 10 V and *average value is 5 V. Hence we arrive at a very important conclusion that a clamper changes the peak value as well as the average value of a waveform.

20.21 Basic Idea of a Clamper

A clamping circuit should not change peak-to-peak value of the signal; it should only change the *dc* level. To do so, a clamping circuit uses a capacitor, together with a diode and a load resistor R_L. Fig. 20.36 shows the circuit of a positive clamper. *The operation of a clamper is based on the principle that charging time of a capacitor is made very small as compared to its discharging time.* Thus referring to Fig. 20.36,

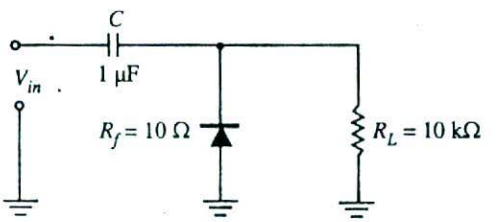


Fig. 20.36

**Charging time constant, $\tau = R_f C = (10\,\Omega) \times (10^{-6}\,\text{F}) = 10\,\mu\text{s}$

Total charging time, $\tau_C = {}^{+}5R_f C = 5 \times 10 = 50\,\mu\text{s}$

---

* Average value (or *dc* value) $= \dfrac{10 + 0}{2} = 5$ V

** When diode is forward biased.

\+ From the knowledge of electrical engineering, we know that charging time of a capacitor is $\simeq 5\,RC$.

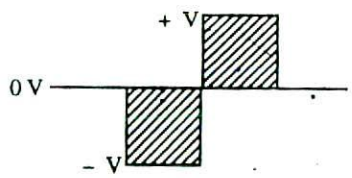
*Discharging time constant, $\tau = R_L C = (10 \times 10^3) \times (1 \times 10^{-6}) = 10$ ms

Total discharging time, $\tau_D = 5 \cdot R_L C = 5 \times 10 = 50$ ms

It may be noted that charging time (*i.e.*, 50 μs) is very small as compared to the discharging time (*i.e.*, 50 ms). This is the basis of clamper circuit operation. In a practical clamping circuit, the values of C and R_L are so chosen that discharging time is very large.

20.22 Positive Clamper

Fig. 20.37 shows the circuit of a **positive clamper. The input signal is assumed to be a square wave with time period T. The clamped output is obtained across R_L. The circuit design incorporates two main features. Firstly, the values of C and R_L are so selected that time constant $\tau = CR_L$ is very large. This means that voltage across the capacitor will not discharge significantly during the interval the diode is non conducting. Secondly, $R_L C$ time constant is deliberately made much greater than the time period T of the incoming signal.



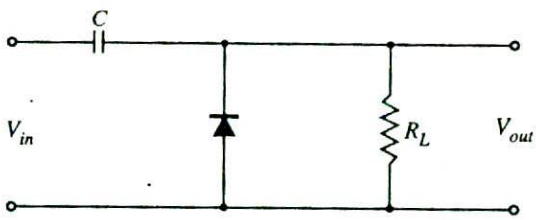


Fig. 20.37

Operation

(*i*) During the negative halfcycle of the input signal, the diode is forward biased. Therefore, the diode behaves as a short as shown in Fig. 20.38. The charging time constant (= CR_f, where R_f = forward resistance of the diode) is very small so that the capacitor will charge to V volts very quickly. It is easy to see that during this interval, the output voltage is directly across the short circuit. Therefore, $V_{out} = 0$.

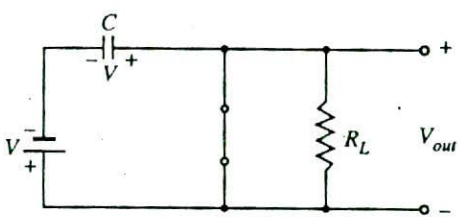


Fig. 20.38

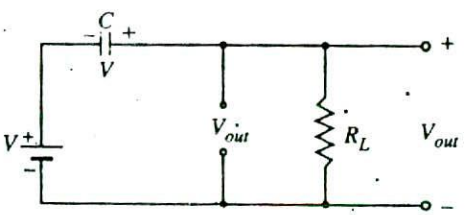


Fig. 20.39

(*ii*) When the input switches to $+V$ state (*i.e.*, positive half-cycle), the diode is reverse biased and behaves as an open as shown in Fig. 20.39. Since the discharging time constant (= CR_L) is much greater than the time period of the input signal, the capacitor remains almost fully charged to V volts during the off time of the diode. Referring to Fig. 20.39 and applying Kirchhoff's voltage law to the input loop, we have,

$$V + V - V_{out} = 0$$

---

* When diode is reverse biased.

** If you want to determine what type of clamper you are dealing with, here is an easy memory trick. If the diode is pointing up (away from ground), the circuit is a positive clamper. On the other hand, if diode is pointing down (towards ground), the circuit is a negative clamper.

or $V_{out} = 2V$

The resulting waveform is shown in Fig. 20.40. It is clear that it is a positively clamped output. That is to say the input signal has been pushed upward by V volts so that negative peaks fall on the zero level.

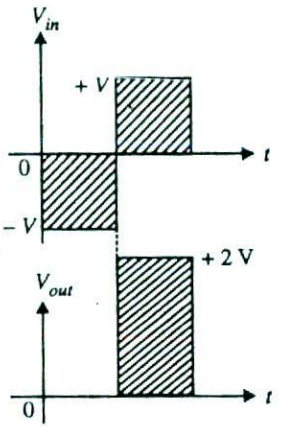


Fig. 20.40

20.23 Negative Clamper

Fig. 20.41 shows the circuit of a negative clamper. The clamped output is taken across R_L. Note that only change from the positive clamper is that the connections of diode are reversed.

(*i*) During the positive half-cycle of the input signal, the diode is forward biased. Therefore, the diode behaves as a short as shown in Fig. 20.42. The charging time constant ($= CR_f$) is very small so that the capacitor will charge to V volts very quickly. It is easy to see that during this interval, the output voltage is directly across the short circuit. Therefore, $V_{out} = 0$.

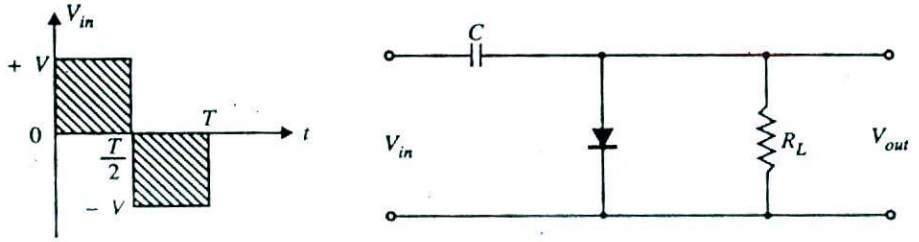


Fig. 20.41

(*ii*) When the input switches to $-V$ state (*i.e.*, negative half-cycle), the diode is reverse biased

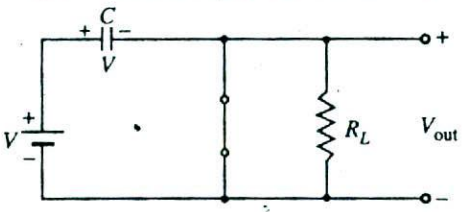


Fig. 20.42

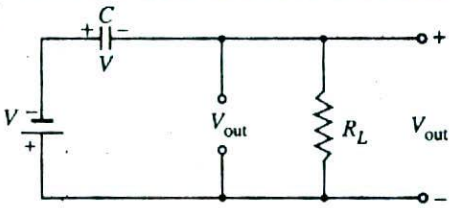


Fig. 20.43

and behaves as an open as shown in Fig. 20.43. Since the discharging time constant ($= CR_L$) is much greater than the time period of the input signal, the capacitor almost remains fully charged to V volts during the off time of the diode. Referring to Fig. 20.43 and applying Kirchhoff's voltage law to the input loop, we have,

$$-V - V - V_{out} = 0$$

or $$V_{out} = -2\,V$$

The resulting waveform is shown in Fig. 20.44. Note that total swing of the output signal is equal to the total swing of the input signal.

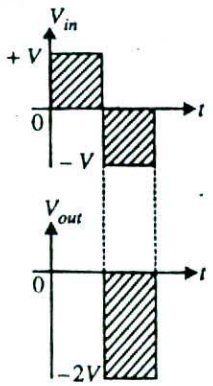


Fig. 20.44

Example 20.10. *Sketch the output waveform for the circuit shown in Fig. 20.45. It is given that discharging time constant (CR_L) is much greater than the time period of input wave.*

Fig. 20.45

Solution.

During positive half-cycle of the input signal, the diode is forward biased. The network will appear as shown in Fig. 20.46. It is clear that $V_{out} = +2$ V. Further, applying Kirchhoff's voltage law to the input loop in Fig. 20.46, we have,

$$5\text{ V} - V_C - 2\text{ V} = 0$$

$$\therefore \quad V_C = 3\text{ V}$$

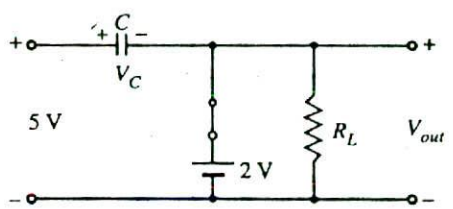


Fig. 20.46

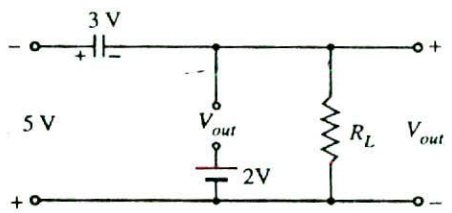


Fig. 20.47

Therefore, the capacitor will charge up to 3 V.

During the negative half-cycle of the input signal, the diode is reverse biased and will behave as an open [See Fig. 20.47]. Now battery of 2 V has no effect on V_{out}. Applying Kirchhoff's voltage law to the outside loop of Fig. 20.47, we have,

$$-5 - 3 - V_{out} = 0$$

or $$V_{out} = -8\text{ V}$$

The negative sign resulting from the fact that the polarity of 8 V is opposite to the polarity defined for V_{out}. The clamped output is shown in Fig. 20.48. Note that the output swing of 10 V matches with the input swing.

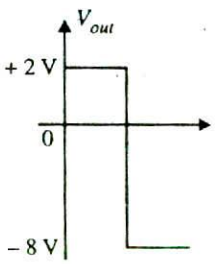


Fig. 20.48

Note. It is a biased clamper circuit. It allows a waveform to be shifted above or below (depending upon the polairty of 2 V battery) a *dc* reference other than 0 V.

Example 20.11. *Sketch the output waveform for the circuit shown in Fig. 20.49. It is given that discharging time constant (= CR_L) is much greater than the time period of input wave.*

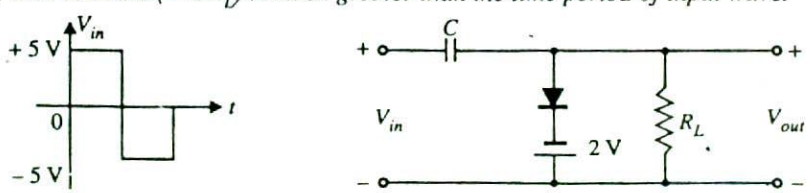


Fig. 20.49

Solution.

During the positive half-cycle of input signal, the diode is forward biased. Therefore, the diode behaves as a short [See Fig. 20.50]. It is easy to see that $V_{out} = -2$ V. Further, applying Kirchhoff's voltage law to the input loop [See Fig. 20.50], we have,

$$5\ V - V_C + 2\ V = 0$$

or $$V_C = 7\ V$$

Therefore, the capacitor will charge upto 7 V.

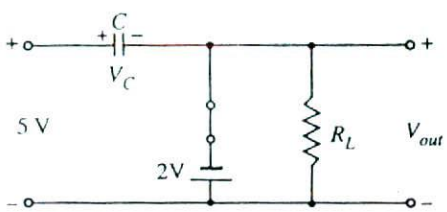


Fig. 20.50

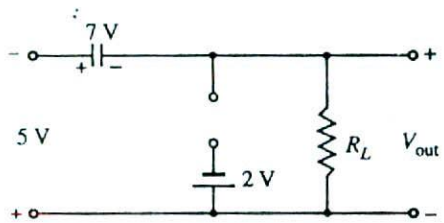


Fig. 20.51

During the negative half-cycle of the input signal, the diode is reverse biased and behaves as an open as shown in Fig. 20.51. Now battery of 2 V has no effect on V_{out}. Applying Kirchhoff's voltage law to the outside loop of Fig. 20.51, we have,

$$-5\ V - 7\ V - V_{out} = 0$$

or $$V_{out} = -12\ V$$

The negative sign resulting from the fact that the polarity of 12 V is opposite to the polarity defined for V_{out}. The clamped output is shown in Fig. 20.52. Note that output and input swings are the same.

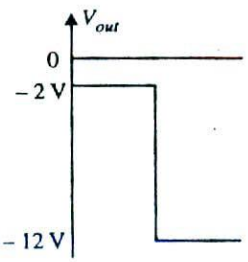


Fig. 20.52

Multiple-Choice Questions

1. A switch has .....
   (*i*) one state (*ii*) two states
   (*iii*) three states (*iv*) none of the above
2. A relay is ..... switch.
   (*i*) a mechanical (*ii*) an electronic
   (*iii*) an electromechanical
   (*iv*) none of the above
3. The switch that has the fastest speed of operation is ..... switch.
   (*i*) electronic
   (*ii*) mechanical
   (*iii*) electromechanical
   (*iv*) none of the above
4. The most inexpensive switch is ..... switch.
   (*i*) electronic
   (*ii*) mechanical
   (*iii*) electromechanical
   (*iv*) none of the above
5. The main disadvantage of a mechanical switch is that it .....
   (*i*) is operated mechanically
   (*ii*) is costly
   (*iii*) has high inertia
   (*iv*) none of the above
6. When a transistor is driven to saturation, ideally the output is .....
   (*i*) V_{CC} (*ii*) 0
   (*iii*) $V_{CC}/2$ (*iv*) $2V_{CC}$
7. The maximum speed of electronic switch can be ..... operations per second.
   (*i*) 10^4 (*ii*) 10
   (*iii*) 1000 (*iv*) 10^9
8. A relay is superior to a mechanical switch

because it .....
(*i*) is relatively inexpensive
(*ii*) does not require moving contacts
(*iii*) combines control with power amplification
(*iv*) none of the above

9. When a transistor is driven to cut off, ideally the output is .....
(*i*) V_{CC} (*ii*) 0
(*iii*) $V_{CC}/2$ (*iv*) $V_{CC}/3$

10. ..... multivibrator is a square wave oscillator.
(*i*) monostable (*ii*) astable
(*iii*) bistable (*iv*) none of the above

11. An astable multivibrator has .....
(*i*) one stable state (*ii*) two stable states
(*iii*) no stable state (*iv*) none of the above

12. If d.c. supply of 10 V is fed to a differentiating circuit, then output will be .....
(*i*) 20 V (*ii*) 10 V
(*iii*) 0 V (*iv*) none of the above

13. If the input to a differentiating circuit is a saw-tooth wave, then output will be ..... wave.
(*i*) square (*ii*) triangular
(*iii*) sine (*iv*) rectangular

14. A bistable multivibrator has .....
(*i*) two stable states
(*ii*) one stable state
(*iii*) no stable state
(*iv*) none of the above

15. If a square wave is fed to a differentiating circuit, the output will be .....
(*i*) sine wave
(*ii*) sharp narrow pulses
(*iii*) rectangular wave
(*iv*) triangular wave

16. An integrating circuit is a simple *RC* series circuit with output taken across .....
(*i*) both *R* and *C* (*ii*) *R*
(*iii*) *C* (*iv*) none of the above

17. For an integrating circuit to be effective, the *RC* product should be ..... the time period of the input wave.
(*i*) 5 times greater than
(*ii*) 5 times smaller than
(*iii*) equal to
(*iv*) atleast 10 times greater than

18. A differentiating circuit is a simple RC circuit with output taken across .....
(*i*) R (*ii*) C
(*iii*) both R and C (*iv*) none of the above

19. A monostable multivibrator has .....
(*i*) no stable state
(*ii*) one stable state
(*iii*) two stable states
(*iv*) none of the above

20. The multivibrator which generates square wave of its own is the ..... multivibrator.
(*i*) monostable (*ii*) bistable
(*iii*) astable (*iv*) none of the above

21. For a differentiating circuit to be effective, the RC product should be ..... the time period of the input wave.
(*i*) equal to
(*ii*) 5 times greater than
(*iii*) 5 times smaller than
(*iv*) atleast 10 times greater than

22. When a rectangular voltage waveform is applied to a capacitor, then the current waveform is .....
(*i*) rectangular (*ii*) sinusoidal
(*iii*) sawtooth (*iv*) square

23. The positive clipper is that which removes the ..... half-cycles of the input voltage.
(*i*) negative
(*ii*) positive
(*iii*) both positive and negative
(*iv*) none of the above

24. A clamping circuit adds ..... component to the signal.
(*i*) d.c.
(*ii*) a.c.
(*iii*) both d.c. and a.c.
(*iv*) none of the above

25. One would find a clamping circuit in .....
(*i*) receiving antenna
(*ii*) radio transmitter
(*iii*) radio receiver (*iv*) television receiver

26. When transistor is used as an amplifier, it is operated in the ..... region.
(*i*) off (*ii*) saturation
(*iii*) active (*iv*) none of the above

27. When the transistor (CE arrangement) is in the cut off region, the collector current is .....
(*i*) I_{CBO} (*ii*) I_{CEO}
(*iii*) $(\beta + 1) I_{CEO}$ (*iv*) $I_{C\,(sat)}$

28. A negative clipper removes the ..... half cycles of the input voltage.
(*i*) negative
(*ii*) positive
(*iii*) both positive and negative
(*iv*) none of the above

29. If the input to an integrating circuit is a succession of alternating positive and negative pulses of very short duration, the output will be ..... wave.
(*i*) rectangular (*ii*) triangular
(*iii*) sine (*iv*) square

30. In a multivibrator, we have ..... feedback.
(*i*) negative
(*ii*) 100 % positive
(*iii*) both positive and negative
(*iv*) none of the above

Answers to Multiple-Choice Questions

1. (*ii*)	**2.** (*iii*)	**3.** (*i*)	**4.** (*i*)	**5.** (*iii*)
6. (*ii*)	**7.** (*iv*)	**8.** (*iii*)	**9.** (*i*)	**10.** (*ii*)
11. (*iii*)	**12.** (*iii*)	**13.** (*iv*)	**14.** (*i*)	**15.** (*ii*)
16. (*iii*)	**17.** (*iv*)	**18.** (*i*)	**19.** (*ii*)	**20.** (*iii*)
21. (*iv*)	**22.** (*i*)	**23.** (*ii*)	**24.** (*i*)	**25.** (*iv*)
26. (*iii*)	**27.** (*ii*)	**28.** (*i*)	**29.** (*iv*)	**30.** (*ii*)

Chapter Review Topics

1. What is a switching circuit ?
2. Discuss the advantages of an electronic switch over a mechanical or electro-mechanical switch.
3. Explain the terms collector leakage current and saturation collector current.
4. Explain the switching action of a transistor with the help of output characteristics.
5. What is a multivibrator ? Explain the principle on which it works.
6. With a neat sketch, explain the working of (*i*) astable multivibrator (*ii*) monostable multivibrator (*iii*) bistable multivibrator.
7. What is the basic difference among the three types of multivibrators. ?
8. Show that the output from a differentiating circuit is derivative of the input. What assumptions are made in the derivation ?
9. Sketch the output waveforms from a differentiating circuit when input is (*i*) a square wave (*ii*) saw-tooth wave.
10. Show that the output from an integrating circuit is the integral of the input.
11. What is a clipper ? Describe (*i*) positive clipper (*ii*) biased clipper and (*iii*) combination clipper.
12. What do you understand by a clamping circuit ? With neat diagrams explain the action of a (*i*) positive clamper (*ii*) negative clamper.

Problems

1. The negative shunt clipper shown in Fig. 20.53 has peak input voltage of +15 V. What is the output peak voltage ? [12.54 V]

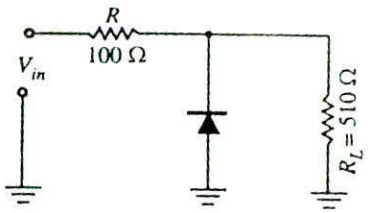


Fig. 20.53

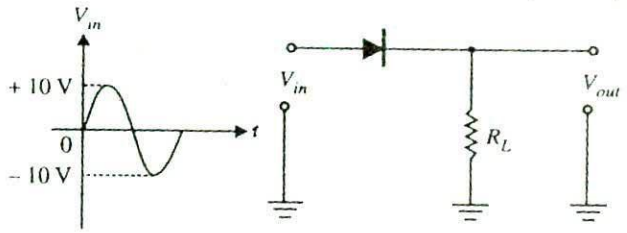
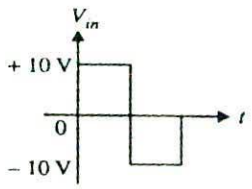


Fig. 20.54

2. In the negative series clipper shown in Fig. 20.54, what is the peak output voltage ? [9.3 V]
3. In the circuit shown in Fig. 20.55, what are the minimum and peak values of the clamped output ? [0 V ; –20 V]



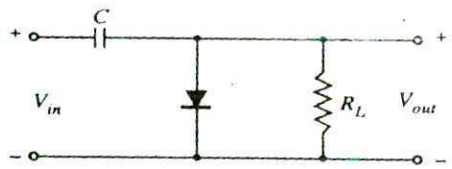
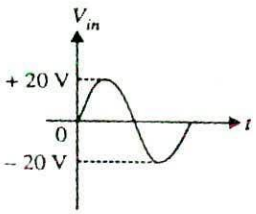


Fig. 20.55



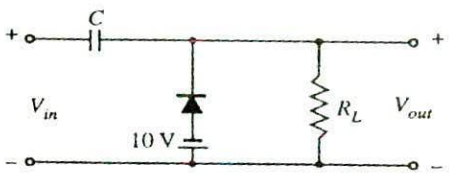


Fig. 20.56

4. Sketch the wave shape of clamped output in Fig. 20.56.

Discussion Questions

1. What is the effect of *RC* product on the output waveform in a differentiating circuit ?
2. A differentiating circuit is essentially an *RC* circuit. Why the output from *RC* coupling is not a differentiated wave ?
3. What is the difference between a switching transistor and an ordinary transistor ?
4. What effect does a clamper have on the average value of a given input wave ?
5. What effect does a clamper have on the r.m.s. voltage of a sine-wave input ?
6. What determines the d.c. reference voltage of a clamper ?
7. Discuss the differences between shunt and series clippers.

21

Field Effect Transistors

Introduction

In the previous chapters, we have discussed the circuit applications of an ordinary transistor. In this type of transistor, both holes and electrons play part in the conduction process. For this reason, it is sometimes called a bipolar transistor. The ordinary or bipolar transistor has two principal disadvantages. First, it has a low input impedance because of forward biased emitter junction. Secondly, it has considerable noise level. Although low input impedance problem may be improved by careful design and use of more than one transistor, yet it is difficult to achieve input impedance more than a few megaohms. The field effect transistor (*FET*) has, by virtue of its construction and biasing, large input impedance which may be more than 100 megaohms. The *FET* is generally much less noisy than the ordinary or bipolar transistor. The rapidly expanding *FET* market has led many semiconductor marketing managers to believe that this device will soon become the most important electronic device, primarily because of its integrated-circuit applications. In this chapter, we shall focus our attention on the construction, working and circuit applications of field effect transistors.

21.1 Types of Field Effect Transistors

A bipolar junction transistor (*BJT*) is a current controlled device *i.e.*, output characteristics of the device are controlled by base current and not by base voltage. However, in a field effect transistor (*FET*), the output characteristics are controlled by input voltage (*i.e.*, electric field) and not by input current. This is probably the biggest difference between *BJT* and *FET*. There are two basic types of field effect transistors:

(*i*) Junction field effect transistor (*JFET*)

(*ii*) Metal oxide semiconductor field effect transistor (*MOSFET*)

To begin with, we shall study about *JFET* and then improved form of *JFET*, namely; *MOSFET*.

21.2 Junction Field Effect Transistor (JFET)

A **junction field effect transistor** *is a three terminal semiconductor device in which current conduction is by one type of carrier i.e., electrons or holes.*

The *JFET* was developed about the same time as the transistor but it came into general use only in the late 1960s. In a *JFET*, the current conduction is either by electrons or holes and is controlled by means of an electric field between the gate electrode and the conducting channel of the device. The *JFET* has high input impedance and low noise level.

Constructional details. A *JFET* consists of a *p*-type or *n*-type silicon bar containing two *pn* junctions at the sides as shown in Fig. 21.1. The bar forms the conducting channel for the charge

carriers. If the bar is of *n*-type, it is called *n-channel JFET* as shown in Fig. 21.1 (*i*) and if the bar is of *p*-type, it is called a *p-channel JFET* as shown in Fig. 21.1 (*ii*). The two *pn* junctions forming diodes are connected internally and a common terminal called *gate* is taken out. Other terminals are *source* and *drain* taken out from the bar as shown. Thus a *JFET* has essentially three terminals *viz.*, *gate* (*G*), *source* (*S*) and *drain* (*D*).

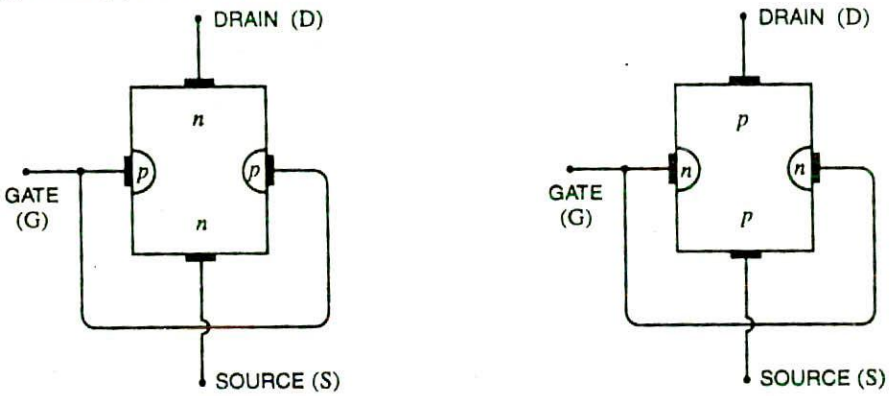


Fig. 21.1

JFET polarities. Fig. 21.2 (*i*) shows *n*-channel *JFET* polarities whereas Fig. 21.2 (*ii*) shows the *p*-channel *JFET* polarities. Note that in each case, the voltage between the gate and source is such that the gate is reverse biased. This is the normal way of *JFET* connection. The drain and source terminals are *interchangeable *i.e.*, either end can be used as source and the other end as drain.

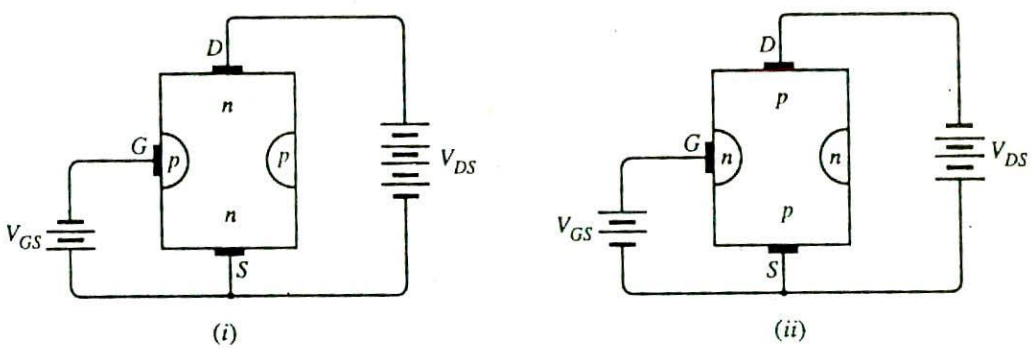


Fig. 21.2

21.3 Working Principle of JFET

Fig. 21.3 shows the circuit of *n*-channel *JFET* with normal polarities. The circuit action is as follows:

(*i*) When a voltage V_{DS} is applied between drain and source terminals and voltage on the gate is zero [See Fig. 21.3 (*i*)], the two *pn* junctions at the sides of the bar establish depletion layers. The electrons will flow from source to drain through a channel between the depletion layers. The size of these layers determines the width of the channel and hence the current conduction through the bar.

* This is generally valid for low frequency applications. However, it is not true at high frequencies.

(*ii*) When a reverse voltage V_{GS} is applied between the gate and source [See Fig. 21.3 (*ii*)], the width of the depletion layers is increased. This reduces the width of conducting channel, thereby increasing the resistance of *n*-type bar. Consequently, the current from source to drain is decreased. On the other hand, if the reverse voltage on the gate is decreased, the width of the depletion layers also decreases. This increases the width of the conducting channel and hence source to drain current.

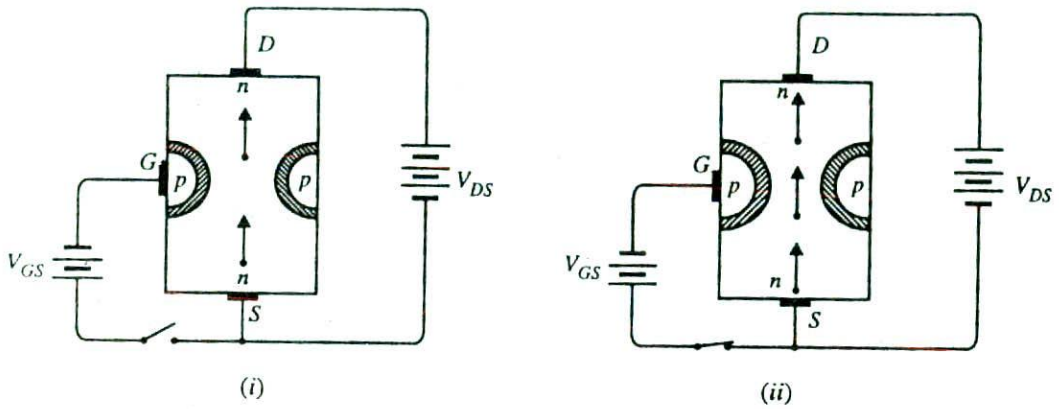


Fig. 21.3

It is clear from the above discussion that current from source to drain can be controlled by the application of potential (*i.e.* electric field) on the gate. For this reason, the device is called *field effect transistor*. It may be noted that a *p*-channel *JFET* operates in the same manner as an *n* -channel *JFET* except that channel current carriers will be the holes instead of electrons and the polarities of V_{GS} and V_{DS} are reversed.

21.4 Schematic Symbol of JFET

Fig. 21.4 shows the schematic symbol of *JFET*. The vertical line in the symbol may be thought as

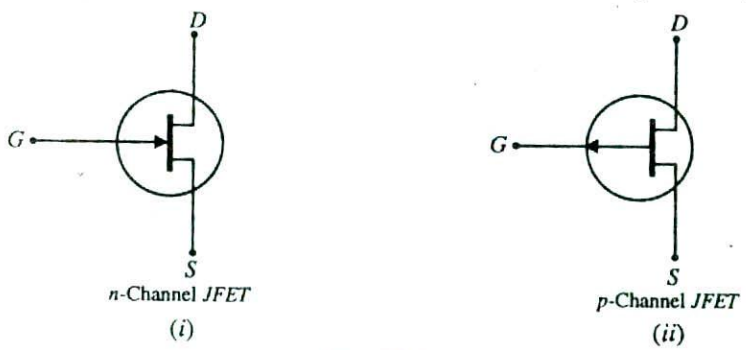


Fig. 21.4

channel and source (S) and drain (D) connected to this line. If the channel is *n*-type, the arrow on the gate points towards the channel as shown in Fig. 21.4 (*i*). However, for *p*-type channel, the arrow on the gate points from channel to gate [See Fig. 21.4 (*ii*)].

21.5 Importance of JFET

A *JFET* acts like a voltage controlled device *i.e.* input voltage (V_{GS}) controls the output current. This

is different from ordinary transistor (or bipolar transistor) where input current controls the output current. Thus *JFET* is a semiconductor device acting *like a vacuum tube. The need for *JFET* arose because as modern electronic equipment became increasingly transistorised, it became apparent that there were many functions in which bipolar transistors were unable to replace vacuum tubes. Owing to their extremely high input impedance, *JFET* devices are more like vacuum tubes than are the bipolar transistors and hence are able to take over many vacuum-tube functions. Thus, because of *JFET*, electronic equipment is closer today to being completely solid state.

The *JFET* devices have not only taken over the functions of vacuum tubes but they now also threaten to depose the bipolar transistors as the most widely used semiconductor devices. As an amplifier, the *JFET* has higher input impedance than that of a conventional transistor, generates less noise and has greater resistance to nuclear radiations.

21.6 Difference Between JFET and Bipolar Transistor

The *JFET* differs from an ordinary or bipolar transistor in the following ways :

(*i*) In a *JFET*, there is only one type of carrier, holes in *p*-type channel and electrons in *n*-type channel. For this reason, it is also called a *unipolar transistor*. However, in an ordinary transistor, both holes and electrons play part in conduction. Therefore, an ordinary transistor is sometimes called a *bipolar transistor*.

(*ii*) As the input circuit (*i.e.*, gate to source) of a *JFET* is reverse biased, therefore, the device has high input impedance. However, the input circuit of an ordinary transistor is forward biased and hence has low input impedance.

(*iii*) As the gate is reverse biased, therefore, it carries very small current. Obviously, *JFET* is just like a vacuum tube where control grid (corresponding to gate in *JFET*) carries extremely small current and input voltage controls the output current. For this reason, *JFET* is essentially a *voltage-driven device*. However, ordinary transistor is a current operated device *i.e.*, input current controls the output current.

Fig. 21.5

(*iv*) A bipolar transistor uses a current into its base to control a large current between collector and emitter whereas a *JFET* uses voltage on the 'gate' (= base) terminal to control the current between drain (= collector) and source (= emitter). Thus a bipolar transistor gain is characterised by current gain whereas the *JFET* gain is characterised as a transconductance *i.e.*, the ratio of change in output current (drain current) to the input (gate) voltage.

(*v*) In *JFET*, there are no junctions as in an ordinary transistor. The conduction is through an *n*- type or *p*-type semi-conductor material. For this reason, noise level in *JFET* is very small.

---

* The gate, source and drain of a *JFET* correspond to grid, cathode and anode of a vacuum tube.

21.7 JFET as an Amplifier

Fig. 21.6 shows *JFET* amplifier circuit. The weak signal is applied between gate and source and amplified output is obtained in the drain-source circuit. For the proper operation of *JFET*, the gate must be negative w.r.t. source *i.e.*, input circuit should always be reverse biased. This is achieved either by inserting a battery V_{GG} in the gate circuit or by a circuit known as biasing circuit. In the present case, we are providing biasing by the battery V_{GG}.

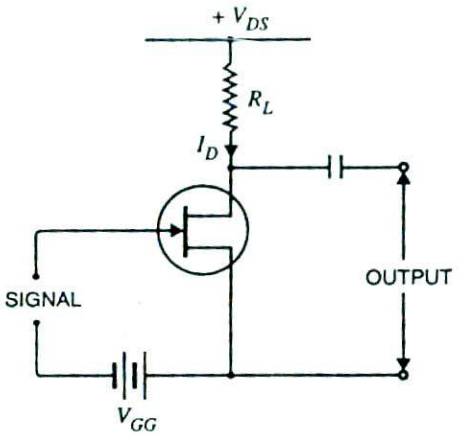


Fig. 21.6

A small change in the reverse bias on the gate produces a large change in drain current. This fact makes *JFET* capable of raising the strength of a weak signal. During the positive half of signal, the reverse bias on the gate decreases. This increases the channel width and hence the drain current. During the negative half-cycle of the signal, the reverse voltage on the gate increases. Consequently, the drain current decreases. The result is that a small change in voltage at the gate produces a large change in drain current. These large variations in drain current produce large output across the load R_L. In this way, *JFET* acts as an amplifier.

21.8 Output Characteristics of JFET

The curve between drain current (I_D) and drain-source voltage (V_{DS}) of a *JFET* at constant gate-source voltage (V_{GS}) is known as *output characteristics of JFET*. Fig. 21.7 shows the circuit for determining the output characteristics of *JFET*. Keeping V_{GS} fixed at some value, say 1V, the drian-source voltage is changed in steps. Corresponding to each value of V_{DS}, the drain current I_D is noted. A plot of these values gives the output characteristic of *JFET* at V_{GS} = 1V. Repeating similar procedure, output characteristics at other gate-source voltages can be drawn. Fig. 21.8 shows a family of output characteristics.

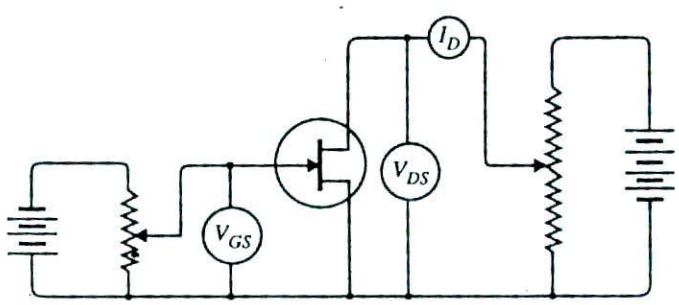


Fig. 21.7

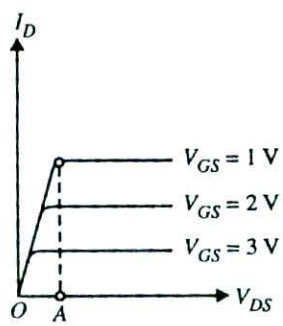


Fig. 21.8

The following points may be noted from the characteristics :

(*i*) At first, the drain current I_D rises rapidly with drain-source voltage V_{DS} but then becomes constant. The drain-source voltage above which drain current becomes constant is known as *pinch off voltage*. Thus in Fig. 21.8, *OA* is the *pinch off voltage*.

(*ii*) After pinch off voltage, the channel width becomes so narrow that depletion layers almost

touch each other. The drain current passes through the small passage between these layers. Therefore, increase in drain current is very small with V_{DS} above pinch off voltage. Consequently, drain current remains constant.

(*iii*) The characteristics resemble that of a pentode valve.

21.9 Important Terms

In the analysis of a *JFET* circuit, the following important terms are often used :

1. Shorted-gate drain current (I_{DSS})
2. Pinch off voltage (V_P)
3. Gate-source cut off voltage [$V_{GS\,(off)}$]

1. Shorted-gate drain current (I_{DSS}). *It is the drain current with source short-circuited to gate (i.e. $V_{GS} = 0$) and drain voltage (V_{DS}) equal to pinch off voltage.* It is sometimes called *zero-bias current.*

Fig 21.9 shows the *JFET* circuit with $V_{GS} = 0$ *i.e.*, source shorted-circuited to gate. This is normally called shorted-gate condition. Fig. 21.10 shows the graph between I_D and V_{DS} for the shorted gate condition. The drain current rises rapidly at first and then levels off at pinch off voltage V_P. The drain current has now reached the maximum value I_{DSS}. When V_{DS} is increased beyond V_P, the depletion layers expand at the top of the channel. The channel now acts as a current limiter and *holds drain current constant at I_{DSS}.

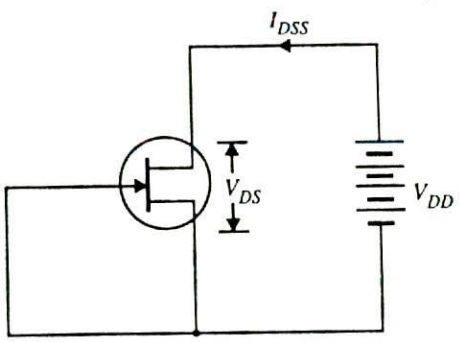


Fig. 21.9

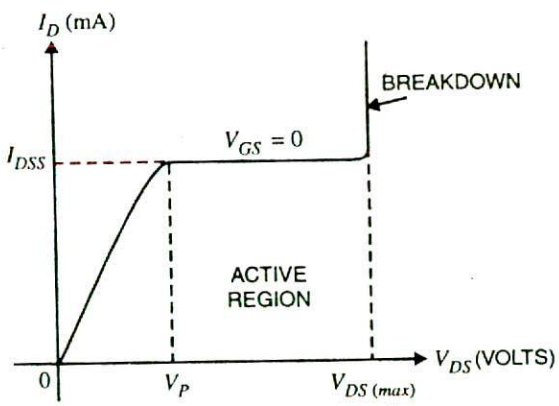


Fig. 21.10

The following points may be noted carefully :

(*i*) Since I_{DSS} is measured under shorted gate conditions, it is the maximum drain current that you can get with normal operation of *JFET*.

(*ii*) There is a maximum drain voltage [$V_{DS\,(max)}$] that can be applied to a *JFET*. If the drain voltage exceeds $V_{DS\,(max)}$, *JFET* would breakdown as shown in Fig. 21.10.

(*iii*) The region between V_P and $V_{DS\,(max)}$ (breakdown voltage) is called *constant-current region* or active region. As long as V_{DS} is kept within this range, I_D will remain constant for a constant value of V_{GS}. In other words, in the active region, *JFET* behaves as a constant–current device. For proper working of *JFET*, it must be operated in the active region.

---

* When drain voltage equals V_P, the channel becomes narrow and the depletion layers almost touch each other. The channel now acts as a current limiter and holds drain current at a constant value of I_{DSS}.

2. Pinch off Voltage (V_P). *It is the minimum drain-source voltage at which the drain current essentially becomes constant.*

Figure 21.11 shows the drain curves of a *JFET*. Note that pinch off voltage is V_P. The highest curve is for $V_{GS} = 0$, the shorted-gate condition. For values of V_{DS} greater than V_P, the drain current is almost constant. It is because when V_{DS} equals V_P, the channel is effectively closed and does not allow further increase in drain current. It may be noted that for proper function of *JFET*, it is always operated for $V_{DS} > V_P$. However, V_{DS} should not exceed $V_{DS\,(max)}$ otherwise *JFET* may breakdown.

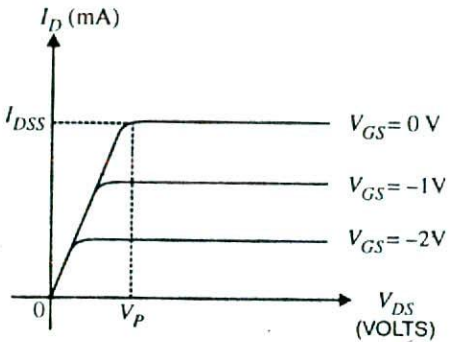


Fig 21.11

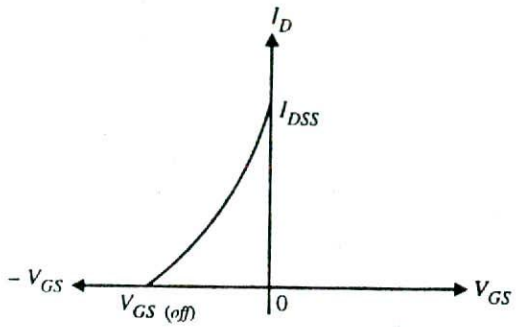


Fig 21.12

3. Gate-source cut off voltage $V_{GS\,(off)}$. *It is the gate-source voltage where the channel is completely cut off and the drain current becomes zero.*

The idea of gate-source cut off voltage can be easily understood if we refer to the transfer characteristic of a *JFET* shown in Fig. 21.12. As the reverse gate-source voltage is increased, the cross-sectional area of the channel decreases This in turn decreases the drain current. At some reverse gate-source voltage, the depletion layers extend completely across the channel. In this condition, the channel is cut off and the drain current reduces to zero. The gate voltage at which the channel is cut off (*i.e.* channel becomes non-conducting) is called gate-source cut off voltage $V_{GS\,(off)}$.

Notes. (*i*) It is interesting to note that $V_{GS\,(off)}$ will always have the same magnitude value as V_P. For example if $V_P = 6$ V, then $V_{GS\,(off)} = -6$ V. Since these two values are always equal and opposite, only one is listed on the specification sheet for a given *JFET*.

(*ii*) There is a distinct difference between V_P and $V_{GS\,(off)}$. Note that V_P is the value of V_{DS} that causes the *JEFT* to become a constant current device. It is measured at $V_{GS} = 0$ V and will have a constant drain current = I_{DSS}. However, $V_{GS\,(off)}$ is the value of V_{GS} that causes I_D to drop to nearly zero.

21.10 Expression for Drain Current (I_D)

The relation between I_{DSS} and V_P is shown in Fig. 21.13. We note that gate-source cut off voltage [*i.e.* $V_{GS\,(off)}$] on the transfer characteristic is equal to pinch off voltage V_P on the drain characteristic *i.e.*

$$V_P = |V_{GS\,(off)}|$$

For example, if a *JFET* has $V_{GS} = -4$V, then $V_P = 4$V.

The transfer characteristic of *JFET* shown in Fig. 21.13 is part of a parabola. A rather complex mathematical analysis yields the following expression for drain current :

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$

where I_D = drain current at given V_{GS}

I_{DSS} = shorted – gate drain current
V_{GS} = gate–source voltage
$V_{GS\,(off)}$ = gate–source cut off voltage

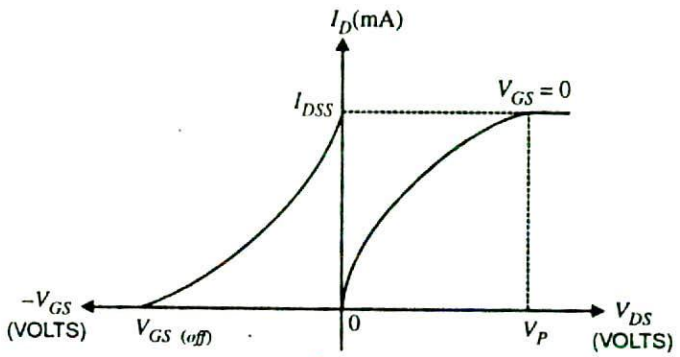


Fig. 21.13

Example 21.1. *Fig. 21.14 shows the transfer characteristic of a JFET. Write the equation for drain current.*

Solution. Referring to the transfer characteristic in Fig. 21.14, we have,

$$I_{DSS} = 12 \text{ mA}$$
$$V_{GS\,(off)} = -5 \text{ V}$$
$$\therefore \quad I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$
$$\text{or} \quad I_D = 12\left[1 + \frac{V_{GS}}{5}\right]^2 \text{ mA}$$

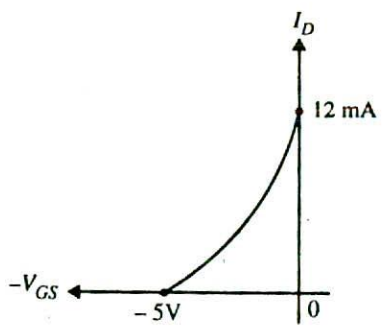


Fig. 21.14

Example 21.2. *A JFET has the following parameters: $I_{DSS} = 32$ mA ; $V_{GS\,(off)} = -8V$; $V_{GS} = -4.5$ V. Find the value of drain current.*

Solution.
$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$
$$= 32\left[1 - \frac{(-4.5)}{-8}\right]^2 \text{ mA}$$
$$= \mathbf{6.12\ mA}$$

Example 21.3. *A JFET has a drain current of 5 mA. If $I_{DSS} = 10$ mA and $V_{GS\,(off)} = -6$ V, find the value of (i) V_{GS} and (ii) V_P.*

Solution.
$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS\,(off)}}\right]^2$$
or
$$5 = 10\left[1 + \frac{V_{GS}}{6}\right]^2$$
or
$$1 + \frac{V_{GS}}{6} = \sqrt{5/10} = 0.707$$

(*i*) $\therefore$ $V_{GS} = -1.76$ V

(*ii*) and $V_P = -V_{GS\,(off)} = 6$ V

21.11 Advantages of JFET

A *JFET* is a voltage controlled, constant current device (similar to a vacuum pentode) in which variations in input voltage control the output current. It combines the many advantages of both bipolar transistor and vacuum pentode. Some of the advantages of a *JFET* are :

(*i*) It has a very high input impedance (of the order of 100 MΩ). This permits high degree of isolation between the input and output circuits.

(*ii*) The operation of a *JFET* depends upon the bulk material current carriers that do not cross junctions. Therefore, the inherent noise of tubes (due to high-temperature operation) and those of transistors (due to junction transitions) are not present in a *JFET*.

(*iii*) A *JFET* has a negative temperature co-efficient of resistance. This avoids the risk of thermal runaway.

(*iv*) A *JFET* has a very high power gain. This eliminates the necessity of using driver stages.

(*v*) A *JFET* has a smaller size, longer life and high efficiency.

21.12 Parameters of JFET

Like vacuum tubes, a *JFET* has certain parameters which determine its performance in a circuit. The main parameters of a *JFET* are (*i*) a.c. drain resistance (*ii*) transconductance (*iii*) amplification factor.

(*i*) **a.c. drain resistance (r_d).** Corresponding to the a.c. plate resistance, we have a.c. drain resistance in a *JFET*. It may be defined as follows :

It is the ratio of change in drain-source voltage (ΔV_{DS}) to the change in drain current (ΔI_D) at constant gate-source voltage i.e.

$$\text{a.c. drain resistance, } r_d = \frac{\Delta V_{DS}}{\Delta I_D} \text{ at constant } V_{GS}$$

For instance, if a change in drain voltage of 2 V produces a change in drain current of 0.02 mA, then,

$$\text{a.c. drain resistance, } r_d = \frac{2 \text{ V}}{0.02 \text{ mA}} = 100 \text{ k}\Omega$$

Referring to the output characteristics of a *JFET* in Fig. 21.8, it is clear that above the pinch off voltage, the change in I_D is small for a change in V_{DS} because the curve is almost flat. Therefore, drain resistance of a *JFET* has a large value, ranging from 10 kΩ to 1 MΩ.

(*ii*) **Transconductance (g_{fs}).** The control that the gate voltage has over the drain current is measured by transconductance g_{fs} and is similar to the transconductance g_m of the tube. It may be defined as follows :

It is the ratio of change in drain current (ΔI_D) to the change in gate-source voltage (ΔV_{GS}) at constant drain-source voltage i.e.

$$\text{Transconductance, } g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} \text{ at constant } V_{DS}$$

The transconductance of a *JFET* is usually expressed either in mA/volt or micromho. As an example, if a change in gate voltage of 0.1 V causes a change in drain current of 0.3 mA, then,

$$\text{Transconductance, } g_{fs} = \frac{0.3 \text{ mA}}{0.1 \text{ V}} = 3 \text{ mA/V} = 3 \times 10^{-3} \text{ A/V or mho}$$

$$= 3 \times 10^{-3} \times 10^{6} \text{ μ mho} = 3000 \text{ μ mho}$$

(iii) **Amplification factor (μ).** *It is the ratio of change in drain-source voltage (ΔV_{DS}) to the change in gate-source voltage (ΔV_{GS}) at constant drain current i.e.*

$$\text{Amplification factor, } \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \text{ at constant } I_D$$

Amplification factor of a *JFET* indicates how much more control the gate voltage has over drain current than has the drain voltage. For instance, if the amplification factor of a *JFET* is 50, it means that gate voltage is 50 times as effective as the drain voltage in controlling the drain current.

21.13 Relation Among JFET Parameters

The relationship among *JFET* parameters can be established as under :

$$\text{We know} \quad \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

Multiplying the numerator and denominator on R.H.S. by ΔI_D, we get,

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \times \frac{\Delta I_D}{\Delta I_D} = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\therefore \quad \mu = r_d \times g_{fs}$$

i.e. amplification factor = a.c. drain resistance × transconductance

Example 21.4. *When a reverse gate voltage of 15 V is applied to a JFET, the gate current is 10^{-3} μA. Find the resistance between gate and source.*

Solution. $V_{GS} = 15 \text{ V} \; ; \; I_G = 10^{-3} \text{ μA} = 10^{-9} \text{ A}$

$$\therefore \quad \text{Gate to source resistance} = \frac{V_{GS}}{I_G} = \frac{15 \text{ V}}{10^{-9} \text{ A}} = 15 \times 10^9 \, \Omega = \mathbf{15{,}000 \text{ MΩ}}$$

This example shows the major difference between a *JFET* and a bipolar transistor. Whereas the input impedance of a *JFET* is several hundred MΩ, the input impedance of a bipolar transistor is only hundreds or thousands of ohms. The large input impedance of a *JFET* permits high degree of isolation between the input and output.

Example 21.5. *When V_{GS} of a JFET changes from –3.1 V to –3 V, the drain current changes from 1 mA to 1.3 mA. What is the value of transconductance ?*

Solution. $\Delta V_{GS} = 3.1 - 3 = 0.1 \text{ V}$ ... magnitude

$$\Delta I_D = 1.3 - 1 = 0.3 \text{ mA}$$

$$\therefore \quad \text{Transconductance, } g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{0.3 \text{ mA}}{0.1 \text{ V}} = 3 \text{ mA/V} = \mathbf{3000 \; \mu \text{ mho}}$$

Example 21.6. *The following readings were obtained experimentally from a JFET :*

V_{GS}	*0 V*	*0 V*	*– 0.2 V*
V_{DS}	*7 V*	*15 V*	*15 V*
I_D	*10 mA*	*10.25 mA*	*9.65 mA*

Determine (i) a. c. drain resistance (ii) transconductance and (iii) amplification factor.

Solution. *(i)* With V_{GS} constant at 0V, the increase in V_{DS} from 7 V to 15 V increases the drain current from 10 mA to 10.25 mA *i.e.*

Change in drain-source voltage, $\Delta V_{DS} = 15 - 7 = 8 \text{ V}$

Change in drain current, $\Delta I_D = 10.25 - 10 = 0.25 \text{ mA}$

$$\therefore \quad \text{a.c. drain resistance, } r_d = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{8\text{ V}}{0.25\text{ mA}} = \mathbf{32\ k\Omega}$$

(*ii*) With V_{DS} constant at 15 V, drain current changes from 10.25 mA to 9.65 mA as V_{GS} is changed from 0 V to – 0.2 V.

$$\Delta V_{GS} = 0.2 - 0 = 0.2\text{ V}$$
$$\Delta I_D = 10.25 - 9.65 = 0.6\text{ mA}$$
$$\therefore \quad \text{Transconductance, } g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{0.6\text{ mA}}{0.2\text{ V}} = 3\text{ mA/V} = \mathbf{3000\ \mu\ mho}$$
$$(iii) \quad \text{Amplification factor, } \mu = r_d \times g_{fs} = (32 \times 10^3) \times (3000 \times 10^{-6}) = \mathbf{96}$$

21.14 JFET Biasing

For the proper operation of *n*-channel *JFET*, gate must be negative *w.r.t.* source. This can be achieved either by inserting a battery in the gate circuit or by a circuit known as biasing circuit. The latter method is preferred because batteries are costly and require frequent replacement.

1. Bias battery. Fig. 21.15 shows the biasing of a *n*-channel *JFET* by a bias battery V_{GG}. This battery ensures that gate is always negative *w.r.t.* source during all parts of the signal.

2. Biasing circuit. The biasing circuit uses supply voltage V_{DD} to provide the necessary bias. Two most commonly used methods are (*i*) self-bias (*ii*) potential divider method.

(*i*) **Self-bias.** Fig. 21.16 shows the self-bias method. The resistor R_S is the bias resistor. The d.c. component of drain current flowing through R_S produces the desired bias voltage. The capacitor C_S bypasses the a.c. component of the drain current.

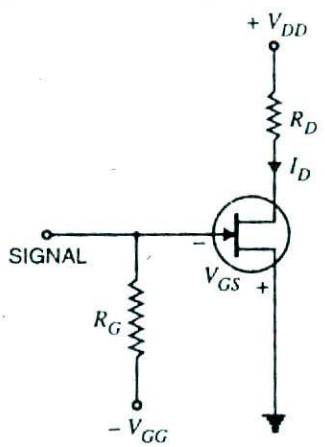


Fig. 21.15

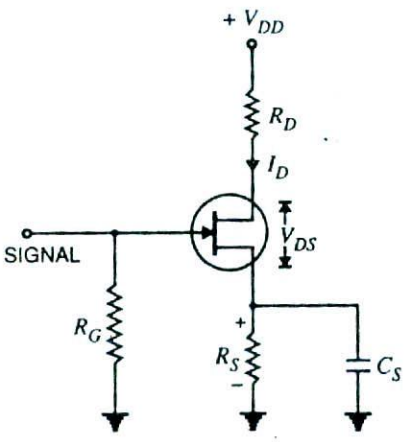


Fig. 21.16

Voltage across R_S, $V_S = I_D R_S$

Since gate current is negligibly small, the gate terminal is at d.c. ground *i.e.*, $V_G = 0$

$$\therefore \quad V_{GS} = V_G - V_S = 0 - I_D R_S$$
$$\text{or} \quad V_{GS} = -I_D R_S$$

Thus bias voltage V_{GS} keeps gate negative *w.r.t.* source.

Operating point. The operating point (*i.e.*, zero signal I_D and V_{DS}) can be easily determined. Since the parameters of the *JFET* are usually known, zero signal I_D can be calculated from the following relation :

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Also $V_{DS} = V_{DD} - I_D (R_D + R_S)$

Thus d.c. conditions of *JFET* amplifier are fully specified.

(*ii*) **Potential divider method.** Fig. 21.17 shows potential divider method of biasing a *JFET*. This circuit is identical to that used for a transistor. The resistors R_1 and R_2 form a voltage divider across drain supply V_{DD}. The voltage V_2 across R_2 provides the necessary bias.

$$V_2 = \frac{V_{DD}}{R_1 + R_2} \times R_2$$

Now $V_2 = V_{GS} + I_D R_S$

or $V_{GS} = V_2 - I_D R_S$

The circuit is so designed that $I_D R_S$ is larger than V_2 so that V_{GS} is negative. This provides correct bias voltage. We can find the operating point as under:

$$I_D = \frac{V_2 - V_{GS}}{R_S}$$

and $V_{DS} = V_{DD} - I_D (R_D + R_S)$

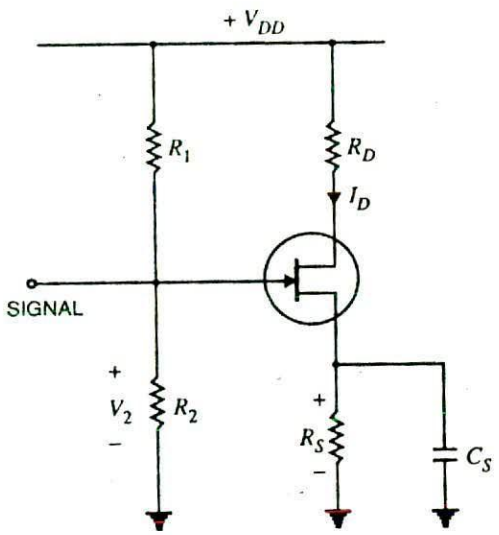
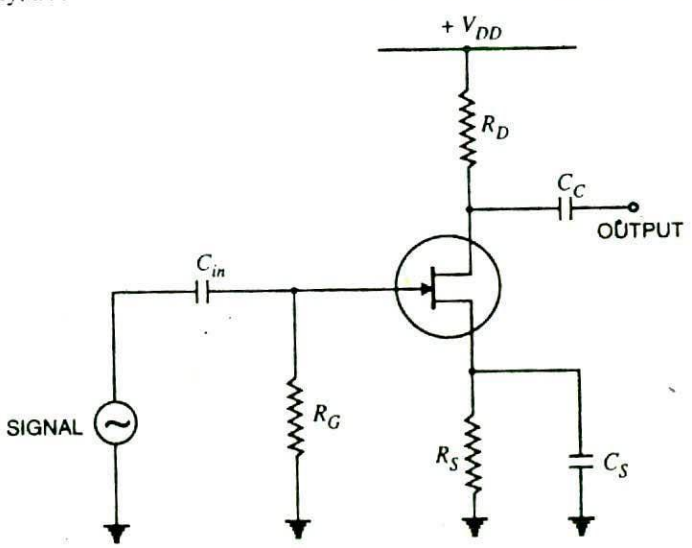


Fig. 21.17

21.15 JFET Connections

There are three leads in a *JFET viz.*, source, gate and drain terminals. However, when *JFET* is to be connected in a circuit, we require four terminals ; two for the input and two for the output. This difficulty is overcome by making one terminal of the *JFET* common to both input and output terminals. Accordingly, a *JFET* can be connected in a circuit in the following three ways :



COMMON SOURCE CONNECTION

Fig. 21.18

(*i*) Common source connection (*ii*) Common gate connection

(*iii*) Common drain connection

The common source connection is the most widely used arrangement. It is because this connection provides high input impedance, good voltage gain and a moderate output impedance. However, the circuit produces a phase reversal *i.e*,. output signal is 180° out of phase with the input signal. Fig. 21.18 shows a common source *n*-channel *JFET* amplifier. Note that source terminal is common to both input and output.

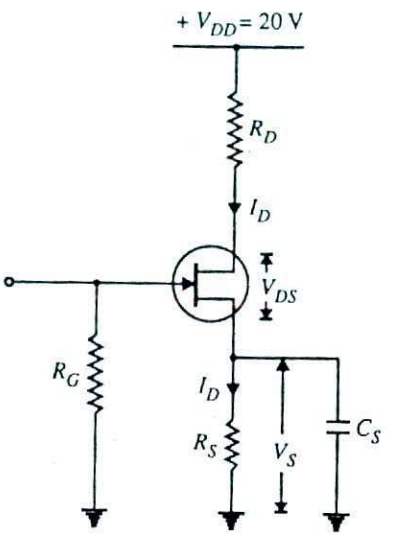


Fig. 21.19

Note. A common source *JFET* amplifier is the *JFET* equivalent of common emitter amplifier. Both amplifiers have a 180° phase shift from input to output. Although the two amplifiers serve the same basic purpose, the means by which they operate are quite different.

Example 21.7. *In a self-bias n-channel JFET, the operating point is to be set at I_D = 1.5 mA and V_{DS} = 10 V. The JFET parameters are I_{DSS} = 5 mA and V_P = − 2 V. Find the values of R_S and R_D. Given that V_{DD} = 20 V.*

Solution. Fig. 21.19 shows the circuit arrangement.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

or $$1.5 = 5\left(1 + \frac{V_{GS}}{2}\right)^2$$

or $$1 + \frac{V_{GS}}{2} = \sqrt{1.5/5} = 0.55$$

or $$V_{GS} = -0.9\,\text{V}$$

Now $$V_{GS} = V_G - V_S$$

or $$V_S = V_G - V_{GS}$$

$$= 0 - (-0.9) = 0.9\,\text{V}$$

$$\therefore \quad R_S = \frac{V_S}{I_D} = \frac{0.9\,\text{V}}{1.5\,\text{mA}} = \mathbf{0.6\,k\Omega}$$

Applying Kirchhoff's voltage law to the drain circuit, we have,

$$V_{DD} = I_D R_D + V_{DS} + I_D R_S$$

or $$20 = 1.5\,\text{mA} \times R_D + 10 + 0.9$$

$$\therefore \quad R_D = \frac{(20 - 10 - 0.9)\,\text{V}}{1.5\,\text{mA}} = \mathbf{6\,k\Omega}$$

Example 21.8. *In an n-channel JFET biased by potential divider method, it is desired to set the operating point at I_D = 2.5 mA and V_{DS} = 8V. If V_{DD} = 30 V, R_1 = 1 MΩ and R_2 = 500 kΩ, find the value of R_S. The parameters of JFET are I_{DSS} = 10 mA and V_P = − 5 V.*

Solution. Fig. 21.20 shows the conditions of the problem.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\text{or} \quad 2.5 = 10\left(1+\frac{V_{GS}}{5}\right)^2$$

$$\text{or} \quad 1+\frac{V_{GS}}{5} = \sqrt{2.5/10} = 0.5$$

$$\text{or} \quad V_{GS} = -2.5\ \text{V}$$

$$\text{Now} \quad V_2 = \frac{V_{DD}}{R_1+R_2}\times R_2$$

$$= \frac{30}{1000+500}\times 500$$

$$= 10\ \text{V}$$

$$V_2 = V_{GS} + I_D R_S$$

$$\text{or} \quad 10\ \text{V} = -2.5\ \text{V} + 2.5\ \text{mA}\times R_S$$

$$\therefore \quad R_S = \frac{10\ \text{V}+2.5\ \text{V}}{2.5\ \text{mA}} = \frac{12.5\ \text{V}}{2.5\ \text{mA}}$$

$$= \mathbf{5\ k\Omega}$$

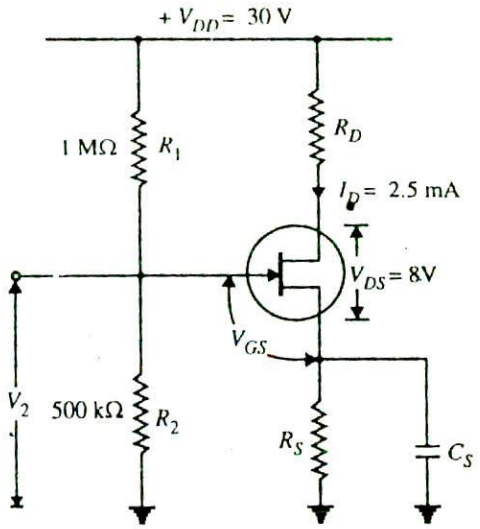


Fig. 21.20

21.16 Voltage Gain of JFET Amplifier

Fig. 21.21 shows a typical circuit of a *JFET* amplifier. The *JFET* is self-biased by using the biasing network $R_S - C_S$. The d.c. component of the drain current flowing through the source-biasing resistance R_S produces the desired bias voltage. The capacitor C_S bypasses the a.c. component of drain current. It may be noted that biasing circuit is similar to the cathode bias for a vacuum tube. The value of R_S can be determined from the following relation :

$$R_S = \frac{V_{GS}}{I_D}$$

where V_{GS} = voltage drop across R_S and I_D = current through R_S

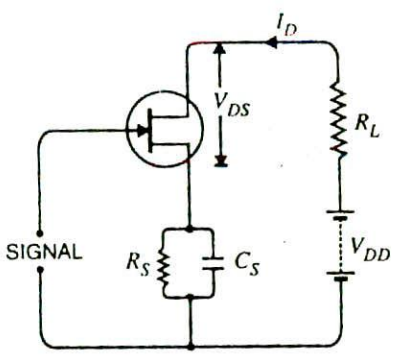


Fig. 21.21

Like a vacuum tube, a *JFET* is a voltage driven device. Therefore, the voltage gain of a *JFET* amplifier can be determined in the same manner as for a vacuum tube.

∴ Voltage gain of *JFET* amplifier is

$$A_v = \frac{\mu R_L}{r_d + R_L}$$

$$\text{Since} \quad \mu = r_d \times g_{fs} \qquad \therefore \quad A_v = \frac{r_d\, g_{fs}\, R_L}{r_d + R_L}$$

If $r_d >> R_L$, then the latter can be neglected as compared to the former.

$$\therefore \quad \text{Voltage gain, } A_v = \frac{r_d\, g_{fs}\, R_L}{r_d} \quad \text{or} \quad A_v = g_{fs} \times R_L$$

Example 21.9. *The transconductance of a JFET used in a voltage-amplifier circuit is 3000 μmho and the load resistance is 10 kΩ. Calculate the voltage amplification of the circuit assuming that* $r_d >> R_L$.

Solution. $g_{fs} = 3000\,\mu\text{mho} = 3000 \times 10^{-6}$ mho and $R_L = 10\,\text{k}\Omega = 10{,}000\,\Omega$

As $r_d >> R_L$, $\therefore$ $A_v = g_{fs} R_L = (3000 \times 10^{-6}) \times (10{,}000) = \mathbf{30}$

Example 21.10. *In the JFET circuit shown in Fig. 21.22, find (i) V_{DS} and (ii) V_{GS}*

Solution.

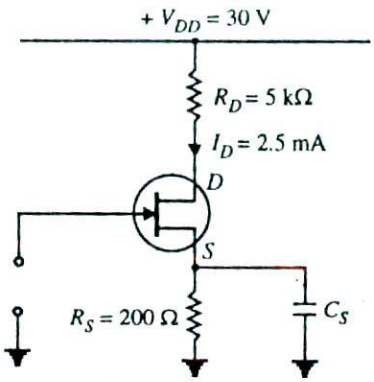


Fig. 21.22

(*i*) $V_{DS} = V_{DD} - I_D(R_D + R_S) = 30 - 2.5\,\text{mA}\,(5 + 0.2) = 30 - 13 = \mathbf{17\ V}$

(*ii*) $V_{GS} = -I_D R_S = -(2.5 \times 10^{-3}) \times 200 = \mathbf{-0.5\ V}$

Example 21.11. *Figure 21.23 shows two stages of JFET amplifier. The first stage has I_D = 2.15mA and the second stage has I_D = 9.15mA. Find the d.c. voltage of drain and source of each stage w.r.t. ground.*

Solution. Voltage drop in 8.2 kΩ = 2.15 mA × 8.2 kΩ = 17.63 V

D.C. Potential of drain of first stage *w.r.t.* ground is

$V_D = V_{DD} - 17.63 = 30 - 17.63 = \mathbf{12.37\ V}$

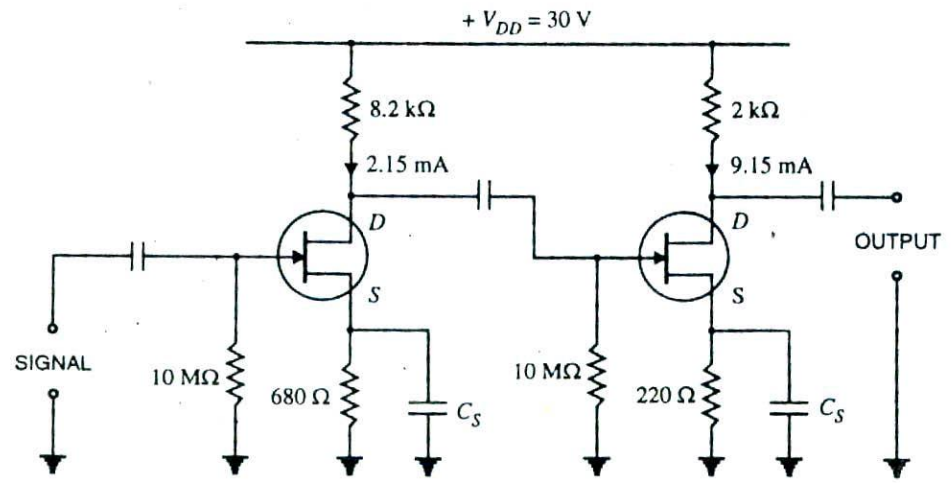


Fig. 21.23

D.C. potential of source of first stage to ground is

$$V_S = I_D R_S = 2.15\,\text{mA} \times 0.68\,\text{k}\Omega = \mathbf{1.46\,V}$$

$$\text{Voltage drop in } 2\,\text{k}\Omega = 9.15\,\text{mA} \times 2\,\text{k}\Omega = 18.3\,\text{V}$$

D.C. potential of drain of second stage to ground is

$$V_D = V_{DD} - 18.3 = 30 - 18.3 = \mathbf{11.7\,V}$$

D.C. potential of source of second stage to ground is

$$V_S = I_D R_S = 9.15\,\text{mA} \times 0.22\,\text{k}\Omega = \mathbf{2.01\,V}$$

21.17 JFET Applications

The high input impedance and low output impedance and low noise level make *JFET* far superior to the bipolar transistor. Some of the circuit applications of *JFET* are :

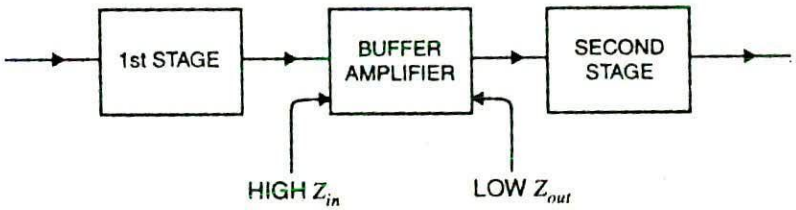


Fig. 21.24

(*i*) **As a buffer amplifier.** A buffer amplifier is a stage of amplification that isolates the preceding stage from the following stage. Because of the high input impedance and low output impedance, a *JFET* can act as an excellent buffer amplifier (See Fig. 21.24). The high input impedance of *JFET* means light loading of the preceding stage. This permits almost the entire output from first stage to appear at the buffer input. The low output impedance of *JFET* can drive heavy loads (or small load resistances). This ensures that all the output from the buffer reaches the input of the second stage.

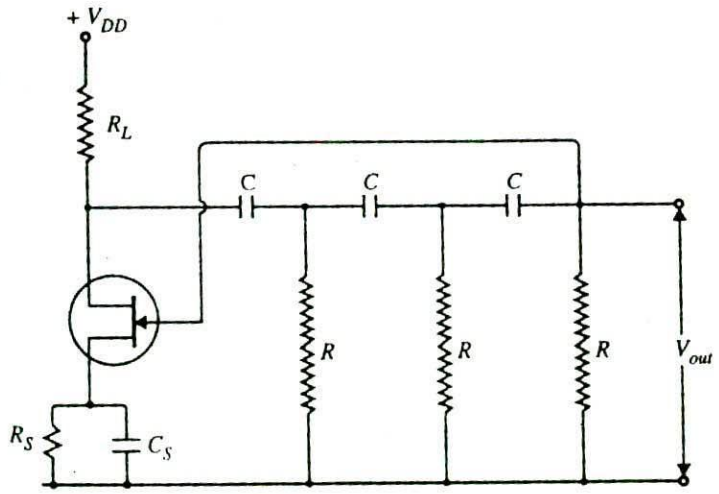


Fig. 21.25

(*ii*) **Phase-shift oscillators.** The oscillators discussed in chapter 16 will also work with *JFETs*. However, the high input impedance of *JFET* is especially valuable in phase-shift oscillators to minimise the loading effect. Fig. 21.25 shows the phase-shift oscillator using *n*-channel *JFET*.

(*iii*) **As RF amplifier.** In communication electronics, we have to use *JFET RF* amplifier in a receiver instead of *BJT* amplifier for the following reasons :

(*a*) The noise level of *JFET* is very low. The *JFET* will not generate significant amount of noise and is thus useful as an *RF* amplifier.

(*b*) The antenna of the receiver receives a very weak signal that has an extremely low amount of current. Since *JFET* is a voltage controlled device, it will well respond to low current signal provided by the antenna.

21.18 Metal Oxide Semiconductor FET (MOSFET)

Metal oxide semiconductor field effect transistor is an important semi-conductor device and is widely used in many circuit applications. The input impedance of a *MOSFET* is much more than that of a *JFET* because of very small gate leakage current. The *MOSFET* can be used in any of the circuits covered for the *JFET*. Therefore, all the equations apply equally well to the *MOSFET* and *JFET* in amplifier connections.

Constructional details. Fig. 21.26 (*i*) shows the constructional details of *n*-channel *MOSFET*. It is similar to *JFET* except with the following modifications :

(*i*) There is only a single *p*-region. This region is called subtrate.

(*ii*) A thin layer of metal oxide (usually silicon dioxide) is deposited over the left side of the channel. A metallic *gate* is deposited over the oxide layer. As silicon dioxide is an insulator, therefore, gate is insulated from the channel. For this reason, *MOSFET* is sometimes called *insulated gate FET*.

(*iii*) Like *JFET*, a *MOSFET* has three terminals *viz*. source, gate and drain.

Fig. 21.26 (*ii*) shows the schematic symbol of *n*-channel *MOSFET*.

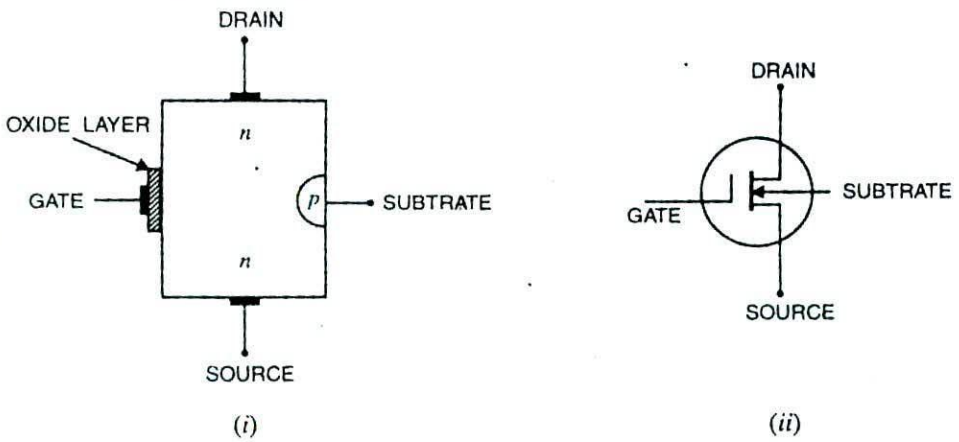


Fig. 21.26

21.19 Working Principle of MOSFET

Fig. 21.27 shows the circuit of *MOSFET*. Instead of gate diode as in *JFET*, here gate is formed as a small capacitor. One plate of this capacitor is the gate and the other plate is the channel with metal oxide as the dielectric. When negative voltage is applied to the gate, electrons accumulate on it.

These electrons *repel the conduction band electrons in the *n*-channel. Therefore, lesser number of conduction electrons are made available for current conduction through the channel. The greater the negative voltage on the gate, the lesser is the current conduction from source to drain. If the gate is given positive voltage, more electrons are made available in the *n*-channel. Consequently, current from source to drain increases. The following points may be noted:

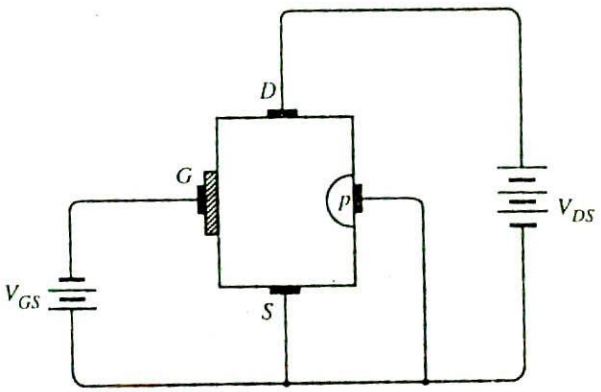


Fig. 21.27

(*i*) In a *MOSFET*, the source to drain current is controlled by the electric field of capacitor formed at the gate.

(*ii*) Unlike the *JFET*, a *MOSFET* has no gate diode. This makes it possible to operate the device with positive or negative gate voltage.

(*iii*) As the gate forms a capacitor, therefore, negligible gate current flows whether positive or negative voltage is applied to the gate. Consequently, the input impedance of *MOSFET* is very high, ranging from 10,000MΩ to 10,000,00MΩ.

Multiple-Choice Questions

1. A *JFET* has three terminals, namely .....
   (*i*) cathode, anode, grid
   (*ii*) emitter, base, collector
   (*iii*) source, gate, drain
   (*iv*) none of the above
2. A *JFET* is similar in operation to ..... valve.
   (*i*) diode (*ii*) pentode
   (*iii*) triode (*iv*) tetrode
3. A *JFET* is also called ..... transistor.
   (*i*) unipolar (*ii*) bipolar
   (*iii*) unijunction (*iv*) none of the above
4. A *JFET* is a ..... driven device.
   (*i*) current
   (*ii*) voltage
   (*iii*) both current and voltage
   (*iv*) none of the above
5. The gate of a *JFET* is ..... biased.
   (*i*) reverse
   (*ii*) forward
   (*iii*) reverse as well as forward
   (*iv*) none of the above
6. The input impedance of a *JFET* is ..... that of an ordinary transistor.
   (*i*) equal to (*ii*) less than
   (*iii*) more than (*iv*) none of the above
7. In a *p*-channel *JFET*, the charge carriers are .....
   (*i*) electrons
   (*ii*) holes
   (*iii*) both electrons and holes
   (*iv*) none of the above.
8. When drain voltage equals the pinch-off voltage, then drain current ..... with the increase in drain voltage.
   (*i*) decreases
   (*ii*) increases
   (*iii*) remains constant
   (*iv*) none of the above
9. If the reverse bias on the gate of a *JFET* is increased, then width of the conducting channel .....

* If one plate of capacitor is negatively charged, it induces positive charge on the other plate.

(*i*) is decreased
(*ii*) is increased
(*iii*) remains the same
(*iv*) none of the above

10. A *MOSFET* has ..... terminals.
(*i*) two (*ii*) five
(*iii*) four (*iv*) three

11. A *MOSFET* can be operated with .....
(*i*) negative gate voltage only
(*ii*) positive gate voltage only
(*iii*) positive as well as negative gate voltage
(*iv*) none of the above

12. A *JFET* has ..... power gain.
(*i*) small (*ii*) very high
(*iii*) very small (*iv*) none of the above

13. The input control parameter of a *JFET* is .....
(*i*) gate voltage (*ii*) source voltage
(*iii*) drain voltage (*iv*) gate current

14. A common base configuration of a *pnp* transistor is analogous to ..... of a *JFET*.
(*i*) common source configuration
(*ii*) common drain configuration
(*iii*) common gate configuration
(*iv*) none of the above

15. A *JFET* has high input impedance because .....
(*i*) it is made of semiconductor material
(*ii*) input is reverse biased
(*iii*) of impurity atoms
(*iv*) none of the above

16. In a *JFET*, when drain voltage is equal to pinch-off voltage, the depletion layers .....
(*i*) almost touch each other
(*ii*) have large gap
(*iii*) have moderate gap
(*iv*) none of the above

17. In a *JFET*, I_{DSS} is known as .....
(*i*) drain to source current
(*ii*) drain to source current with gate shorted
(*iii*) drain to source current with gate open
(*iv*) none of the above

18. The two important advantages of a *JFET* are .....
(*i*) high input impedance and square-law property
(*ii*) inexpensive and high output impedance
(*iii*) low input impedance and high output impedance
(*iv*) none of the above

19. ..... has the lowest noise-level.
(*i*) triode (*ii*) ordinary transistor
(*iii*) tetrode (*iv*) *JFET*

20. A *MOSFET* is sometimes called ..... *JFET*.
(*i*) many gate (*ii*) open gate
(*iii*) insulated gate (*iv*) shorted gate

21. Which of the following devices has the highest input impedance ?
(*i*) *JFET*
(*ii*) *MOSFET*
(*iii*) crystal diode
(*iv*) ordinary transistor

22. A *MOSFET* uses the electric field of a ..... to control the channel current.
(*i*) capacitor (*ii*) battery
(*iii*) generator (*iv*) none of the above

23. The pinch-off voltage in a *JFET* is analogous to ..... voltage in a vacuum tube.
(*i*) anode
(*ii*) cathode
(*iii*) grid cut off
(*iv*) none of the above

24. The formula for a.c. drain resistance of a *JFET* is .....
(*i*) $\frac{\Delta V_{DS}}{\Delta I_D}$ at constant V_{GS}
(*ii*) $\frac{\Delta V_{GS}}{\Delta I_D}$ at constant V_{DS}
(*iii*) $\frac{\Delta I_D}{\Delta V_{GS}}$ at constant V_{DS}
(*iv*) $\frac{\Delta I_D}{\Delta V_{DS}}$ at constant V_{GS}

25. In class A operation, the input circuit of a *JFET* is ..... biased.

(*i*) forward (*ii*) reverse
(*iii*) not (*iv*) none of the above

26. If the gate of a *JFET* is made less negative, the width of the conducting channel .....
(*i*) remains the same
(*ii*) is decreased
(*iii*) is increased
(*iv*) none of the above

27. The pinch-off voltage of a *JFET* is about .....
(*i*) 5 V (*ii*) 0.6 V
(*iii*) 15 V (*iv*) 25 V

28. The input impedance of a *MOSFET* is of the order of .....
(*i*) Ω (*ii*) a few hundred Ω
(*iii*) k Ω (*iv*) several M Ω

29. The gate voltage in a *JFET* at which drain current becomes zero is called ..... voltage.
(*i*) saturation (*ii*) pinch-off
(*iii*) active (*iv*) cut-off

30. The drain current I_D in a *JFET* is given by .....
(*i*) $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$
(*ii*) $I_D = I_{DSS}\left(1 + \frac{V_{GS}}{V_P}\right)^2$
(*iii*) $I_D = I_{DSS}\left(1 - \frac{V_P}{V_{GS}}\right)^2$
(*iv*) $I_D = I_{DSS}\left(1 + \frac{V_P}{V_{GS}}\right)^{1/2}$

31. In a *FET*, there are ..... *pn* junctions at the sides.
(*i*) three (*ii*) four
(*iii*) five (*iv*) two

32. The transconductance of a *JFET* ranges from .....
(*i*) 100 to 500 mA/V
(*ii*) 500 to 1000 mA/V
(*iii*) 0.5 to 30 mA/V
(*iv*) above 1000 mA/V

33. The source terminal of a *JFET* corresponds to ..... of a vacuum tube.
(*i*) plate (*ii*) cathode
(*iii*) grid (*iv*) none of the above

34. The output characteristics of a *JFET* closely resemble the output characteristics of a ..... valve
(*i*) pentode (*ii*) tetrode
(*iii*) triode (*iv*) diode

35. If the cross-sectional area of the channel in *n*-channel *JFET* increases, the drain current .....
(*i*) is increased
(*ii*) is decreased
(*iii*) remains the same
(*iv*) none of the above

36. The channel of a *JFET* is between the .....
(*i*) gate and drain
(*ii*) drain and source
(*iii*) gate and source
(*iv*) input and output

37. For V_{GS}= 0 V, the drain current becomes constant when V_{DS} exceeds .....
(*i*) cut off (*ii*) V_{DD}
(*iii*) V_P (*iv*) 0 V

38. A certain *JFET* data sheet gives $V_{GS(off)}$ = – 4 V. The pinch-off voltage V_P is .....
(*i*) + 4 V (*ii*) – 4 V
(*iii*) dependent on V_{GS}
(*iv*) data insufficient

39. The constant-current region of a *JFET* lies between .....
(*i*) cut off and saturation
(*ii*) cut off and pinch-off
(*iii*) 0 and I_{DSS}
(*iv*) pinch-off and breakdown

40. At cut-off, the *JFET* channel is .....
(*i*) at its widest point
(*ii*) completely closed by the depletion region
(*iii*) extremely narrow
(*iv*) reverse biased

Answers to Multiple-Choice Questions

1. (*iii*)	**2.** (*ii*)	**3.** (*i*)	**4.** (*ii*)	**5.** (*i*)
6. (*iii*)	**7.** (*ii*)	**8.** (*iii*)	**9.** (*i*)	**10.** (*iv*)
11. (*iii*)	**12.** (*ii*)	**13.** (*i*)	**14.** (*iii*)	**15.** (*ii*)
16. (*i*)	**17.** (*ii*)	**18.** (*i*)	**19.** (*iv*)	**20.** (*iii*)
21. (*ii*)	**22.** (*i*)	**23.** (*iii*)	**24.** (*i*)	**25.** (*ii*)
26. (*iii*)	**27.** (*i*)	**28.** (*iv*)	**29.** (*ii*)	**30.** (*i*)
31. (*iv*)	**32.** (*iii*)	**33.** (*ii*)	**34.** (*i*)	**35.** (*i*)
36. (*ii*)	**37.** (*iii*)	**38.** (*i*)	**39.** (*iv*)	**40.** (*ii*)

Chapter Review Topics

1. Explain the construction and working of a *JFET*.
2. What is the difference between a *JFET* and a bipolar transistor ?
3. How will you determine the drain characteristics of *JFET* ? What do they indicate?
4. Define the *JFET* parameters and establish the relationship between them.
5. Briefly describe some practical applications of *JFET*.
6. Explain the construction and working of *MOSFET*.
7. Write short notes on the following :
   (*i*) Advantages of *JFET* (*ii*) Difference between *MOSFET* and *JFET*

Problems

1. A *JFET* has a drain current of 5 mA. It I_{DSS} = 10 mA and $V_{GS(off)}$ is – 6 V, find the value of (*i*) V_{GS} and (*ii*) V_P. **[(*i*) – 1.5 V (*ii*) 6 V]**
2. A *JFET* has an I_{DSS} of 9 mA and a $V_{GS(off)}$ of – 3V. Find the value of drain current when V_{GS} = –1.5V. **[2.25mA]**
3. In the *JFET* circuit shown in Fig. 21.28 if I_D = 1.9 mA, find V_{GS} and V_{DS}. **[– 1.56V; 13.5V]**

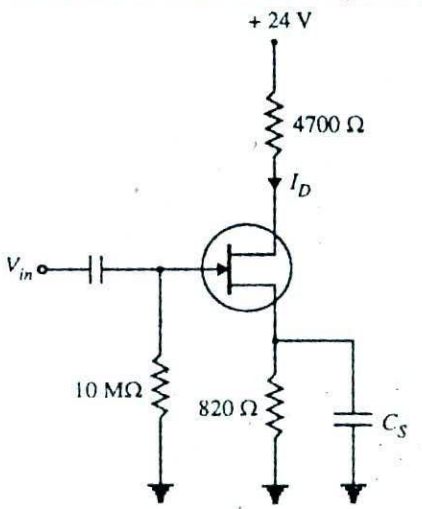


Fig. 21.28

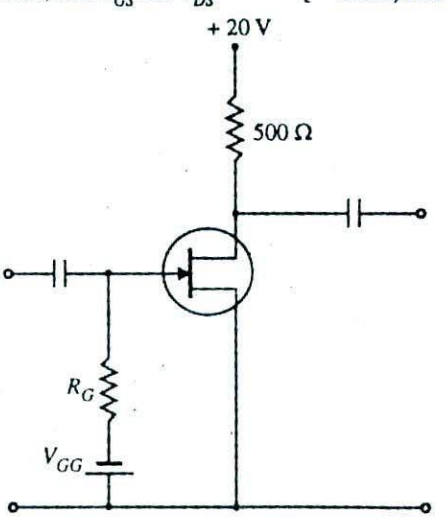


Fig. 21.29

4. For the *JFET* amplifier shown in Fig. 21.29, draw the d.c. load line.
5. For a *JFET*, I_{DSS} = 9 mA and V_P = –3.5 V. Determine I_D when (*i*) V_{GS} = 0 V (*ii*) V_{GS} = – 2V. **[(*i*) 9mA (*ii*) 1.65 mA]**
6. Sketch the transfer curve for a *P*-channel *JFET* with I_{DSS} = 4 mA and V_P = 3 V.

22

Silicon Controlled Rectifiers

Introduction

The silicon controlled rectifier (abbreviated as SCR) is a three terminal semi-conductor switching device which is probably the most important circuit element after the diode and the transistor. Invented in 1957, an SCR can be used as a controlled switch to perform various functions such as rectification, inversion and regulation of power flow. The SCR has assumed paramount importance in electronics because it can be produced in versions to handle currents upto several thousand amperes and voltages upto more than 1 kV.

The SCR has appeared in the market under different names such as thyristor, thyrode and transistor. It is a unidirectional power switch and is being extensively used in switching d.c. and a.c., rectifying a.c. to give controlled d.c. output, converting d.c. into a.c. etc. In this chapter, we shall examine the various characteristics of silicon controlled rectifiers and their increasing applications in power electronics.

22.1 Silicon Controlled Rectifier (SCR)

A silicon *controlled rectifier is a semiconductor **device that acts as a true electronic switch. It can

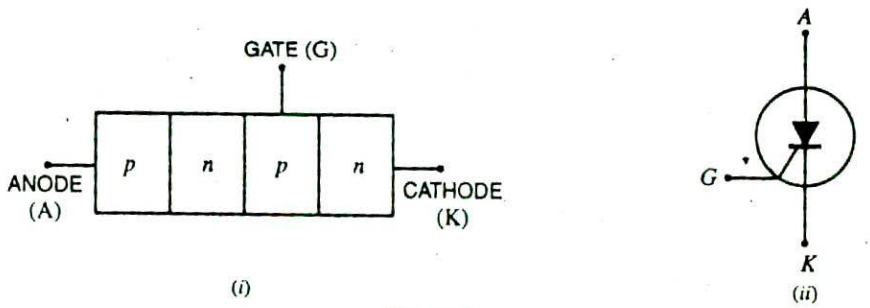


Fig. 22.1

change alternating current into direct current and at the same time can control the amount of power fed to the load. Thus SCR combines the features of a rectifier and a transistor.

* **Why not germanium controlled rectifier ?** The device is made of silicon because leakage current in silicon is very small as compared to germanium. Since the device is used as a switch, it will carry leakage current in the off condition which should be as small as possible.

** It got this name because it is a silicon device and is used as a rectifier and that rectification can be controlled.

Constructional details. When a *pn* junction is added to a junction transistor, the resulting three *pn* junction device is called a silicon controlled rectifier. Fig. 22.1 (*i*) shows its construction. It is clear that it is essentially an ordinary rectifier (*pn*) and a junction transistor (*npn*) combined in one unit to form *pnpn device*. Three terminals are taken; one from the outer *p-type* material called *anode A*, second from the outer *n*-type material called *cathode K* and the third from the base of transistor section and is called *gate G*. In the normal operating conditions of *SCR*, anode is held at high positive potential *w.r.t.* cathode and gate at small positive potential *w.r.t.* cathode. Fig. 22.1 (*ii*) shows the symbol of *SCR*.

The silicon controlled rectifier is a solid state equivalent of thyratron. The gate, anode and cathode of *SCR* correspond to the grid, plate and cathode of thyratron. For this reason, *SCR* is sometimes called *thyristor*.

22.2 Working of SCR

In a silicon controlled rectifier, load is connected in series with anode. The anode is always kept at positive potential *w.r.t.* cathode. The working of *SCR* can be studied under the following two heads.

(*i*) **When gate is open.** Fig. 22.2 shows the *SCR* circuit with gate open *i.e.* no voltage applied to the gate. Under this condition, junction J_2 is reverse biased while junctions J_1 and J_3 are forward biased. Hence, the situation in the junctions J_1 and J_3 is just as in a *npn* transistor with base open. Consequently, no current flows through the load R_L and the *SCR* is *cut off*. However, if the applied voltage is gradually increased, a stage is reached when * reverse biased junction J_2 breaks down. The *SCR* now conducts ** heavily and is said to be in the *ON* state. The applied voltage at which *SCR* conducts heavily without gate voltage is called *Breakover voltage*.

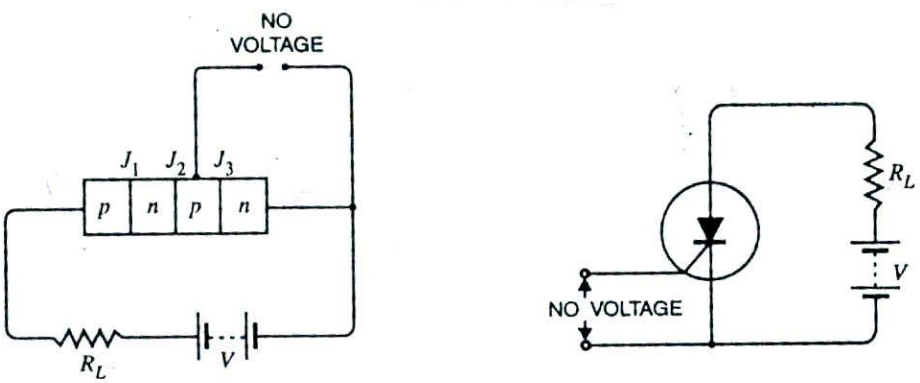


Fig. 22.2

(*ii*) **When gate is positive w.r.t. cathode.** The *SCR* can be made to conduct heavily at smaller applied voltage by applying a small positive potential to the gate as shown in Fig. 22.3. Now junction J_3 is forward biased and junction J_2 is reverse biased. The electrons from *n*-type material start moving across junction J_3 towards left whereas holes from *p*-type towards the right. Consequently, the electrons from junction J_3 are attracted across junction J_2 and gate current starts flowing. As soon as the gate current flows, anode current increases. The increased anode current in turn makes more electrons available at junction J_2. This process continues and in an extremely small time, junction J_2

---

* The whole applied voltage V appears as reverse bias across junction J_2 as junctions J_1 and J_3 are forward biased.

** Because J_1 and J_3 are forward biased and J_2 has broken down.

breaks down and the *SCR* starts conducting heavily. *Once SCR starts conducting, the gate* (the reason for this name is obvious) *loses all control.* Even if gate voltage is removed, the anode current does not decrease at all. The only way to stop conduction (*i.e.* bring *SCR* in off condition) is to reduce the applied voltage to zero.

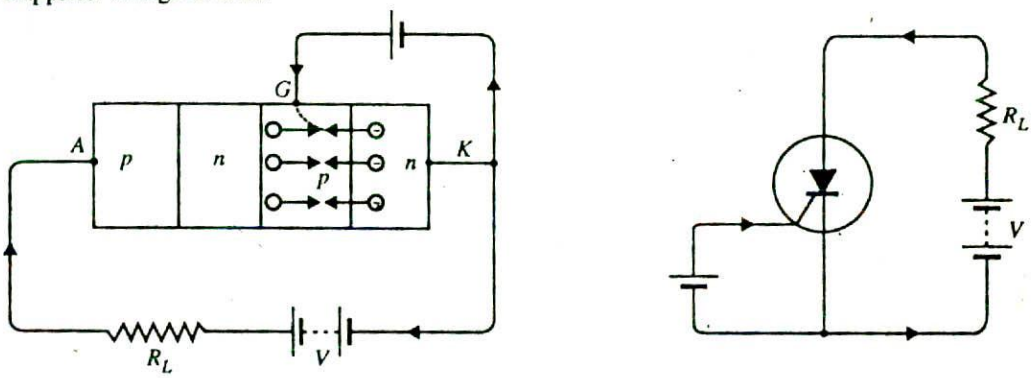


Fig: 22.3

Conclusion. The following conclusions are drawn from the working of *SCR* :

(*i*) An *SCR* has two states *i.e.* either it does not conduct or it conducts heavily. There is no state in between. Therefore, *SCR* behaves like a switch.

(*ii*) There are two ways to turn on the *SCR*. The first method is to keep the gate open and make the supply voltage equal to the breakover voltage. The second method is to operate *SCR* with supply voltage less than breakover voltage and then turn it on by means of a small voltage (typically 1.5 V, 30 mA) applied to the gate.

(*iii*) Applying small positive voltage to the gate is the normal way to close an *SCR* because the breakover voltage is usually much greater than supply voltage.

(*iv*) To open the *SCR* (*i.e.* to make it non-conducting), reduce the supply voltage to zero.

22.3 Equivalent Circuit of SCR

The *SCR* shown in Fig. 22.4 (*i*) can be visualised as separated into two transistors as shown in

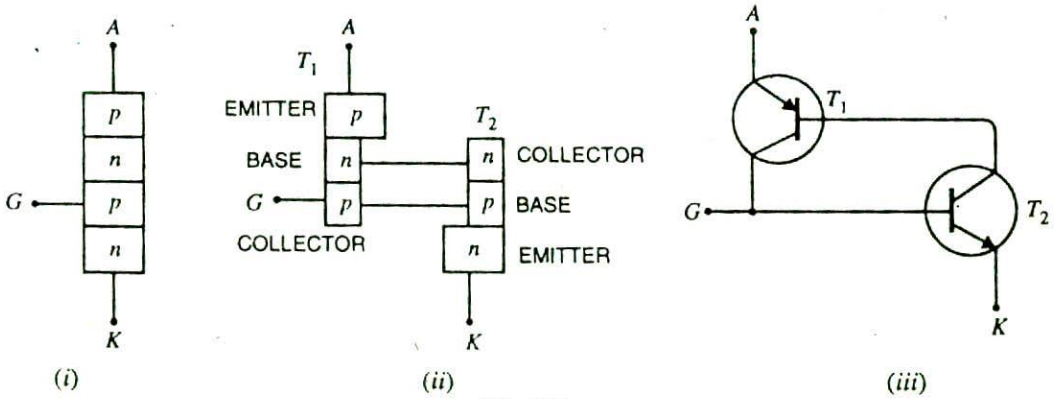


Fig. 22.4

Fig. 22.4 (*ii*). Thus, the equivalent circuit of *SCR* is composed of *pnp* transistor and *npn* transistor connected as shown in Fig. 22.4. (*iii*). It is clear that collector of each transistor is coupled to the base of the other, thereby making a positive feedback loop.

The working of *SCR* can be easily explained from its equivalent circuit. Fig. 22.5. shows the equivalent circuit of *SCR* with supply voltage V and load resistance R_L. Assume the supply voltage V is less than breakover voltage as is usually the case. With gate open (*i.e.* switch *S* open), there is no base current in transistor T_2. Therefore, no current flows in the collector of T_2 and hence that of T_1. Under such conditions, the *SCR* is open. However, if switch *S* is closed, a small gate current will flow through the base of T_2 which means its collector current will increase. The collector current of T_2 is the base current of T_1. Therefore, collector current of T_1 increases. But collector current of T_1 is the base current of T_2. This action is accumulative since an increase of current in one transistor causes an increase of current in the other transistor. As a result of this action, both transistors are driven to saturation, and heavy current flows through the load R_L. Under such conditions, the *SCR* closes.

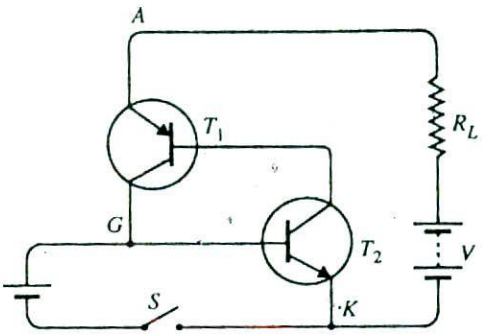


Fig. 22.5

22.4 Important Terms

The following terms are much used in the study of *SCR* :

(*i*) Breakover voltage (*ii*) Peak reverse voltage

(*iii*) Holding current (*iv*) Forward current rating

(*v*) Circuit fusing rating

(*i*) **Breakover voltage.** *It is the minimum forward voltage, gate being open, at which SCR starts conducting heavily i.e. turned on.*

Thus, if the breakover voltage of an *SCR* is 200 V, it means that it can block a forward voltage (*i.e. SCR* remains open) as long as the supply voltage is less than 200 V. If the supply voltage is more than this value, then *SCR* will be turned on. In practice, the *SCR* is operated with supply voltage less than breakover voltage and it is then turned on by means of a small voltage applied to the gate. Commercially available *SCRs* have breakover voltages from about 50 V to 500 V.

(*ii*) **Peak reverse voltage (*PRV*).** *It is the maximum reverse voltage (cathode positive w.r.t. anode) that can be applied to an SCR without conducting in the reverse direction.*

Peak reverse voltage (*PRV*) is an important consideration while connecting an *SCR* in an a.c. circuit. During the negative half of a.c. supply, reverse voltage is applied across *SCR*. If *PRV* is exceeded, there may be avalanche breakdown and the *SCR* will be damaged if the external circuit does not limit the current. Commercially available *SCRs* have PRV ratings upto 2.5 kV.

(*iii*) **Holding current.** *It is the maximum anode current, gate being open, at which SCR is turned off from ON conditions.*

As discussed earlier, when *SCR* is in the conducting state, it cannot be turned OFF even if gate voltage is removed. The only way to turn off or open the *SCR* is to reduce the supply voltage to almost zero at which point the internal transistor comes out of saturation and opens the *SCR*. The anode current under this condition is very small (a few mA) and is called *holding current*. Thus, if an *SCR* has a holding current of 5mA, it means that if anode current is made less than 5mA, then SCR will be turned off.

(*iv*) **Forward current rating.** *It is the maximum anode current that an SCR is capable of passing without destruction.*

Every *SCR* has a safe value of forward current which it can conduct. If the value of current exceeds this value, the *SCR* may be destroyed due to intensive heating at the junctions. For example, if an SCR has a forward current rating of 40A, it means that the *SCR* can safely carry only 40 A. Any attempt to exceed this value will result in the destruction of the *SCR*. Commercially available *SCRs* have forward current ratings from about 30A to 100A.

(*v*) **Circuit fusing (I^2t) rating.** *It is the product of square of forward surge current and the time of duration of the surge i.e.,*

$$\text{Circuit fusing rating} = I^2t$$

The circuit fusing rating indicates the maximum forward surge current capability of *SCR*. For example, consider an *SCR* having circuit fusing rating of 90 A^2s. If this rating is exceeded in the *SCR* circuit, the device will be destroyed by excessive power dissipation.

Example 22.1. *An SCR has a breakover voltage of 400 V, a trigger current of 10 mA and holding current of 10 mA. What do you infer from it ? What will happen if gate current is made 15 mA ?*

Solution. (*i*) *Breakover voltage of 400 V.* It means that if gate is open and the supply voltage is 400 V, then *SCR* will start conducting heavily. However, as long as the supply voltage is less than 400 V, the *SCR* stays open *i.e.* it does not conduct.

(*ii*) *Trigger current of 10 mA.* It means that if the supply voltage is less than breakover voltage (*i.e.* 400 V) and a minimum gate current of 10 mA is passed, the *SCR* will close *i.e.* starts conducting heavily. The *SCR* will not conduct if the gate current is less than 10 mA. It may be emphasised that triggering is the normal way to close an *SCR* as the supply voltage is normally much less than the breakover voltage.

(*iii*) *Holding current of 10 mA.* When the *SCR* is conducting, it will not open (*i.e.* stop conducting) even if triggering current is removed. However, if supply voltage is reduced, the anode current also decreases. When the anode current drops to 10 mA, the holding current, the *SCR* is turned off.

(*iv*) If gate current is increased to 15 mA, the *SCR* will be turned on lower supply voltage.

Example 22.2. *An SCR in a circuit is subjected to a 50 A surge that lasts for 12 ms. Determine whether or not this surge will destroy the device. Given that circuit fusing rating is 90 A^2s.*

Solution. Circuit fusing rating $= I^2t = (50)^2 \times (12 \times 10^{-3}) = \mathbf{30\ A^2s}$

Since this value is well below the maximum rating of 90 A^2s, the device will not be destroyed.

Example 22.3. *An SCR has a circuit fusing rating of 50 A^2s. The device is being used in a circuit where it could be subjected to a 100 A surge. Determine the maximum allowable duration of such a surge.*

Solution. $t_{max} = \dfrac{I^2t\ (\text{rating})}{I_s^2}$ where I_s = known value of surge current

$\therefore$ $t_{max} = \dfrac{50}{(100)^2} = 5 \times 10^{-3}s = \mathbf{5\ ms}$

22.5 V-I Characteristics of SCR

It is the curve between anode-cathode voltage (V) and anode current (I) of an *SCR* at constant gate current. Fig. 22.6 shows the *V-I* characteristics of a typical *SCR*.

(*i*) **Forward characteristics.** When anode is positive *w.r.t.* cathode, the curve between V and I is called the forward characteristic. In Fig. 22.6, *OABC* is the forward characteristic of *SCR* at $I_G = 0$. If the supply voltage is increased from zero, a point is reached (point A) when the *SCR* starts

conducting. Under this condition, the voltage across *SCR* suddenly drops as shown by dotted curve *AB* and most of supply voltage appears across the load resistance R_L. If proper gate current is made to flow, *SCR* can close at much smaller supply voltage.

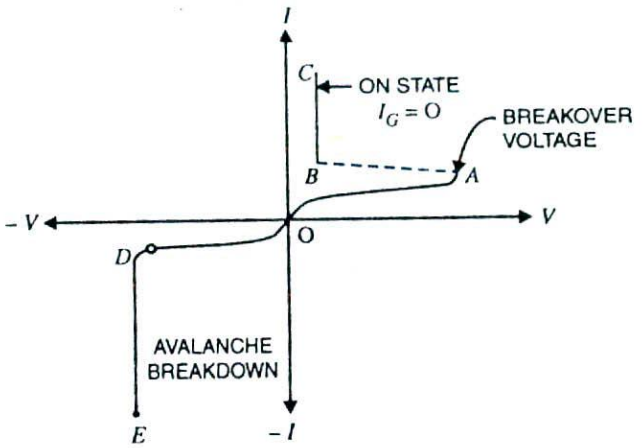


Fig. 22.6

(*ii*) **Reverse characteristics.** When anode is negative *w.r.t.* cathode, the curve between *V* and *I* is known as *reverse characteristic*. The reverse voltage does come across *SCR* when it is operated with a.c. supply. If the reverse voltage is gradually increased, at first the anode current remains small (*i.e.* leakage current) and at some reverse voltage, avalanche breakdown occurs and the *SCR* starts conducting heavily in the reverse direction as shown by the curve *DE*. This maximum reverse voltage at which *SCR* starts conducting heavily is known as *reverse breakdown voltage*.

22.6 SCR in Normal Operation

In order to operate the *SCR* in normal operation, the following points are kept in view :

(*i*) The supply voltage is generally much less than breakover voltage.

(*ii*) The *SCR* is turned on by passing an appropriate amount of gate current (a few mA) and not by breakover voltage.

(*iii*) When *SCR* is operated from a.c. supply, the peak reverse voltage which comes during negative half-cycle should not exceed the reverse breakdown voltage.

(*iv*) When *SCR* is to be turned OFF from the ON state, anode current should be reduced to holding current.

(*v*) If gate current is increased above the required value, the *SCR* will close at much reduced supply voltage.

22.7 SCR as a Switch

The *SCR* has only two states, namely; ON state and OFF state and no state inbetween. When appropriate gate current is passed, the *SCR* starts conducting heavily and remains in this position indefinitely even if gate voltage is removed. This corresponds to the ON condition. However, when the anode current is reduced to the holding current, the *SCR* is turned OFF. It is clear that behaviour of *SCR* is similar to a mechanical switch. As *SCR* is an electronic device, therefore, it is more appropriate to call it an *electronic switch*.

Advantages of *SCR* as a switch. An *SCR* has the following advantages over a mechanical or electromechanical switch (relay) :

(*i*) It has no moving parts. Consequently, it gives noiseless operation at high efficiency.

(*ii*) The switching speed is very high upto 10^9 operations per second.

(*iii*) It permits control over large current (30-100 A) in the load by means of a small gate current (a few mA).

(*iv*) It has small size and gives trouble free service.

22.8 SCR Switching

We have seen that *SCR* behaves as a switch *i.e.* it has only two states *viz.* ON state and OFF state. It is profitable to discuss the methods employed to turn-on or turn-off an *SCR*.

1. SCR turn-on methods. In order to turn on the *SCR*, the gate voltage V_G is increased upto a minimum value to initiate triggering. This minimum value of gate voltage at which *SCR* is turned ON is called *gate triggering voltage* V_{GT}. The resulting gate current is called gate triggering current I_{GT}. Thus to turn on an *SCR* all that we have to do is to apply positive gate voltage equal to V_{GT} or pass a gate current equal to I_{GT}. For most of the *SCRs*, $V_{GT} = 2$ to 10 V and $I_{GT} = 100\ \mu A$ to 1500 mA. We shall discuss two methods to turn on an *SCR*.

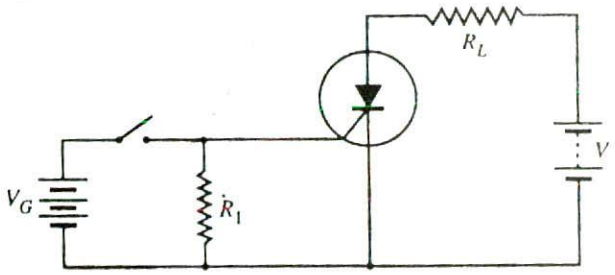


Fig. 22.7

(*i*) *D.C. gate trigger circuit.* Fig. 22.7 shows a typical circuit used for triggering an *SCR* with a d.c. gate bias. When the switch is closed, the gate receives sufficient positive voltage ($= V_{GT}$) to turn the *SCR* on. The resistance R_1 connected in the circuit provides noise suppression and improves the turn-on time. The turn-on time primarily depends upon the magnitude of the gate current. The higher the gate-triggered current, the shorter the turn-on time.

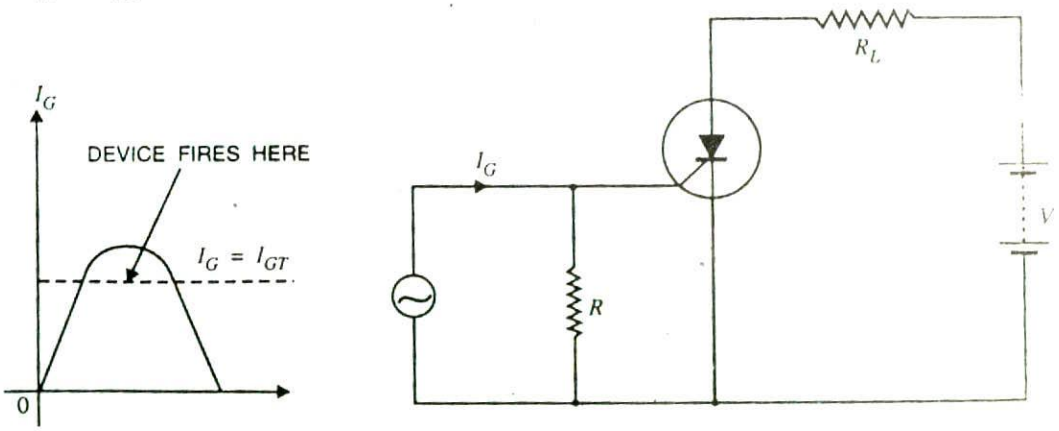


Fig. 22.8

(*ii*) *A.C. trigger circuit.* An *SCR* can also be turned on with positive cycle of a.c. gate current. Fig. 22.8 (*ii*) shows such a circuit. During the positive half cycle of the gate current, at some point $I_G = I_{G1}$, the device is turned on as shown in Fig. 22.8 (*i*).

2. SCR turn-off methods. The *SCR* turn-off poses more problems than *SCR* turn-on. It is because once the device is ON, the gate loses all control. There are many methods of *SCR* turn-off but only two will be discussed.

(*i*) *Anode current interruption.* When the anode current is reduced below a minimum value called holding current, the *SCR* turns off. The simple way to turn off the *SCR* is to open the line switch *S* as shown in Fig. 22.9.

(*ii*) *Forced commutation.* The method of discharging a capacitor in parallel with an *SCR* to turn off the *SCR* is called forced commutation. Fig. 22.10 shows the forced commutation of *SCR* where capacitor *C* performs the commutation. Assuming the *SCRs* are switches with *SCR*1 ON and *SCR*2 OFF, current flows through the load and *C* as shown in Fig. 22.10. When *SCR*2 is triggered on, *C* is effectively paralleled across *SCR*1. The charge on *C* is then opposite to *SCR*1's forward voltage, *SCR*1 is thus turned off and the current is transferred to *R*-*SCR*2 path.

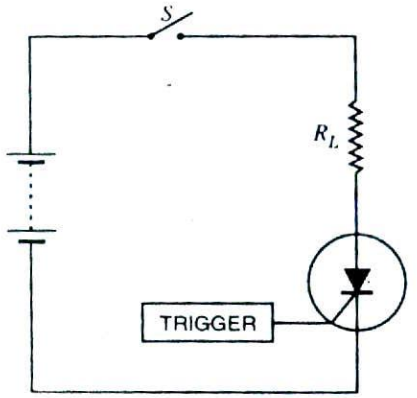


Fig. 22.9

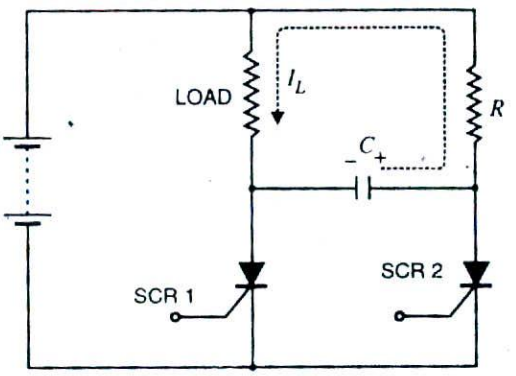
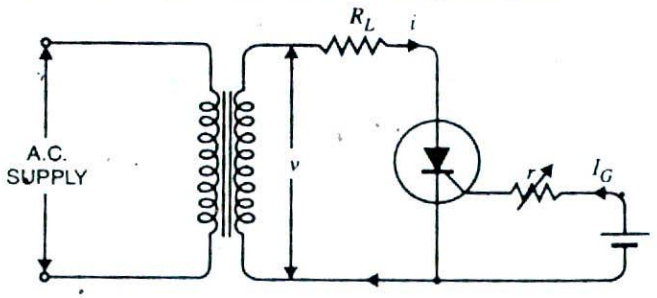


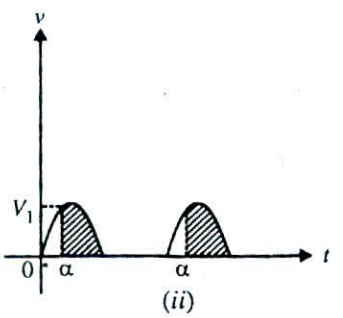
Fig. 22.10

22.9 SCR Half-Wave Rectifier

One important application of an *SCR* is the controlled half-wave rectification. Fig. 22.11 (*i*) shows the circuit of an *SCR* half-wave rectifier. The a.c. supply to be rectified is supplied through the transformer. The load resistance R_L is connected in series with the anode. A variable resistance *r* is inserted in the gate circuit to control the gate current.



(*i*)



(*ii*)

Fig. 22.11

Operation. The a.c. supply to be converted into d.c., supply is applied to the primary of the transformer. Suppose the peak reverse voltage appearing across secondary is less than the reverse breakdown voltage of the *SCR*. This condition ensures that *SCR* will not breakdown during negative half-cycles of a.c. supply. The circuit action is as follows :

(*i*) During the negative half-cycles of a.c. voltage appearing across secondary, the *SCR* does not conduct regardless of the gate voltage. It is because in this condition, anode is negative *w.r.t.* cathode and also *PRV* is less than the reverse breakdown voltage.

(*ii*) The *SCR* will conduct during the positive half-cycles provided proper gate current is made to flow. The greater the gate current, the lesser the supply voltage at which *SCR* is turned ON. The gate current can be changed by the variable resistance *r* as shown in Fig. 22.11 (*i*).

(*iii*) Suppose that gate current is adjusted to such a value that *SCR* closes at a positive voltage V_1 which is less than the peak voltage V_m. Referring to Fig. 22.11 (*ii*), it is clear that *SCR* will start conducting when secondary a.c. voltage becomes V_1 in the positive half-cycle. Beyond this, the *SCR* will continue to conduct till voltage becomes zero at which point it is turned OFF. Again at the start of the next positive half-cycle, *SCR* will start conducting when secondary voltage becomes V_1.

(*iv*) Referring to Fig. 22.11 (*ii*), it is clear that firing angle is α *i.e.* at this angle in the positive half-cycle, *SCR* starts conduction. The conduction angle is ϕ ($= 180° - \alpha$).

It is worthwhile to distinguish between an ordinary half-wave rectifier and *SCR* half-wave rectifier. Whereas an ordinary half-wave rectifier will conduct full positive half-cycle, an *SCR* half-wave rectifier can be made to conduct full or part of a positive half-cycle by proper adjustment of gate current. Therefore, an *SCR* can control power fed to the load and hence the name *controlled rectifier*.

Mathematical treatment. Referring to Fig. 22.11 (*i*), let $v = V_m \sin\theta$ be the alternating voltage that appears across the secondary. Let α be the firing angle. It means that rectifier will conduct from α to 180° during the positive half-cycles.

$$\therefore \quad \text{Average output, } V_{av} = \frac{1}{2\pi}\int_{\alpha}^{180°} V_m \sin\theta\, d\theta = \frac{V_m}{2\pi}\int_{\alpha}^{180°} \sin\theta\, d\theta$$

$$= \frac{V_m}{2\pi}\left[-\cos\theta\right]_{\alpha}^{180°}$$

$$= \frac{V_m}{2\pi}(\cos\alpha - \cos 180°)$$

$$V_{av} = \frac{V_m}{2\pi}(1 + \cos\alpha)$$

$$\text{Average current, } I_{av} = \frac{V_{av}}{R_L} = \frac{V_m}{2\pi R_L}(1 + \cos\alpha)$$

The following points may be noted :

(*i*) If the firing angle $\alpha = 0°$, then full positive half-cycle will appear across the load R_L and the output current becomes :

$$I_{av} = \frac{V_m}{2\pi R_L}(1 + \cos 0°) = \frac{V_m}{\pi R_L}$$

This is the value of average current for ordinary half-wave rectifier. This is expected since the full positive half-cycle is being conducted.

(*ii*) If $\alpha = 90°$, then average current is given by;

$$I_{av} = \frac{V_m}{2\pi R_L}(1 + \cos 90°) = \frac{V_m}{2\pi R_L}$$

This shows that greater the firing angle α, the smaller is the average current and *vice-versa*.

Example 22.4. *A half-wave rectifier circuit employing an SCR is adjusted to have a gate current of 1mA. The forward breakdown voltage of SCR is 100 V for I_g = 1mA. If a sinusoidal voltage of 200 V peak is applied, find :*

(i) firing angle (ii) conduction angle (iii) average current

Assume load resistance = 100Ω and the holding current to be zero.

Solution. $v = V_m \sin\theta$

Here, $v = 100$ V, $V_m = 200$ V

(i) $\therefore \quad 100 = 200 \sin\theta$

or $\sin\theta = \dfrac{100}{200} = 0.5$

$\therefore \quad \theta = \sin^{-1}(0.5) = 30°$ *i.e.* Firing angle, $\alpha = \theta = \mathbf{30°}$

(ii) Conduction angle, $\phi = 180° - \alpha = 180° - 30° = \mathbf{150°}$

(iii) Average voltage $= \dfrac{V_m}{2\pi}(1 + \cos\alpha) = \dfrac{200}{2\pi}(1 + \cos 30°) = 59.25$ V

$\therefore$ Average current $= \dfrac{\text{Average voltage}}{R_L} = \dfrac{59.25}{100} = \mathbf{0.5925\ A}$

Example 22.5. *An SCR half-wave rectifier has a forward breakdown voltage of 150 V when a gate current of 1 mA flows in the gate circuit. If a sinusoidal voltage of 400 V peak is applied, find:*

(i) firing angle (ii) average output voltage

(iii) average current for a load resistance of 200Ω (iv) power output

Assume that the gate current is 1mA throughout and the forward breakdown voltage is more than 400 V when I_g = 1 mA.

Solution. $V_m = 400$ V, $v = 150$ V, $R_L = 200\ \Omega$

(i) Now $v = V_m \sin\theta$

or $\sin\theta = \dfrac{v}{V_m} = \dfrac{150}{400} = 0.375$

i.e. firing angle, $\alpha\ (= \theta) = \sin^{-1} 0.375 = \mathbf{22°}$

(ii) Average output voltage is

$$V_{av} = \frac{V_m}{2\pi}(1 + \cos 22°) = \frac{400}{2\pi}(1 + \cos 22°) = \mathbf{122.6\ V}$$

(iii) Average current, $I_{av} = \dfrac{\text{average output voltage}}{R_L} = \dfrac{122.6}{200} = \mathbf{0.613\ A}$

(iv) Output power $= V_{av} \times I_{av} = 122.6 \times 0.613 = \mathbf{75.15\ W}$

Example 22.6. *An a.c. voltage v = 240 sin314 t is applied to an SCR half-wave rectifier. If the SCR has a forward breakdown voltage of 180 V, find the time during which SCR remains off.*

Solution. The *SCR* will remain off till the voltage across it reaches 180 V. This is shown in Fig. 22.12. Clearly, *SCR* will remain off for *t* second.

Now $v = V_m \sin 314\, t$

Here $v = 180$ V; $V_m = 240$ V

$$\therefore \quad 180 = 240 \sin (314\, t)$$

$$\text{or} \quad \sin 314\, t = \frac{180}{240} = 0.75$$

$$\text{or} \quad 314\, t = \sin^{-1} (0.75)$$

$$= 48.6° = 0.848 \text{ radian}$$

$$\therefore \quad t = \frac{0.848}{314} = 0.0027 \text{ sec} = \textbf{2.7 millisecond}$$

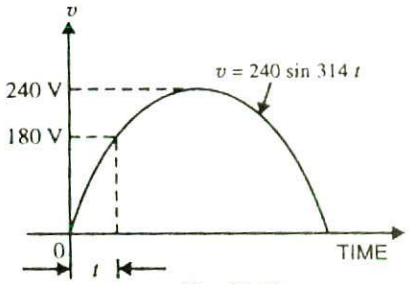


Fig. 22.12

22.10 SCR Full-Wave Rectifier

Fig. 22.13 (*i*) shows the circuit of *SCR* full-wave rectifier. It is exactly like an ordinary centre-tap circuit except that the two diodes have been replaced by two *SCRs*. The gates of both *SCRs* get their

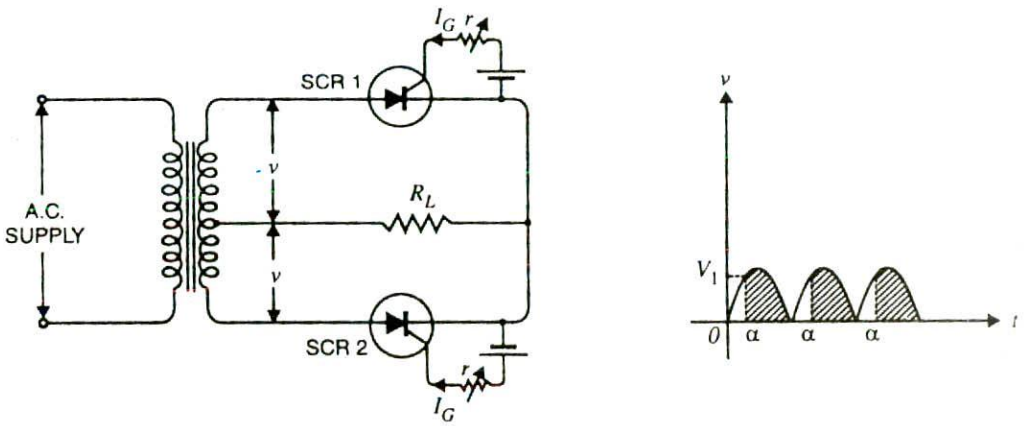


Fig. 22.13

supply from two gate controls. One *SCR* conducts during the positive half-cycle and the other during the negative-half-cycle. Consequently, full-wave rectified output is obtained across the load.

Operation. The angle of conduction can be changed by adjusting the gate currents. Suppose the gate currents are so adjusted that *SCRs* conduct as the secondary voltage (across half winding) becomes V_1. During the positive half-cycle of a.c. across secondary, the upper end of secondary is positive and the lower end negative. This will cause *SCR*1 to conduct. However, the conduction will start only when the voltage across the upper half of secondary becomes V_1 as shown in Fig. 22.13 (*ii*). In this way only shaded portion of positive half-cycle will pass through the load.

During the negative half-cycle of a.c. input, the upper end of secondary becomes negative and the lower end positive. This will cause *SCR*2 to conduct when the voltage across the lower half of secondary becomes V_1. It may be seen that current through the load is in the same direction (d.c.) on both half-cycles of input a.c. The obvious advantage of this circuit over ordinary full-wave rectifier circuit is that by adjusting the gate currents, we can change the conduction angle and hence the output voltage.

Mathematical treatment. Referring to Fig. 22.13 (*i*), let $v = V_m \sin \theta$ be the alternating voltage that appears between centre tap and either end of secondary. Let α be the firing angle.

$$\text{Average output, } V_{av} = \frac{1}{\pi} \int_{\alpha}^{180°} V_m \sin \theta \, d\theta = \frac{V_m}{\pi} \int_{\alpha}^{180°} \sin \theta \, d\theta$$

$$= \frac{V_m}{\pi}[-\cos\theta]_{\alpha}^{180^\circ} = \frac{V_m}{\pi}(\cos\alpha - \cos 180^\circ)$$

$$\therefore \quad V_{av} = \frac{V_m}{\pi}(1 + \cos\alpha)$$

This value is double that of a half-wave rectifier. It is expected since now negative half-cycle is also rectified.

$$\text{Average current, } I_{av} = \frac{V_{av}}{R_L} = \frac{V_m}{\pi R_L}(1 + \cos\alpha)$$

Example 22.7. *An SCR full-wave rectifier supplies to a load of 100 Ω. If the peak a.c. voltage between centre tap and one end of secondary is 200V, find (i) d.c. output voltage and (ii) load current for a firing angle of 60°.*

Solution. $V_m = 200$ V; $\alpha = 60^\circ$; $R_L = 100\ \Omega$

(*i*) D.C. output voltage, $V_{av} = \frac{V_m}{\pi}(1 + \cos\alpha) = \frac{200}{\pi}(1 + \cos 60^\circ) = \mathbf{95.5\ V}$

(*ii*) Load current, $I_{av} = \frac{V_{av}}{R_L} = \frac{95.5}{100} = \mathbf{0.955\ A}$

22.11 Applications of SCR

The ability of an *SCR* to control large currents in a load by means of small gate current makes this device useful in switching and control applications. Some of the important applications of *SCR* are discussed below :

(*i*) **SCR as static contactor.** An important application of *SCR* is for switching operations. As *SCR* has no moving parts, therefore, when it is used as a switch, it is often called a *static contactor.*

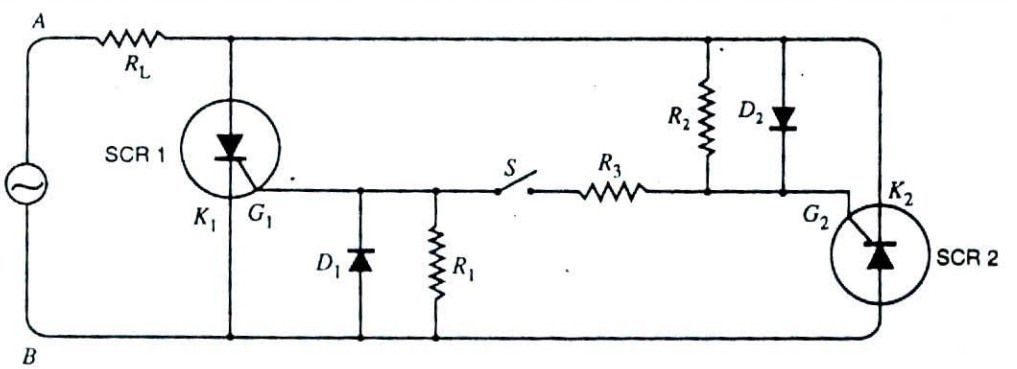


Fig. 22.14

Fig. 22.14 shows the use of *SCR* to switch ON or OFF a.c. power to a load R_L. Resistances R_1 and R_2 are for the protection of diodes D_1 and D_2 respectively. Resistance R_3 is the gate current limiting resistor. To start the circuit, switch is closed. During the positive half-cycle of a.c. supply, end *A* is positive and end *B* is negative. Then diode D_2 sends gate current through *SCR*1. Therefore *SCR*1 is turned ON while *SCR*2 remains OFF as its anode is negative *w.r.t.* cathode. The current conduction by *SCR*1 follows the path AR_LK_1BA. Similarly, in the next half-cycle, *SCR*2 is turned ON and conducts current through the load. It may be seen that switch *S* handles only a few mA of gate current to switch ON several hundred amperes in the load R_L. This is a distinct advantage over a mechanical switch.

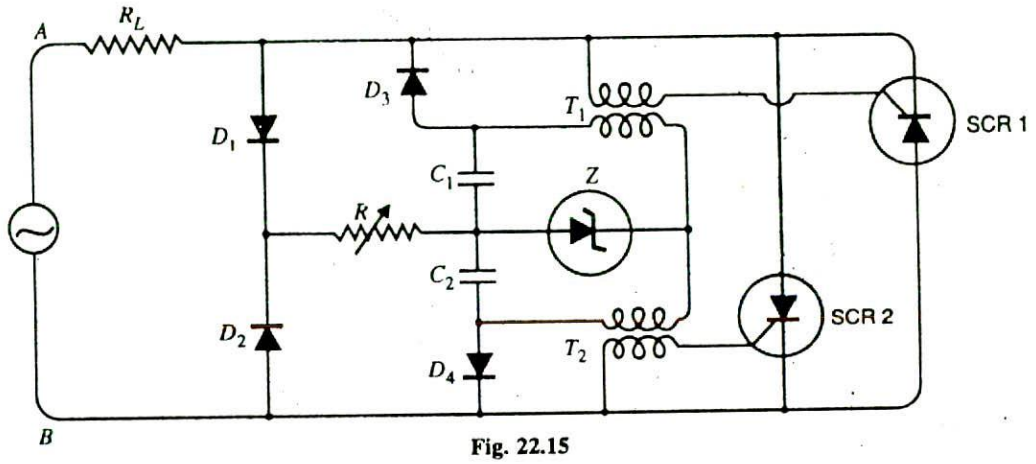


Fig. 22.15

(*ii*) **SCR for power control.** It is often necessary to control power delivered to some load such as the heating element of a furnace. Series resistances or potentiometers cannot be used because they waste power in high power circuits. Under such conditions, silicon controlled rectifiers are used which are capable of adjusting the transmitted power with little waste. Fig. 22.15 shows a common circuit for controlling power in the load R_L. During the positive half-cycle of a.c. supply, end A is positive and end B is negative. Therefore, capacitor C_2 is charged through $AD_1RC_2D_4B$. The charge on the capacitor C_2 depends upon the value of potentiometer R. When the capacitor C_2 is charged through a sufficient voltage, it discharges through the zener Z. This gives a pulse to the primary and hence secondary of transformer T_2. This turns on $SCR2$ which conducts currents through the load R_L. During negative half-cycle of supply, the capacitor C_1 is charged. It discharges through the zener and fires $SCR1$ which conducts current through the load.

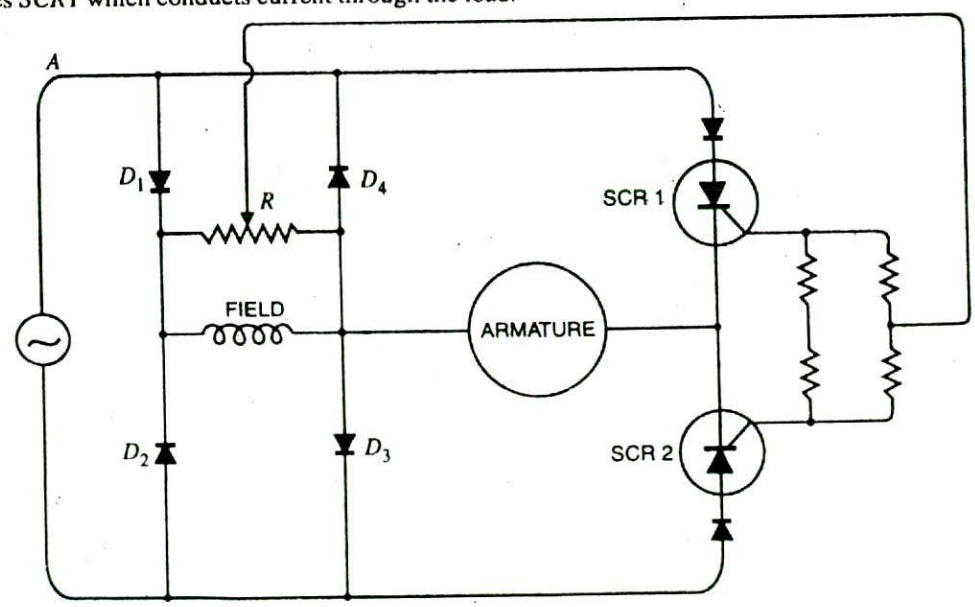


Fig. 22.16

The angle of conduction can be controlled by the potentiometer R. The greater the resistance of R, lesser is the voltage across C_1 or C_2 and hence smaller will be the time during which $SCR1$ and

*SCR*2 will conduct in a full cycle. In this way, we can control a large power of several kW in the load R_l with the help of a small potentiometer R.

(*iii*) **SCRs for speed control of d.c. shunt motor.** The conventional method of speed control of d.c. shunt motor is to change the field excitation. But change in field excitation changes the motor torque also. This drawback is overcome in *SCR* control as shown in Fig. 22.16. Diodes D_1, D_2, D_3 and D_4 form the bridge. This bridge circuit converts a.c. into d.c. and supplies it to the field winding of the motor. During the positive half-cycle of a.c. supply, *SCR*1 conducts because it gets gate current from bridge circuit as well as its anode is positive *w.r.t.* cathode. The armature winding of the motor gets current. The angle of conduction can be changed by varying the gate current. During the negative half cycle of a.c. supply, *SCR*2 provides current to the armature winding. In this way, the voltage fed to the motor armature and hence the speed can be controlled.

(*iv*) **Overlight detector.** Fig. 22.17 shows the use of *SCR* for overlight detection. The resistor R is a photo-resistor, a device whose resistance decreases with the increase in light intensity. When the light falling on R has normal intensity, the value of R is high enough and the voltage across R_1 is insufficient to trigger the *SCR*. However, when R is in strong light, its resistance decreases and the voltage drop across R_1 becomes high enough to trigger the *SCR*. Consequently, the buzzer sounds the alarm. It may be noted that even if the strong light disappears, the buzzer continues to sound the alarm. It is because once the *SCR* is fired, the gate loses all control.

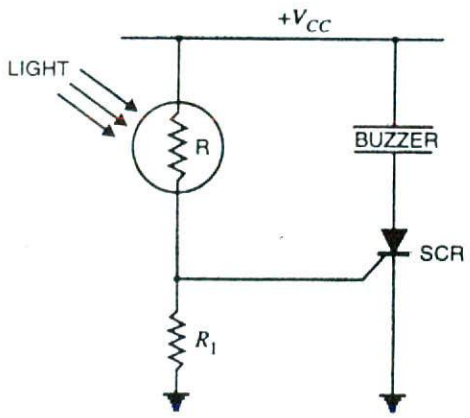


Fig. 22.17

22.12 Light-Activated SCR

The light-activated *SCR* (LASCR) is the light sensitive equivalent of the normal *SCR* and is shown in Fig. 22.18. As the name suggests, its state is controlled by the light falling on depletion layers. In a normal *SCR*, gate current turns on the device. In the *LASCR, instead of having the external gate current applied, light shinning on the device turns it ON. Just as a normal *SCR*, the LASCR will continue to conduct even if the light source is removed. The LASCRs find many applications including optical light controls, relays, phase control, motor control and a large number of computer applications.

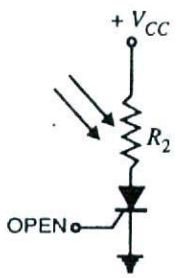


Fig. 22.18

Multiple-Choice Questions

1. An *SCR* has ..... *pn* junctions.
   (*i*) two (*ii*) three
   (*iii*) four (*iv*) none of the above
2. An *SCR* is a solid state equivalent of .....
   (*i*) triode (*ii*) pentode
   (*iii*) gas-filled triode (*iv*) tetrode
3. An *SCR* has ..... semiconductor layers.
   (*i*) two (*ii*) three
   (*iii*) four (*iv*) none of the above
4. An *SCR* has three terminals *viz.* .....
   (*i*) cathode, anode, gate
   (*ii*) anode, cathode, grid
   (*iii*) anode, cathode, drain
   (*iv*) none of the above

* For maximum sensitivity to light, the gate is left open.

5. An *SCR* behaves as a ..... switch.
   (*i*) unidirectional (*ii*) bidirectional
   (*iii*) mechanical (*iv*) none of the above
6. An *SCR* is sometimes called .....
   (*i*) triac
   (*ii*) diac
   (*iii*) unijunction transistor
   (*iv*) thyristor
7. An *SCR* is made of .....
   (*i*) germanium (*ii*) silicon
   (*iii*) carbon (*iv*) none of the above
8. In the normal operation of an *SCR*, anode is ..... *w.r.t.* cathode.
   (*i*) at zero potential
   (*ii*) negative
   (*iii*) positive
   (*iv*) none of the above
9. In normal operation of an *SCR*, gate is ..... *w.r.t.* cathode.
   (*i*) positive
   (*ii*) negative
   (*iii*) at zero potential
   (*iv*) none of the above
10. An *SCR* combines the features of .....
   (*i*) a rectifier and resistance
   (*ii*) a rectifier and transistor
   (*iii*) a rectifier and capacitor
   (*iv*) none of the above
11. The control element in an *SCR* is .....
   (*i*) cathode (*ii*) anode
   (*iii*) anode supply (*iv*) gate
12. The normal way to turn on an *SCR* is by .....
   (*i*) breakover voltage
   (*ii*) appropriate anode current
   (*iii*) appropriate gate current
   (*iv*) none of the above
13. An *SCR* is turned off by .....
   (*i*) reducing anode voltage to zero
   (*ii*) reducing gate voltage to zero
   (*iii*) reverse biasing the gate
   (*iv*) none of the above
14. An *SCR* is a ..... triggered device.
   (*i*) voltage
   (*ii*) current
   (*iii*) voltage as well as current
   (*iv*) none of the above
15. In an *SCR* circuit, the supply voltage is generally ..... that of breakover voltage.
   (*i*) equal to (*ii*) less than
   (*iii*) greater than (*iv*) none of the above
16. When an *SCR* is turned on, the voltage across it is about .....
   (*i*) zero (*ii*) 10 V
   (*iii*) 0.1 V (*iv*) 1V
17. An *SCR* is made of silicon and not germanium because silicon .....
   (*i*) is inexpensive
   (*ii*) is mechanically strong
   (*iii*) has small leakage current
   (*iv*) is tetravalent
18. An *SCR* is turned off when .....
   (*i*) anode current is reduced to zero
   (*ii*) gate voltage is reduced to zero
   (*iii*) gate is reverse biased
   (*iv*) none of the above
19. In an *SCR* circuit, the angle of conduction can be changed by .....
   (*i*) changing anode voltage
   (*ii*) changing gate voltage
   (*iii*) reverse biasing the gate
   (*iv*) none of the above
20. If firing angle in an *SCR* circuit is increased, the output .....
   (*i*) remains the same
   (*ii*) is increased
   (*iii*) is decreased
   (*iv*) none of the above
21. If gate current is increased, then anode-cathode voltage at which *SCR* closes .....
   (*i*) is decreased
   (*ii*) is increased
   (*iii*) remains the same
   (*iv*) none of the above
22. When *SCR* is OFF, the current in the circuit is .....
   (*i*) exactly zero
   (*ii*) small leakage current
   (*iii*) large leakage current
   (*iv*) none of the above

23. An *SCR* can exercise control over ..... of a.c. supply.
   (*i*) positive half-cycles only
   (*ii*) negative half-cycles only
   (*iii*) both positive and negative half-cycles
   (*iv*) positive or negative half-cycles
24. We can control a.c. power in a load by connecting .....
   (*i*) two *SCRs* in series
   (*ii*) two *SCRs* in parallel
   (*iii*) two *SCRs* in parallel opposition
   (*iv*) none of the above
25. When *SCR* starts conducting, then ..... loses all control.
   (*i*) gate (*ii*) cathode
   (*iii*) anode (*iv*) none of the above

Answers to Multiple-Choice Questions

1. (*ii*)	**2.** (*iii*)	**3.** (*iii*)	**4.** (*i*)	**5.** (*i*)
6. (*iv*)	**7.** (*ii*)	**8.** (*iii*)	**9.** (*i*)	**10.** (*ii*)
11. (*iv*)	**12.** (*iii*)	**13.** (*i*)	**14.** (*ii*)	**15.** (*ii*)
16. (*iv*)	**17.** (*iii*)	**18.** (*i*)	**19.** (*ii*)	**20.** (*iii*)
21. (*i*)	**22.** (*ii*)	**23.** (*iv*)	**24.** (*iii*)	**25.** (*i*)

Chapter Review Topics

1. Explain the construction and working of an *SCR*.
2. Draw the equivalent circuit of an *SCR* and explain its working from this equivalent circuit.
3. Explain the terms breakover voltage, holding current and forward current rating as used in connection with *SCR* analysis.
4. Draw the *V-I* characteristics of an *SCR*. What do you infer from them ?
5. Explain the action of an *SCR* as a switch. What are the advantages of *SCR* switch over a mechanical or electro-mechanical switch ?
6. Discuss some important applications of *SCR*.

Problems

1. An *SCR* has a breakover voltage of 450 V, a trigger current of 15 mA and holding current of 10 mA. What do you infer from it?
2. An *SCR* in a circuit is subjected to a 50 A current surge that lasts for 10 ms. Determine whether or not this surge will destroy the device. Given that circuit fusing rating of *SCR* is 90 A^2s.
   [will not be destroyed]
3. An *SCR* has a circuit fusing rating of 70 A^2s. The device is being used in a circuit where it could be subjected to a 100 A surge. Determine the limit on the duration of such a surge. **[7ms]**
4. An *SCR* has a circuit fusing rating of 60 A^2s. Determine the highest surge current value that *SCR* can withstand for a period of 20 ms. **[54.77A]**

Discussion Questions

1. How does *SCR* differ from an ordinary rectifier ?
2. Why is *SCR* always turned on by gate current ?
3. Why *SCR* cannot be used as a bidirectional switch ?
4. How does *SCR* control the power fed to the load ?
5. Why are *SCRs* usually used in a.c. circuits?
6. Name three thyristor devices.
7. Why is *SCR* turned on by high-frequency radiation ?

23

Power Electronics

Introduction

Since the 1950's there has been a great upsurge in the development, production and applications of semiconductor devices. Today there are well over 100 million semiconductor devices manufactured in a year. These figures alone indicate how important semiconductor devices have become to the electrical industry. In fact, the present day advancement in technology is largely attributed to the widespread use of semiconductor devices in the commercial and industrial fields.

One major field of application of semiconductor devices in the recent years has been to control large blocks of power flow in a system. This has led to the development of a new branch of engineering called power electronics. The purpose of this chapter is to acquaint the readers with some important switching devices much used in power electronics.

23.1 Power Electronics

The branch of electronics which deals with the control of power at 50 Hz (i.e. supply frequency) is known as **power electronics**.

There are many applications where it is desired to control (or regulate) the power fed to a load *e.g.* to change the speed of a fan or motor. So far we have been using electrical methods to exercise such a control. However, electrical methods do not permit a *fine control over the flow of power in a system. Moreover, there is a considerable wastage of power. In the recent years, such semiconductor devices have been developed which can exercise fine control over the flow of large blocks of power in a system. Such devices act as controlled switches and can perform the duties of controlled rectification, inversion and regulation of power in a load. The important semiconductor switching devices are :

(*i*) Silicon controlled rectifier (*SCR*) (*ii*) Triac

(*iii*) Diac (*iv*) Unijunction transistor (*UJT*)

The silicon controlled rectifier (*SCR*) has already been discussed in the previous chapter. Therefore, we shall deal with the other three switching devices in the following discussion.

23.2 The Triac

The major drawback of an *SCR* is that it can conduct current in one direction only. Therefore, an *SCR* can only control d.c. power or forward biased half-cycles of a.c. in a load. However, in an a.c. system, it is often desirable and necessary to exercise control over both positive and negative half-

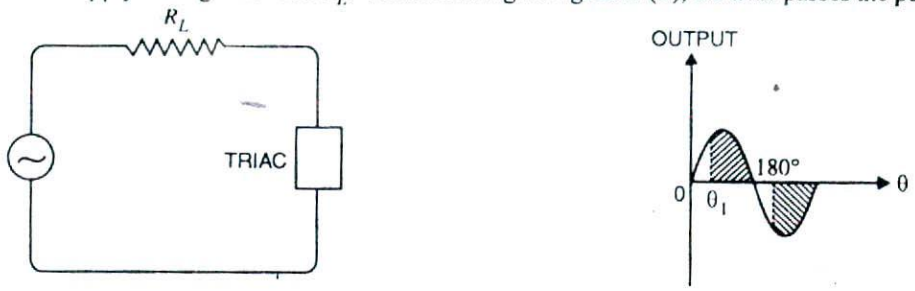
* For example, the speed of a ceiling fan can be changed in four to five steps by electrical method.

cycles. For this purpose, a semiconductor device called *triac* is used.

A **triac** *is a three terminal semiconductor switching device which can control alternating current in a load.*

Triac is an abbreviation for *triode a.c.* switch. 'Tri'– indicates that the device has three terminals and 'ac' means that the device controls alternating current or can conduct current in either direction.

The key function of a triac may be understood by referring to the simplified Fig. 23.1. The *control circuit of triac can be adjusted to pass the desired portions of positive and negative half-cycle of a.c. supply through the load R_L. Thus referring to Fig. 23.1 (*ii*), the triac passes the positive



(*i*) (*ii*)

Fig. 23.1

half-cycle of the supply from θ_1 to 180° *i.e.* the shaded portion of positive half-cycle. Similarly, the shaded portion of negative half-cycle will pass through the load. In this way, the alternating current and hence a.c. power flowing through the load can be controlled.

Since a triac can control conduction of both positive and negative half-cycles of a.c. supply, it is sometimes called a bidirectional semi-conductor triode switch. The above action of a triac is certainly not a rectifying action (as in an ****SCR*) so that the triac makes no mention of rectification in its name.

23.3 Triac Construction

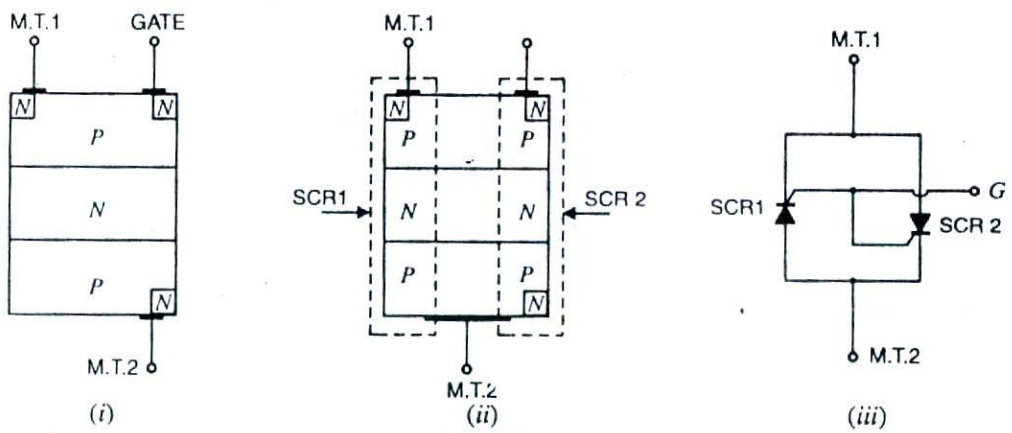


Fig. 23.2

* Although it appears that 'triac' has two terminals, there is also third terminal connected to the control circuit.

** SCR is a controlled rectifier. It is a unidirectional switch and can conduct only in one direction. Therefore, it can control only one half-cycle (positive or negative) of a.c. apply

A triac is a bidirectional switch having three terminals. Fig. 23.2 (*i*) shows the basic structure of a triac. Referring to Fig. 23.2 (*ii*), the basic structure can be shown to be consisting of two halves. Each half may be considered as a *pnpn SCR* with the gates commoned as shown in Fig. 23.2 (*iii*). The equivalent circuit of triac shown in Fig. 23.2 (*iii*) indicates that a triac corresponds to two separate *SCRs* connected in inverse parallel (*i.e.* anode of each connected to the cathode of the other) with gates commoned.

Fig. 23.3 shows the symbol of a triac. The control terminal as with *SCR*, is called the gate *G*. The other two terminals are *MT*1 and *MT*2 respectively called 'main terminal 1' and 'main terminal 2'. With proper gate current, the triac can be made to conduct when *MT*2 is either positive or negative *w.r.t. MT*1.

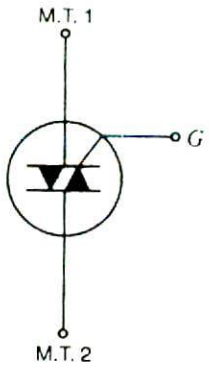


Fig. 23.3

It can be seen that even symbol of triac indicates that it can conduct for either polarity of voltage across the main terminals. The gate provides control over conduction in either direction.

Triacs are commercially available to handle maximum r.m.s. currents from about 0.5 A upto 25 A, although special triacs for upto about 1000 A have been developed. As the current handling capacity increases, so does the semi-conductor element size and the containing package.

23.4 Triac Operation

Fig. 23.4 shows the simple triac circuit. The a.c. supply to be controlled is connected across the main terminals of triac through a load resistance R_L. The gate circuit consists of battery, a current limiting resistor R and a switch S. The circuit action is as follows :

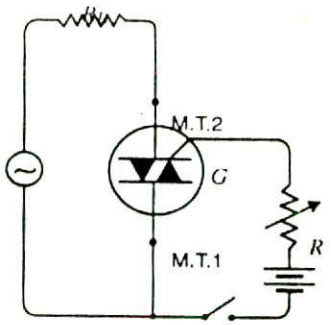


Fig. 23.4

(*i*) With switch S open, there will be no gate current and the triac is cut off. Even with no gate current, the triac can be turned on provided the supply voltage becomes equal to the breakover voltage of triac. However, the normal way to turn on a triac is by introducing a proper gate current.

(*ii*) When switch S is closed, the gate current starts flowing in the gate circuit. In a similar manner to *SCR*, the breakover voltage of the triac can be varied by making proper gate current to flow. With a few milliamperes introduced at the gate, the triac will start conducting whether terminal *MT*2 is positive or negative *w.r.t. MT*1.

(*iii*) If terminal *MT*2 is positive *w.r.t. MT*1, the triac turns on and the conventional current will flow from *MT*2 to *MT*1. If the terminal *MT*2 is negative *w.r.t. MT*1, the triac is again turned on but this time the conventional current flows from *MT*1 to *MT*2.

The above action of triac reveals that it can act as an *a.c.* contactor to switch on or off alternating current to a load. The additional advantage of triac is that by adjusting the gate current to a proper value, any portion of both positive and negative half-cycles of *a.c.* supply can be made to flow through the load. This permits to adjust the transfer of a.c. power from the source to the load.

23.5 Triac Characteristics

Fig. 23.5 shows the *V-I* characteristics of a triac. Because the triac essentially consists of two *SCRs* of opposite orientation fabricated in the same crystal, its operating characteristics in the first and third quadrants are the same except for the direction of applied voltage and current flow. The following points may be noted from the triac characteristics :

(*i*) The *V-I* characteristics for triac in the Ist and IIIrd quadrants are essentially identical to those of an *SCR* in the Ist quadrant.

(*ii*) The triac can be operated with either positive or negative *gate* control voltage but in *normal operation usually the gate voltage is positive in quadrant I and negative in quadrant III.

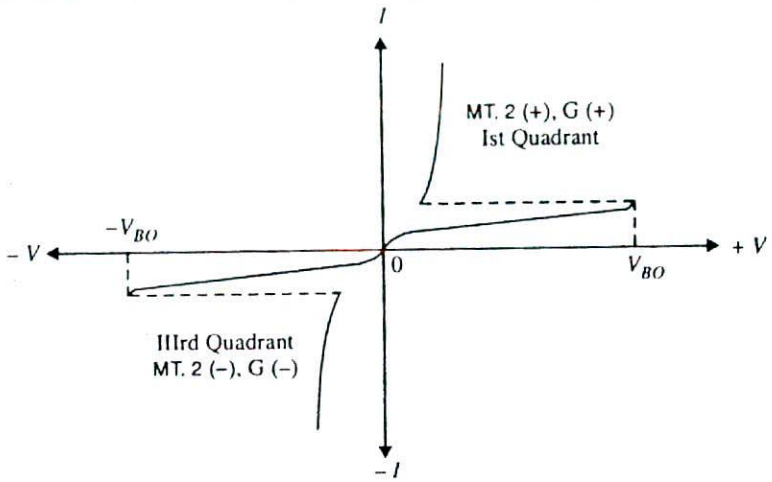


Fig. 23.5

(*iii*) The supply voltage at which the triac is turned *ON* depends upon the gate current. The greater the gate current, the smaller the supply voltage at which the triac is turned on. This permits to use a triac to control a.c. power in a load from zero to full power in a smooth and continuous manner with no loss in the controlling device.

23.6 Applications of Triac

As low gate currents and voltages can be used to control large load currents and voltages, therefore, triac is often used as an electronic on/off switch controlled by a low-current mechanical switch.

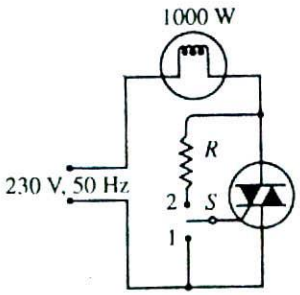


Fig. 23.6

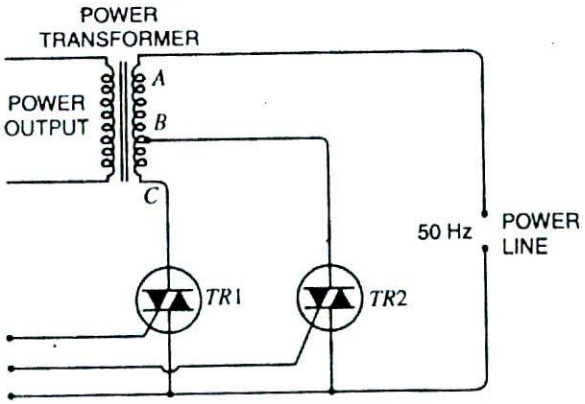


Fig. 23.7

(*i*) **As a high-power lamp switch.** Fig. 23.6 shows the use of a triac as an *a.c.* on/off switch.

*With this arrangement, less charge is required to turn on the triac.

When switch S is thrown to position 1, the triac is cut off and the output power of lamp is zero. But as the switch is thrown to position 2, a small gate current (a few mA) flowing through the gate turns the triac on. Consequently, the lamp is switched on to give full output of 1000 watts.

(*ii*) **Electronic change over of transformer taps.** Fig. 23.7 shows the circuit of electronic change over of power transformer input taps. Two triacs *TR*1 and *TR*2 are used for the purpose. When triac *TR*1 is turned on and *TR*2 is turned off, the line input is connected across the full transformer primary *AC*. However, if it is desired to change the tapping so that input appears across part *AB* of the primary, then *TR*2 is turned on and *TR*1 is turned off. The gate control signals are so controlled that both triacs are never switched on together. This avoids a dangerous short circuit on the section *BC* of the primary.

23.7 The Diac

A **diac** *is a two terminal, three layer bidirectional device which can be switched from its OFF state to ON state for either polarity of applied voltage.*

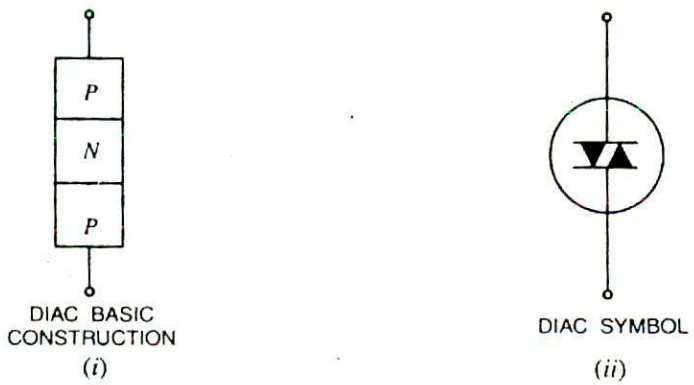


Fig. 23.8

The diac can be constructed in either *npn* or *pnp* form. Fig. 23.8 (*i*) shows the basic structure of a diac in *pnp* form. The two leads are connected to *p*-regions of silicon separated by an *n*-region. The structure of diac is very much similar to that of a transistor. However, there are several imporant differences:

(*i*) there is no terminal attached to the base layer.

(*ii*) the three regions are nearly identical in size.

(*iii*) the doping concentrations are identical (unlike a bipolar transistor) to give the device symmetrical properties.

Fig. 23.8 (*ii*) shows the symbol of a diac.

Operation. When a positive or negative voltage is applied across the terminals of a diac, only a small leakage current I_{BO} will flow through the device. As the applied voltage is increased, the leakage current will continue to flow until the voltage reaches the breakover voltage V_{BO}. At this point, avalanche breakdown of the reverse-biased junction occurs and the device exhibits negative resistance *i.e.* current through the device increases with the decreasing values of applied voltage. The voltage across the device then drops to 'breakback' voltage V_w.

Fig. 23.9 shows the *V-I* characteristics of a diac. For applied positive voltage less than $+ V_{BO}$ and negative voltage less than $- V_{BO}$, a small leakage current ($\pm I_{BO}$) flows through the device. Under such conditions, the diac blocks the flow of current and effectively behaves as an open circuit. The

voltage $+V_{BO}$ and $-V_{BO}$ are the breakdown voltages and usually have a range of 30 to 50 volts.

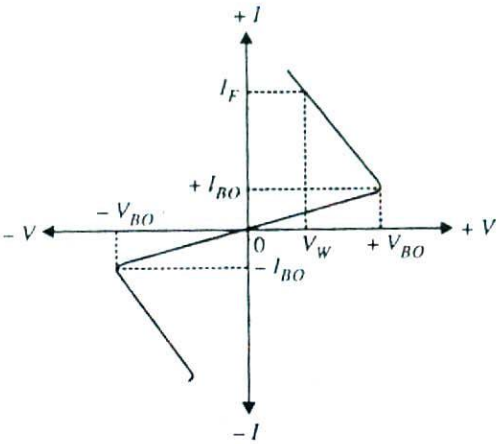


Fig. 23.9

When the positive or negative applied voltage is equal to or greater than the breakdown voltage, diac begins to conduct and the voltage drop across it becomes a few volts. Conduction then continues until the device current drops below its holding current. Note that the breakover voltage and holding current values are identical for the forward and reverse regions of operation.

Diacs are used primarily for triggering of triacs in adjustable phase control of a.c. mains power. Some of the circuit applications of diac are (*i*) light dimming (*ii*) heat control and (*iii*) universal motor speed control.

23.8 Applications of Diac

Although a triac may be fired into the conducting state by a simple resistive triggering circuit, more reliable and faster turn-on may be had if a switching device is used in series with the gate. One of the switching devices that can trigger a triac is the diac. This is illustrated in the following applications.

(*i*) **Lamp dimmer.** Fig. 23.10 shows a typical circuit that may be used for smooth control of a.c. power fed to a lamp. This permits to control the light output from the lamp. The basic control is by an *RC* variable gate voltage arrangement. The series $R_4 - C_1$ circuit across the triac is designed to limit the rate of voltage rise across the device during switch off.

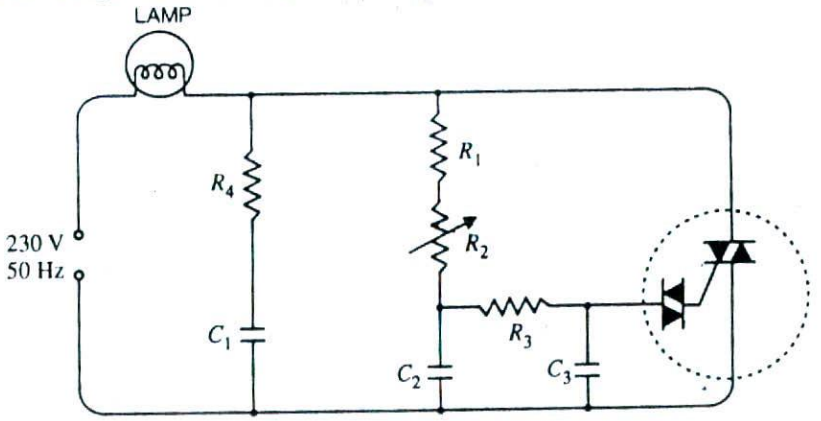


Fig. 23.10

The circuit action is as follows. As the input voltage increases positively or negatively, C_1 and C_2 charge at a rate determined primarily by R_2. When the voltage across C_3 exceeds the breakover voltage of the diac, the diac is fired into the conducting state. The capacitor C_3 discharges through the conducting diac into the gate of the triac. Hence, the triac is turned on to pass the a.c. power to the lamp. By adjusting the value of R_2, the rate of charge of capacitors and hence the point at which triac will trigger on the positive or negative half-cycle of input voltage can be controlled. Fig. 23.11 shows the waveforms of supply voltage and load voltage in the diac-triac control circuit

(*i*) (*ii*)

Fig. 23.11

The firing of triac can be controlled upto a maximum of 180°. In this way, we can provide a continuous control of load voltage from practically zero to full *r.m.s.* value.

(*ii*) **Heat control.** Fig. 23.12 shows a typical diac-triac circuit that may be used for the smooth control of a.c. power in a heater. This is similar to the circuit shown in Fig. 23.10. The capacitor C_1 in series with choke L across the triac helps to slow-up the voltage rise across the device during switch-off. The resistor R_4 in parallel with the diac ensures smooth control at all positions of variable resistance R_2.

The circuit action is as follows. As the input voltage increases positively or negatively, C_1 and C_2 charge at a rate determined primarily by R_2. When the voltage across C_3 exceeds the breakover voltage of the diac, the diac conducts. The capacitor C_3 discharges through the conducting diac into the gate of the triac. This turns on the triac and hence a.c. power to the heater. By adjusting the value of R_2, any portion of positive and negative half-cycles of the supply voltage can be passed through the heater. This permits a smooth control of the heat output from the heater.

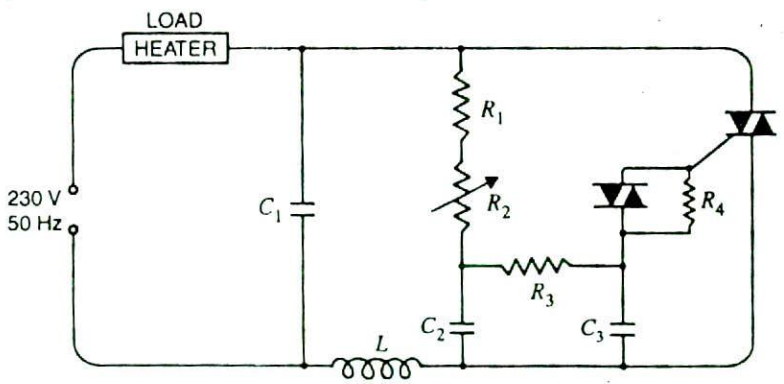


Fig. 23.12

23.9 Unijunction Transistor (UJT)

A unijunction transistor (abbreviated as UJT) is a three terminal semiconductor switching device. This device has a unique characteristic that when it is triggered, the emitter current increases

regeneratively until it is limited by emitter power supply. Due to this characteristic, the unijunction transistor can be employed in a variety of applications *e.g.*, switching, pulse generator, saw-tooth generator etc.

Construction. Fig. 23.13 (*i*) shows the basic *structure of a unijunction transistor. It consists of an *n*-type silicon bar with an electrical connection on each end. The leads to these connections are

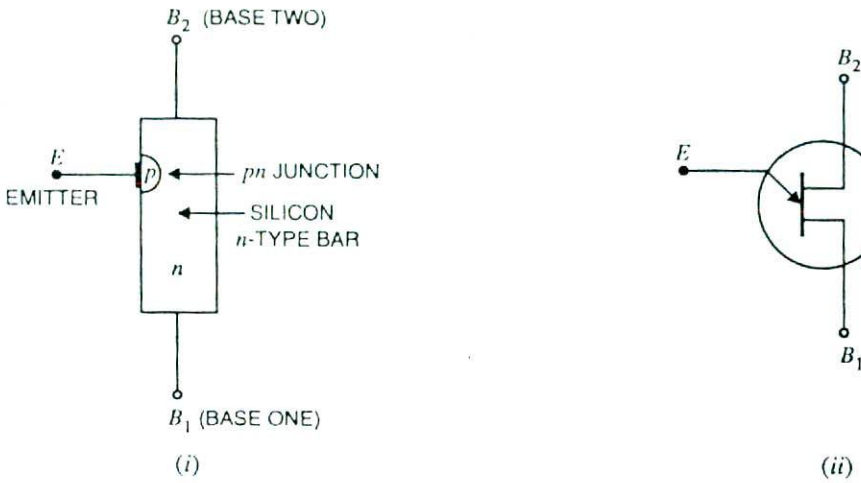


Fig. 23.13

called base leads *base-one* B_1 and *base two* B_2. Part way along the bar between the two bases, nearer to B_2 than B_1, a *pn* junction is formed between a *p*-type emitter and the bar. The lead to this junction is called the *emitter* lead *E*. Fig. 23.13 (*ii*) shows the symbol of unijunction transistor. Note that emitter is shown closer to B_2 than B_1. The following points are worth noting :

(*i*) Since the device has one *pn* junction and three leads, it is **commonly called a unijunction transistor (*uni* means single).

(*ii*) With only one *pn*-junction, the device is really a form of diode. Because the two base terminals are taken from one section of the diode, this device is also called *double-based diode.*

(*iii*) The emitter is heavily doped having many holes. The *n* region, however, is lightly doped. For this reason, the resistance between the base terminals is very high (5 to 10 kΩ) when emitter lead is open.

Operation. Fig. 23.14 shows the basic circuit operation of a unijunction transistor. The device has normally B_2 positive *w.r.t.* B_1.

(*i*) If voltage V_{BB} is applied between B_2 and B_1 with emitter open [See Fig. 23.14 (*i*)], a voltage gradient is established along the *n*-type bar. Since the emitter is located nearer to B_2, more than †half of V_{BB} appears between the emitter and B_1. The voltage V_1 between emitter and B_1 establishes a reverse bias on the *pn* junction and the emitter current is cut off. Of course, a small leakage current flows from B_2 to emitter due to minority carriers.

---

* Note that structure of *UJT* is very much similar to that of the *n*-channel *JFET*. The only difference in the two components is that *p*-type (gate) material of the *JFET surrounds* the *n*-type (channel) material.

** In packaged form, a UJT looks very much like a small signal transistor. As a UJT has only one *pn* junction, therefore, naming it a 'transistor' is really a misnomer.

† The *n*-type silicon bar has a high resistance. The resistance between emitter and B_1 is greater than between B_2 and emitter. It is because emitter is nearer to B_2 than B_1.

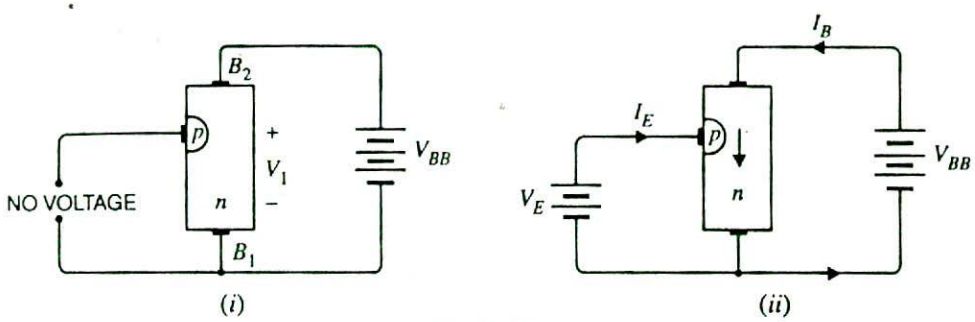


Fig. 23.14

(*ii*) If a positive voltage is applied at the emitter [See Fig. 23.14 (*ii*)], the *pn* junction will remain reverse biased so long as the input voltage is less than V_1. If the input voltage to the emitter exceeds V_1, the *pn* junction becomes * forward biased. Under these conditions, holes are injected from *p*-type material into the *n*-type bar. These holes are repelled by positive B_2 terminal and they are attracted towards B_1 terminal of the bar. This accumulation of holes in the emitter to B_1 region results in the decrease of resistance in this section of the bar. The result is that internal voltage drop from emitter to B_1 is decreased and hence the emitter current I_E increases. As more holes are injected, a condition of saturation will eventually be reached. At this point, the emitter current is limited by emitter power supply only. The device is now in the ON state.

(*iii*) If a negative pulse is applied to the emitter, the *pn* junction is reverse biased and the emitter current is cut off. The device is then said to be in the OFF state.

23.10 Equivalent Circuit of a UJT

Fig. 23.15 shows the equivalent circuit of a UJT. The resistance of the silicon bar is called the inter-base resistance R_{BB}. The inter-base resistance is represented by two resistors in series *viz.*

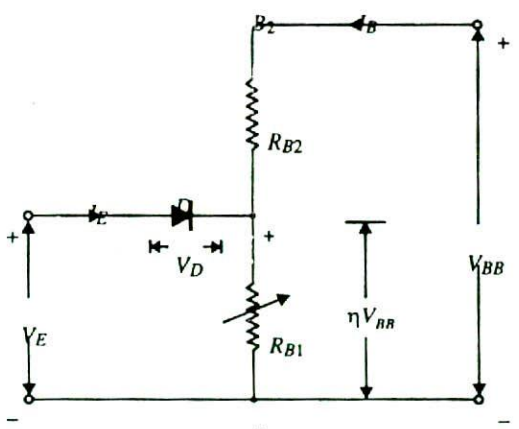


Fig. 23.15

(*a*) R_{B2} is the resistance of silicon bar between B_2 and the point at which the emitter junction lies.

---

* The main operational difference between the *FET* and the *UJT* is that the *FET* is normally operated with the gate junction reverse biased whereas the useful behaviour of the *UJT* occurs when the emitter is forward biased.

(*b*) R_{B1} is the resistance of the bar between B_1 and emitter junction. This resistance is shown variable because its value depends upon the bias voltage across the *pn* junction.

The *pn* junction is represented in the emitter by a diode *D*.

The circuit action of a *UJT* can be explained more clearly from its equivalent circuit.

(*i*) With no voltage applied to the *UJT*, the inter-base resistance is given by ;

$$R_{BB} = R_{B1} + R_{B2}$$

The value of R_{BB} generally lies between 4 kΩ and 10 kΩ.

(*ii*) If a voltage V_{BB} is applied between the bases with emitter open, the voltage will divide up across R_{B1} and R_{B2}.

$$\text{Voltage across } R_{B1},\ V_1 = \frac{R_{B1}}{R_{B1} + R_{B2}} V_{BB}$$

or

$$V_1/V_{BB} = \frac{R_{B1}}{R_{B1} + R_{B2}}$$

The ratio V_1/V_{BB} is called *intrinsic stand-off ratio* and is represented by Greek letter η.

$$\text{Obviously, } \eta = \frac{R_{B1}}{R_{B1} + R_{B2}}$$

The value of η usually lies between 0.51 and 0.82.

$$\therefore \quad \text{Voltage across } R_{B1} = \eta\, V_{BB}$$

The voltage $\eta\, V_{BB}$ appearing across R_{B1} reverse biases the diode. Therefore, the emitter current is zero.

(*iii*) If now a progressively rising positive voltage is applied to the emitter, the diode will become forward biased when input voltage exceeds $\eta\, V_{BB}$ by V_D, the forward voltage drop across the silicon diode *i.e.*

$$V_P = \eta\, V_{BB} + V_D$$

where

V_P = 'peak point voltage'

V_D = forward voltage drop across silicon diode (≃ 0.7 V)

When the diode *D* starts conducting, holes are injected from *p*-type material to the *n*-type bar. These holes are swept down towards the terminal B_1. This decreases the resistance between emitter and B_1 (indicated by variable resistance symbol for R_{B1}) and hence the internal drop from emitter to B_1. The emitter current now increases regeneratively until it is limited by the emitter power supply.

Conclusion. The above discussion leads to the conclusion that when input positive voltage to the emitter is less than peak-point voltage V_P, the *pn*-junction remains reverse biased and the emitter current is practically zero. However, when the input voltage exceeds V_P, R_{B1} falls from several thousand ohms to a small value. The diode is now forward biased and the emitter current quickly reaches to a saturation value limited by R_{B1} (about 20 Ω) and forward resistance of *pn*-junction (about 200 Ω).

23.11 Characteristics of UJT

Fig. 23.16 shows the curve between emitter voltage (V_E) and emitter current (I_E) of a *UJT* at a given voltage V_{BB} between the bases. This is known as the emitter characteristic of *UJT*. The following points may be noted from the characteristics :

(*i*) Initially, in the cut-off region, as V_E increases from zero, slight leakage current flows from terminal B_2 to the emitter. This current is due to the minority carriers in the reverse biased diode.

(*ii*) Above a certain value of V_E, forward I_E begins to flow, increasing until the peak voltage V_P and current I_P are reached at point *P*.

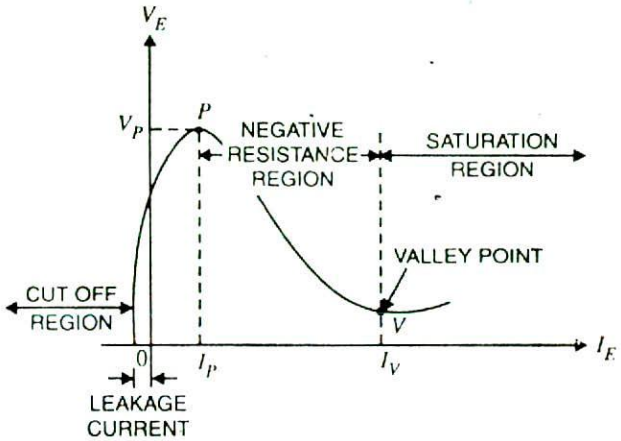


Fig. 23.16

(*iii*) After the peak point P, an attempt to increase V_E is followed by a sudden increase in emitter current I_E with a corresponding decrease in V_E. This is a *negative resistance* portion of the curve because with increase in I_E, V_E decreases. The device, therefore, has a negative resistance region which is stable enough to be used with a great deal of reliability in many areas e.g., trigger circuits, sawtooth generators, timing circuits.

(*iv*) The negative portion of the curve lasts until the valley point V is reached with valley-point voltage V_V and valley-point current I_V. After the valley point, the device is driven to saturation.

Fig. 23.17 shows the typical family of V_E/I_E characteristics of a *UJT* at different voltages between the bases. It is clear that peak-point voltage ($= \eta V_{BB} + V_D$) falls steadily with reducing V_{BB} and so does the valley point voltage V_V. The difference $V_P - V_V$ is a measure of the switching efficiency of *UJT* and can be seen to fall off as V_{BB} decreases. For a general purpose *UJT*, the peak-point current is of the order of 1 μA at $V_{BB} = 20$ V with a valley-point voltage of about 2.5 V at 6 mA.

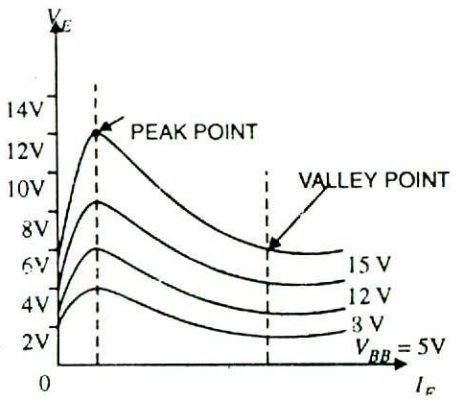


Fig. 23.17

Example 23.1. *The intrinsic stand-off ratio for a UJT is determined to be 0.6. If the inter-base resistance is 10 kΩ, what are the values of R_{B1} and R_{B2}?*

Solution. $R_{BB} = 10\ \text{k}\Omega, \quad \eta = 0.6$

Now $R_{BB} = R_{B1} + R_{B2}$

or $10 = R_{B1} + R_{B2}$

Also $$\eta = \frac{R_{B1}}{R_{B1} + R_{B2}}$$

or $$0.6 = \frac{R_{B1}}{10} \qquad (\because R_{B1} + R_{B2} = 10\ \text{k}\Omega)$$

$\therefore$ $R_{B1} = 10 \times 0.6 = \mathbf{6\ k\Omega}$

and $R_{B2} = 10 - 6 = \mathbf{4\ k\Omega}$

Example 23.2. *A unijunction transistor has 10 V between the bases. If the intrinsic stand off ratio is 0.65, find the value of stand off voltage. What will be the peak-point voltage if the forward voltage drop in the pn junction is 0.7 V ?*

Solution. $V_{BB} = 10\text{ V};\quad \eta = 0.65;\quad V_D = 0.7\text{ V}$

Stand off voltage $= \eta V_{BB} = 0.65 \times 10 = \mathbf{6.5\ V}$

Peak-point voltage, $V_P = \eta V_{BB} + V_D = 6.5 + 0.7 = \mathbf{7.2\ V}$

23.12 Advantages of UJT

The *UJT* was introduced in 1948 but did not become commercially available until 1952. Since then, the device has achieved great popularity due to the following reasons :

(*i*) It is a low cost device.

(*ii*) It has excellent characteristics.

(*iii*) It is a low-power absorbing device under normal operating conditions.

Due to above reasons, this device is being used in a variety of applications. A few include oscillators, trigger circuits, saw-tooth generators, bistable network etc.

23.13 Applications of UJT

Unijunction transistors are used extensively in oscillator, pulse and voltage sensing circuits. Some of the important applications of *UJT* are discussed below :

(*i*) **UJT relaxation oscillator.** Fig. 23.18 shows *UJT* relaxation oscillator where the discharging of a capacitor through *UJT* can develop a saw-tooth output as shown.

When battery V_{BB} is turned on, the capacitor C charges through resistor R_1. During the charging period, the voltage across the capacitor rises in an exponential manner until it reaches the peak - point voltage. At this instant of time, the *UJT* switches to its low resistance conducting mode and the capacitor is discharged between E and B_1. As the capacitor voltage flys back to zero, the emitter ceases to conduct and the *UJT* is switched off. The next cycle then begins, allowing the capacitor C to charge again. The frequency of the output saw-tooth wave can be varied by changing the value of R_1 since this controls the time constant R_1C of the capacitor charging circuit.

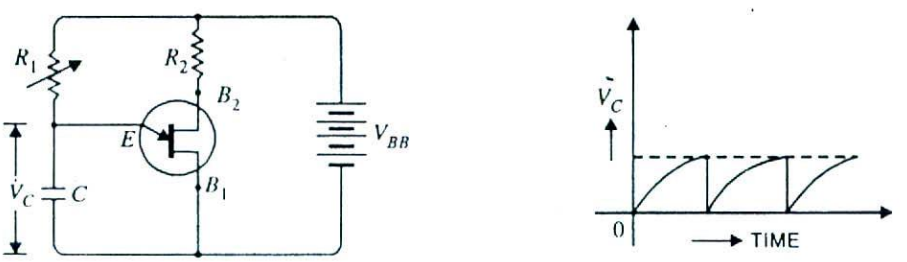


Fig. 23.18

The time period and hence the frequency of the saw-tooth wave can be calculated as follows. Assuming that the capacitor is initially uncharged, the voltage V_C across the capacitor prior to breakdown is given by ;

$$V_C = V_{BB}(1 - e^{-t/R_1C})$$

where R_1C = charging time constant of resistor-capacitor circuit

t = time from the commencement of waveform.

The discharge of the capacitor occurs when V_c is equal to the *peak-point voltage ηV_{BB} *i.e.*

$$\eta V_{BB} = V_{BB}(1 - e^{-t/R_1C})$$

or $$\eta = 1 - e^{-t/R_1C}$$

or $$e^{-t/R_1C} = 1 - \eta$$

or $$t = R_1 C \log_e \frac{1}{1-\eta}$$

$\therefore$ Time period, $$t = 2.3\, R_1 C \log_{10} \frac{1}{1-\eta}$$

Frequency of saw-tooth wave, $$f = \frac{1}{t \text{ in seconds}} \text{ Hz}$$

(*ii*) **Overvoltage detector.** Fig. 23.19 shows a simple d.c. over-voltage indicator. A warning pilot - lamp L is connected between the emitter and B_1 circuit. So long as the input voltage is less than the peak-point voltage (V_p) of the *UJT*, the device remains switched off. However, when the input voltage exceeds V_p, the *UJT* is switched on and the capacitor discharges through the low resistance path between terminals E and B_1. The current flowing in the pilot lamp L lights it, thereby indicating the overvoltage in the circuit.

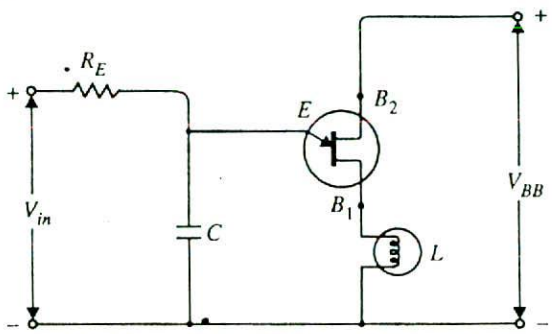


Fig. 23.19

Multiple-Choice Questions

1. A triac has three terminals *viz.* .....
   (*i*) drain, source, gate
   (*ii*) two main terminal and a gate terminal
   (*iii*) cathode, anode, gate
   (*iv*) none of the above
2. A triac is equivalent to two *SCRs* .....
   (*i*) in parallel
   (*ii*) in series
   (*iii*) in inverse-parallel
   (*iv*) none of the above
3. A triac is a ..... switch.
   (*i*) bidirectional
   (*ii*) undirectional
   (*iii*) mechanical
   (*iv*) none of the above
4. The *V-I* characteristics for a triac in the first and third quadrants are essentially identical to those of ..... in the first quadrant.
   (*i*) transistor (*ii*) *SCR*
   (*iii*) *UJT* (*iv*) none of the above
5. A triac can pass a portion of ..... half-cycle through the load.
   (*i*) only positive
   (*ii*) only negative

* Actually, peak point voltage, $V_p = \eta V_{BB} + V_D$. As V_D, the forward voltage drop across emitter diode is generally small, it can be neglected with reasonable accuracy.

$\therefore$ $$V_p = \eta V_{BB}$$

(*iii*) both positive and negative
(*iv*) none of the above

6. A diac has ..... terminals.
(*i*) two (*ii*) three
(*iii*) four (*iv*) none of the above

7. A triac has ..... semiconductor layers.
(*i*) two (*ii*) three
(*iii*) four (*iv*) five

8. A diac has ..... *pn* junctions.
(*i*) four (*ii*) two
(*iii*) three (*iv*) none of the above

9. The device that does not have the gate terminal is .....
(*i*) triac (*ii*) FET
(*iii*) SCR (*iv*) diac

10. A diac has ..... semiconductor layers.
(*i*) three (*ii*) two
(*iii*) four (*iv*) none of the above

11. A *UJT* has .....
(*i*) two *pn* junctions
(*ii*) one *pn* junction
(*iii*) three *pn* junctions
(*iv*) none of the above

12. The normal way to turn on a diac is by .....
(*i*) gate current
(*ii*) gate voltage
(*iii*) breakover voltage
(*iv*) none of the above

13. A diac is ..... switch.
(*i*) an a.c. (*ii*) a d.c.
(*iii*) a mechanical (*iv*) none of the above

14. In a *UJT*, the *p*-type emitter is ..... doped.
(*i*) lightly (*ii*) heavily
(*iii*) moderately (*iv*) none of the above

15. Power electronics essentially deals with control of a.c. power at .....
(*i*) frequencies above 20 kHz
(*ii*) frequencies above 1000 kHz
(*iii*) frequencies less than 10 Hz
(*iv*) 50 Hz frequency

16. When the emitter terminal of a *UJT* is open, the resistance between the base terminals is generally .....
(*i*) high (*ii*) low
(*iii*) extremely low (*iv*) none of the above

17. When a *UJT* is turned ON, the resistance between emitter terminal and lower base terminal .....
(*i*) remains the same
(*ii*) is decreased
(*iii*) is increased
(*iv*) none of the above

18. To turn on *UJT*, the forward bias on the emitter diode should be ..... the peak point voltage.
(*i*) less than (*ii*) equal to
(*iii*) more than (*iv*) none of the above

19. A *UJT* is sometimes called ..... diode.
(*i*) low resistance (*ii*) high resistance
(*iii*) single-base (*iv*) double-based

20. When the temperature increases, the inter-base resistance (R_{BB}) of a UJT .....
(*i*) increases
(*ii*) decreases
(*iii*) remains the same
(*iv*) none of the above

21. The intrinsic stand off ratio (η) of a *UJT* is given by .....
(*i*) $R_{B1} + R_{B2}$ (*ii*) $\frac{R_{B1} + R_{B2}}{R_{B1}}$
(*iii*) $\frac{R_{B1}}{R_{B1} + R_{B2}}$ (*iv*) $\frac{R_{B1} + R_{B2}}{R_{B2}}$

22. When the temperature increases, the intrinsic stand off ratio .....
(*i*) increases
(*ii*) decreases
(*iii*) essentially remains the same
(*iv*) none of the above

23. Between the peak point and the valley point of *UJT* emitter characteristics we have ..... region.
(*i*) saturation (*ii*) negative resistance

(*iii*) cut-off (*iv*) none of the above

24. A diac is turned on by .....
    (*i*) breakover voltage
    (*ii*) gate voltage
    (*iii*) gate current
    (*iv*) none of the above
25. The device that exhibits negative resistance region is .....
    (*i*) diac (*ii*) triac
    (*iii*) transistor (*iv*) *UJT*
26. The *UJT* may be used as .....
    (*i*) an amplifier
    (*ii*) a sawtooth generator
    (*iii*) a rectifier
    (*iv*) none of the above
27. A diac is simply .....
    (*i*) a single junction device
    (*ii*) a three junction device
    (*iii*) a triac without gate terminal
    (*iv*) none of the above
28. After peak point, the *UJT* operates in the ..... region.
    (*i*) cut-off
    (*ii*) saturation
    (*iii*) negative resistance
    (*iv*) none of the above
29. Which of the following is *not* a characteristic of *UJT*?
    (*i*) intrinsic stand off ratio
    (*ii*) negative resistance
    (*iii*) peak-point voltage
    (*iv*) bilateral conduction
30. The triac is .....
    (*i*) like a bidirectional *SCR*
    (*ii*) a four-terminal device
    (*iii*) not a thyristor
    (*iv*) answers (*i*) and (*ii*)

Answers to Multiple-Choice Questions

1. (*ii*)	**2.** (*iii*)	**3.** (*i*)	**4.** (*ii*)	**5.** (*iii*)
6. (*i*)	**7.** (*iii*)	**8.** (*ii*)	**9.** (*iv*)	**10.** (*i*)
11. (*ii*)	**12.** (*iii*)	**13.** (*i*)	**14.** (*ii*)	**15.** (*iv*)
16. (*i*)	**17.** (*ii*)	**18.** (*iii*)	**19.** (*iv*)	**20.** (*i*)
21. (*iii*)	**22.** (*iii*)	**23.** (*ii*)	**24.** (*i*)	**25.** (*iv*)
26. (*ii*)	**27.** (*iii*)	**28.** (*iii*)	**29.** (*iv*)	**30.** (*i*)

Chapter Review Topics

1. Discuss the importance of power electronics.
2. Explain the construction and working of a triac.
3. Sketch the *V-I* characteristics of a triac. What do you infer from them ?
4. Describe some important applications of a triac.
5. Explain the construction and working of a diac.
6. Discuss the applications of a diac.
7. Explain the construction and working of a *UJT*.
8. Draw the equivalent circuit of a *UJT* and discuss its working from the circuit.
9. Describe some important applications of a *UJT*.
10. Write short notes on the following :
    (*i*) *UJT* relaxation oscillator
    (*ii*) Triac as an a.c. switch
    (*iii*) Diac as a triggering device

Problems

1. The intrinsic stand off ratio for a *UJT* is determined to be 0.6. If the inter-base resistance is 5 kΩ, what are the values of R_{B1} and R_{B2} ? **[R_{B1} = 3 kΩ ; R_{B2} = 2 kΩ]**
2. A unijunction transistor has 18 V between the bases. If the intrinsic stand off ratio is 0.8, find the value of stand off voltage. What will be the peak point voltage if the forward voltage drop in the *pn* junction is 0.7 V ? **[14.4 V ; 15.1 V]**
3. In a unijunction transistor, $\eta = 0.8$, $V_p = 10.3$ V and $R_{B2} = 5$ kΩ. Determine R_{B1} and V_{BB}. **[20 kΩ ; 12 V]**
4. The instrinsic stand-off ratio for a *UJT* is 0.75 and $V_{BB} = 12$ V. If the forward drop in the *pn*-junction is 0.7 V, find the peak point voltage. **[9.7 V]**
5. A unijunction transistor has 12 V between the bases. If the intrinsic stand off ratio is 2/3, find the value of stand-off voltage. What will be the peak point voltage if the forward drop in the *pn* junction is 0.7 V? **[8 V ; 8.7 V]**

Discussion Questions

1. What are advantages of a triac over an *SCR* ?
2. Why is diac preferred to trigger a triac ?
3. Why is power electronics so important ?
4. Why is diac used to trigger a triac ?
5. Is the name *UJT* appropriate?
6. What is the most common application of diac?
7. What are the symptoms of a *shorted* diac or triac?
8. What are the symptoms of an *open* diac or triac?
9. For what are *UJTs* used?

24

Electronic Instruments

Introduction

In recent years, the rapid strides and remarkable advances in the field of electronics is partly due to modern electronic instruments. By using these instruments, we can gather much information regarding the performance of specific electronic circuit. Electronic instruments are also used for trouble shooting since they permit readings to be taken so that circuit faults can be located by ascertaining which component values do not coincide with the pre-established values indicated by the manufacturer. In fact, electronic instruments are playing a vital role in the fast developing field of electronics. It is with this view that they have been treated in a separate chapter.

24.1 Electronic Instruments

Those instruments which employ electronic devices for measuring various electrical quantities (e.g. voltage, current, resistance etc.) are known as **electronic instruments.**

There are a large number of electronic instruments available for completion of various tests and measurements. However, in this chapter, we shall confine our attention to the following electronic instruments :

(*i*) Multimeter (*ii*) Vacuum tube voltmeter (*VTVM*)

(*iii*) Cathode ray oscilloscope

The knowledge of the manner in which each instrument is used plus an understanding of the applications and limitations of each instrument will enable the reader to utilise such instruments successfully.

24.2 Multimeter

A *multimeter* is an electronic instrument which can measure resistances, currents and voltages. It is an indispensable instrument and can be used for measuring d.c. as well as a.c. voltages and currents. Multimeter is the most inexpensive equipment and can make various electrical measurements with reasonable accuracy.

Construction. A multimeter consists of an ordinary pivoted type of moving coil galvanometer. This galvanometer consists of a coil pivoted on jeweled bearings between the poles of a permanent magnet. The indicating needle is fastened to the coil. When electric current is passed through the coil, mechanical force acts and the pointer moves over the scale.

Functions. A multimeter can measure voltages, currents and resistances. To achieve this objective, proper circuits are incorporated with the galvanometer. The galvanometer in a multimeter is

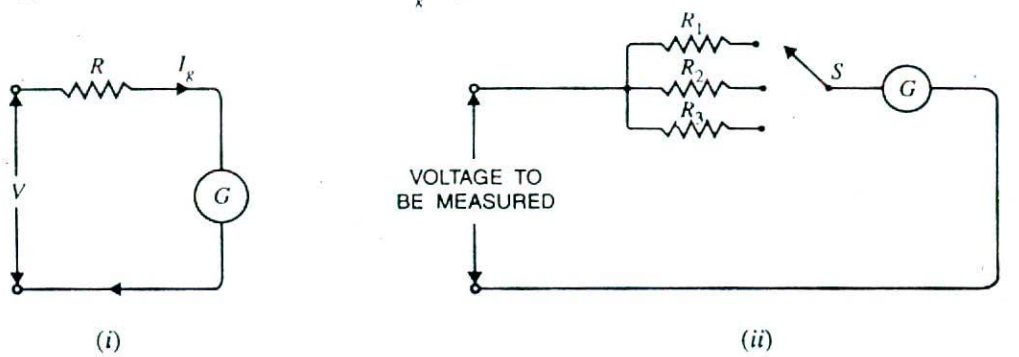
always of *left zero type i.e.* normally its needle rests in extreme left position as compared to centre zero position of ordinary galvanometers.

(*i*) **Multimeter as voltmeter.** When a high resistance is connected in series with a galvanometer, it becomes a voltmeter. Fig. 24.1 (*i*) shows a high resistance R connected in series with the galvanometer of resistance G. If I_g is the *full scale deflection current*, then the galvanometer becomes a voltmeter of range 0 – V volts. The required value of series resistance R is given by;

$$V = I_g R + I_g G$$

or $$V/I_g = R + G$$

or $$R = V/I_g - G$$



(*i*) (*ii*)

Fig. 24.1

For maximum accuracy, a multimeter is always provided with a number of voltage ranges. This is achieved by providing a number of high resistances in the multimeter as shown in Fig. 24.1 (*ii*). Each resistance corresponds to one voltage range. With the help of selector switch S, we can put any resistance (R_1, R_2 and R_3) in series with the galvanometer. When d.c. voltages are to be measured, the multimeter switch is turned on to d.c. position. This puts the circuit shown in Fig. 24.1 (*ii*) in action. By throwing the range selector switch S to a suitable position, the given d.c. voltage can be measured.

The multimeter can also measure a.c. voltages. To permit it to perform this function, a full-wave rectifier is used as shown in Fig. 24.2. The rectifier converts a.c. into d.c. for application to the galvanometer. The desired a.c. voltage range can be selected by the switch S. When a.c. voltage is to be measured, the multimeter switch is thrown to a.c. position. This puts the circuit shown in Fig. 24.2 in action. By throwing the range selector switch S to a suitable position, the given a.c. voltage can

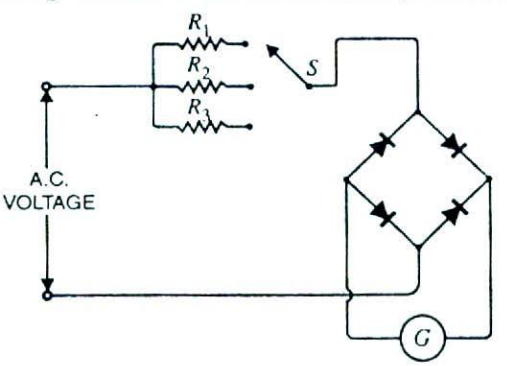


Fig. 24.2

be measured. It may be mentioned here that a.c. voltage scale is calibrated in r.m.s. values. Therefore, the meter will give the r.m.s. value of the a.c. voltage under measurement.

(*ii*) **Multimeter as ammeter.** When low resistance is connected in parallel with a galvanometer, it becomes an ammeter. Fig. 24.3 (*i*) shows a low resistance S (generally called *shunt*) connected in parallel with the galvanometer of resistance G. If I_g is the full scale deflection current, then the galvanometer becomes an ammeter of range $0 - I$ amperes. The required value of shunt resistance S is given by ;

$$I_s S = I_g G$$

or $$I_s/I_g = G/S \quad \text{or} \quad \frac{I_s}{I_g} + 1 = \frac{G}{S} + 1$$

or $$\frac{I_s + I_g}{I_g} = \frac{G + S}{S} \quad \text{or} \quad \frac{I}{I_g} = \frac{G + S}{S}$$

In practice, a number of low resistances are connected in parallel with the galvanometer to provide a number of current ranges as shown in Fig. 24.3 (*ii*). With the help of range selector switch S, any shunt can be put in parallel with the galvanometer. When d.c. current is to be measured, the multimeter switch is turned on to d.c. position. This puts the circuit shown in Fig. 24.3 (*ii*) in action. By throwing the range selector switch S to a suitable position, the desired d.c. current can be measured.

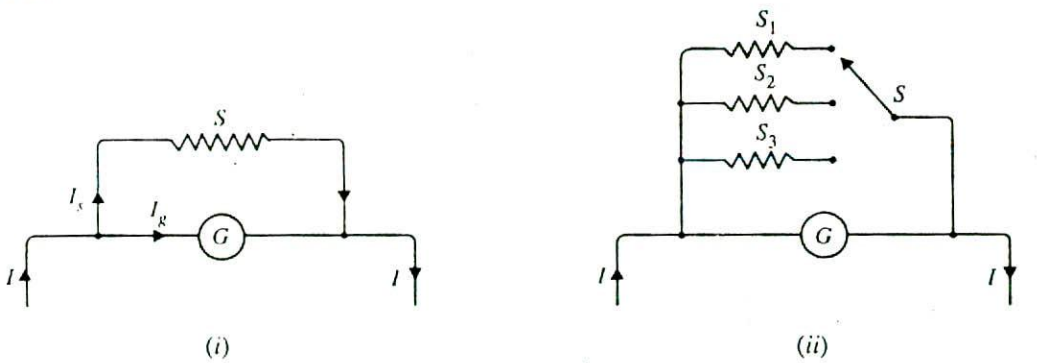


Fig. 24.3

The multimeter can also be used to measure alternating current. For this purpose, a full - wave rectifier is used as shown in Fig. 24.4. The rectifier converts a.c. into d.c. for application to the galvanometer. The desired current range can be selected by switch S. By throwing the range selector switch S to a suitable position, the given a.c. current can be measured. Again, the a.c. current scale is calibrated in r.m.s. values so that the instrument will give r.m.s. value of alternating current under measurement.

(*iii*) **Multimeter as ohmmeter.** Fig. 24.5 (*i*) shows the circuit of ohmmeter. The multimeter employs the internal battery. A fixed resistance R and a variable resistance r are connected in series with the battery and galvanometer. The fixed resistance R limits the current within the range desired and variable resistance r is for zero-adjustment reading. The resistance to be measured is connected between terminals A and B. The current flowing through the circuit will depend upon the value of resistor connected across the terminals. The ohmmeter scale is calibrated in terms of ohms. The ohmmeter is generally made multirange instrument by using different values of R as shown in Fig. 24.5 (*ii*).

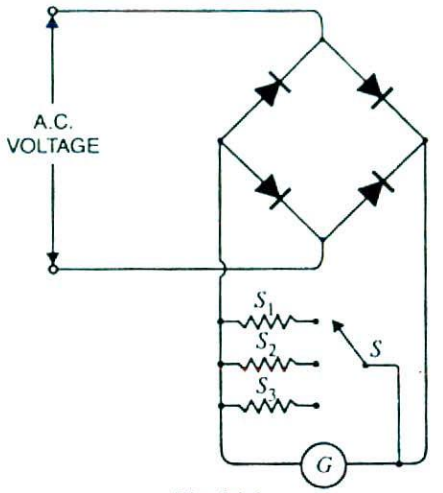


Fig. 24.4

To use ohmmeter, terminals A and B are shorted and resistance r is adjusted to give full scale deflection of the galvanometer. Under this condition, the resistance under measurement is zero. Because the needle deflects to full scale, the ohmmeter scale must then indicate *full scale deflection as zero ohm*. Then probes A and B are connected across the resistance to be measured. If the resistance to be measured is high, lower current flows through the circuit and the meter will indicate lower reading. It may be mentioned here that each time the ohmmeter is used, it is first shorted across AB and r is adjusted to zero the meter. This calibrates the meter and accommodates any decrease in the terminal voltage of the battery with age.

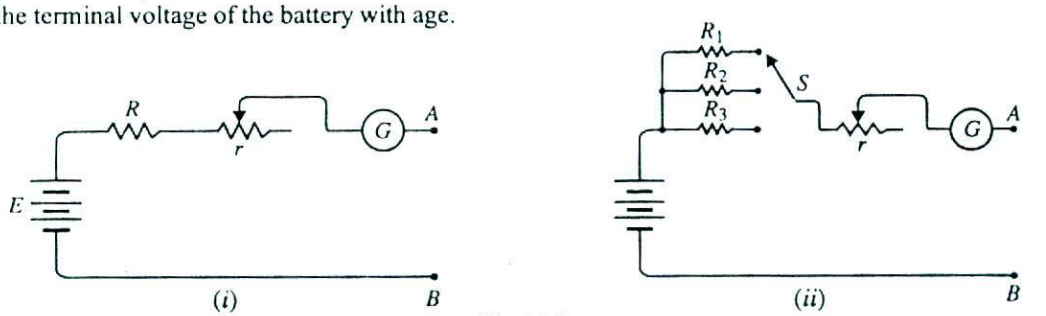


Fig. 24.5

Typical multimeter circuit. Fig 24.6 shows a typical multimeter circuit incorporating three voltage and current ranges.

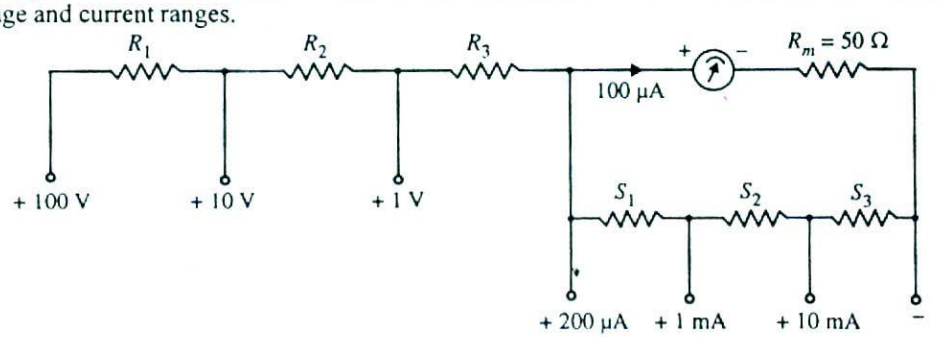


Fig. 24.6

Here the full-scale deflection (*f.s.d.*) current of the meter is 100 μA and meter resistance is 50 Ω. The design of this multimeter means finding the values of various resistances.

24.3 Applications of Multimeter

A multimeter is an extremely important electronic instrument and is extensively used for carrying out various tests and measurements in electronic circuits. It is used :

(*i*) For checking the circuit continuity. When the multimeter is employed as continuity-checking device, the ohmmeter scale is utilised and the equipment to be checked is shut off or disconnected from the power mains.

(*ii*) For measuring d.c. current flowing through the cathode, plate, screen and other vacuum tube circuits.

(*iii*) For measuring d.c. voltages across various resistors in electronic circuits.

(*iv*) For measuring a.c. voltages across power supply transformers.

(*v*) For ascertaining whether or not open or short circuit exists in the circuit under study.

24.4 Sensitivity of Multimeter

The resistance offered per volt of full scale deflection by the multimeter is known as **multimeter sensitivity.**

Multimeter sensitivity indicates the internal resistance of the multimeter. For example, if the total resistance of the meter is 5000 ohms and the meter is to read 5 volts full scale, then internal resistance of the meter is 1000 Ω per volt *i.e.* meter sensitivity is 1000 Ω per volt. Conversely, if the meter sensitivity is 400 Ω per volt which reads from 0 to 100 V, then meter resistance is 40,000 ohms. If the meter is to read V volts and I_g is the full scale deflection current, then,

$$\text{Meter resistance} = \frac{V}{I_g}$$

$$\text{Meter sensitivity} = \text{Resistance per volt full scale deflection}$$

$$= \frac{V}{I_g}\Big/V = \frac{1}{I_g}$$

Sensitivity is the most important characteristic of a multimeter. If the sensitivity of a multimeter is high, it means that it has high internal resistance. When such a meter is connected in the circuit to read voltage, it will draw a very small current. Consequently, there will be no change in the circuit current due to the introduction of the meter. Hence, it will measure the voltage correctly. On the other hand, if the sensitivity of multimeter is low, it would cause serious error in voltage measurement. The sensitivity of multimeters available in the market range from 5 kΩ per volt to 20 kΩ per volt.

24.5 Merits and Demerits of Multimeter

Although multimeter is widely used for manufacturing and servicing of electronics equipment, it has its own merits and demerits.

Merits

(*i*) It is a single meter that performs several measuring functions.

(*ii*) It has a small size and is easily portable.

(*iii*) It can make measurements with reasonable accuracy.

Demerits

(*i*) It is a costly instrument. The cost of a multimeter having sensitivity of 20 kΩ per volt is about Rs. 1000.

(*ii*) It cannot make precise and accurate measurements due to the loading effect.

(*iii*) Technical skill is required to handle it.

24.6 Meter Protection

It is important to provide protection for the meter in the event of an accidental overload. This is achieved by connecting a diode in parallel with the voltmeter as shown in Fig. 24.7.

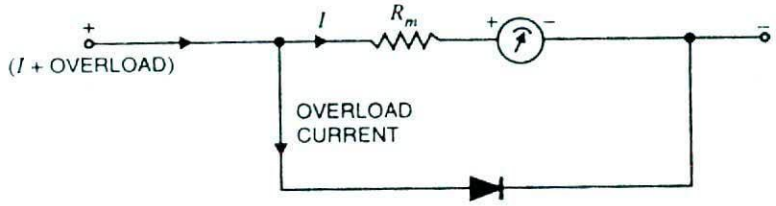


Fig. 24.7

Let us see how diode across the meter enables it to withstand overload without destroying the expensive movement. If I is the normal *f.s.d.* current, a potential difference of IR_m is developed across the diode. The circuit is so designed that IR_m does not turn on the diode. In the event of an accidental overload (say 5 I), the voltage across diode becomes 5 times greater and it is immediately turned on. Consequently, diode diverts most of the overload current in the same manner as a shunt. Thus protection of the meter against overload is ensured. Silicon diodes are perhaps the best to use in such circuits.

Example 24.1. *A multimeter has full scale deflection current of 1 mA. Determine its sensitivity.*

Solution. Full scale deflection current, $I_g = 1 \text{ mA} = 10^{-3} \text{ A}$

$\therefore$ Multimeter sensitivity $= 1/I_g = 1/10^{-3} =$ **1000 Ω per volt**

Example 24.2. *A multimeter has a sensitivity of 1000 Ω per volt and reads 50 V full scale. If the meter is to be used to measure the voltage across 50000 Ω resistor, will it read correctly ?*

Solution. Meter sensitivity = 1000 Ω per volt

Full scale volts = 50 V

$\therefore$ Meter resistance $= 50 \times 1000 = 50{,}000\ \Omega$

When the meter is used to measure the voltage across the resistance as shown in Fig. 24.8, the total resistance of the circuit is a parallel combination of two 50,000 Ω resistors. Therefore, the circuit resistance would be reduced to 25000 Ω and double the amount of current would be drawn than would otherwise be the case.

$\therefore$ *Meter will give highly incorrect reading.*

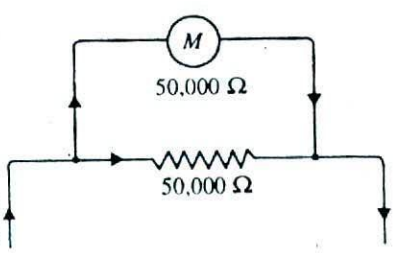


Fig. 24.8

Comments. This example shows the limitation of multimeter. The multimeter will read correctly only if its resistance is very high as compared to the resistance across which voltage is to be measured.

As a rule, the resistance of the multimeter should be atleast 100 times the resistance across which voltage is to be measured.

Example 24.3. *In the circuit shown in Fig. 24.9 (i), it is desired to measure the voltage across 10 kΩ resistance. If a multimeter of sensitivity 4 kΩ/volt and range 0-10 V is used for the purpose, what will be the reading ?*

Solution. In the circuit shown in Fig. 24.9 (*i*), the circuit current by Ohm's law is 1 mA. Therefore, voltage across 10 kΩ resistance is 10 V. Let us see whether the given multimeter reads this value. Fig. 24.9 (*ii*) shows the multimeter connected across 10 kΩ resistance. The introduction of multimeter will change the circuit resistance and hence circuit current.

$$\text{Resistance of meter} = 4\ \text{k}\Omega \times 10 = 40\ \text{k}\Omega$$

$$\text{Total circuit resistance} = 40\ \text{k}\Omega \parallel 10\ \text{k}\Omega + 10\ \text{k}\Omega$$

$$= \frac{40 \times 10}{40 + 10} + 10 = 8 + 10 = 18\ \text{k}\Omega$$

$$\text{Circuit current} = \frac{20\ V}{18\ \text{k}\Omega} = 1.11\ \text{mA}$$

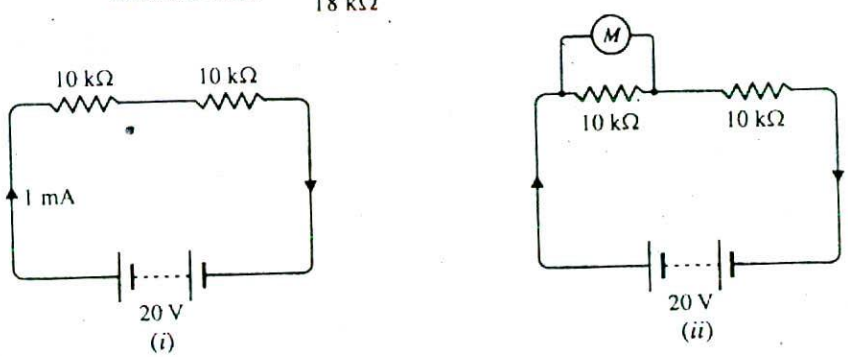


Fig. 24.9

$$\text{Voltage read by multimeter} = 8\ \text{k}\Omega \times 1.11\ \text{mA} = \mathbf{8.88\ V}$$

Example 24.4. *If in the above example, a multimeter of sensitivity 20 kΩ per volt is used, what will be the reading ?*

Solution. $\text{Meter resistance} = 20\ \text{k}\Omega \times 10 = 200\ \text{k}\Omega$

$$\text{Total circuit resistance} = 200\ \text{k}\Omega \parallel 10\ \text{k}\Omega + 10\ \text{k}\Omega$$

$$= \frac{200 \times 10}{200 + 10} + 10 = 9.5 + 10 = 19.5\ \text{k}\Omega$$

$$\text{Circuit current} = \frac{20\ V}{19.5\ \text{k}\Omega} = 1.04\ \text{mA}$$

$\therefore$ Voltage read by multimeter $= 9.5\ \text{k}\Omega \times 1.04\ \text{mA} = \mathbf{9.88\ V}$

A comparison of examples 24.3 and 24.4 shows that a multimeter with higher sensitivity gives more correct reading.

Example 24.5. *In the circuit shown in Fig. 24.10, find the voltage at points A, B, C and D (i) before the meter is connected and (ii) after the meter is connected. Explain why the meter readings differ from those without the meter connected.*

Solution. (*i*) **When meter is not connected.** When meter is not connected in the circuit, the circuit is a simple series circuit consisting of resistances 20 kΩ, 20 kΩ, 30 kΩ and 30 kΩ.

$$\text{Total circuit resistance} = 20 + 20 + 30 + 30 = 100\ \text{k}\Omega$$

$$\text{Circuit current} = \frac{100\ V}{100\ \text{k}\Omega} = 1\ \text{mA}$$

$$\text{Voltage at point } A = \mathbf{100\ V}$$

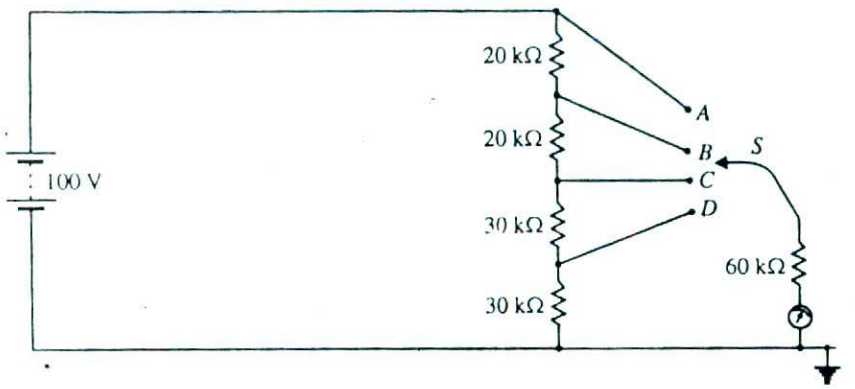


Fig. 24.10

Voltage at point B = 100 − 1 mA × 20 kΩ = **80 V**

Voltage at point C = 100 − 1 mA × 40 kΩ = **60V**

Voltage at point D = 100 − 1 mA × 70 kΩ = **30V**

(*ii*) **When meter is connected.** When meter is connected in the circuit, the circuit becomes a series parallel circuit. The total circuit resistance would depend upon the position of switch S.

(*a*) *When switch is at position A*

The voltage at point A is 100 V because point A is directly connected to the voltage source.

$\therefore$ Voltage at point A = **100 V**

(*b*) *When switch is at position B*

$$\text{Total circuit resistance} = 20 + \frac{80 \times 60}{80 + 60} = 20 + 34.28 = 54.28\ \text{k}\Omega$$

$$\therefore \quad \text{Circuit current} = \frac{100\ V}{54.28\ \text{k}\Omega}$$

$$\therefore \quad \text{Voltage at point } B = \frac{100\ \text{V}}{54.28\ \text{k}\Omega} \times 34.28\ \text{k}\Omega = \mathbf{63\ V}$$

(*c*) *When switch is at point C*

$$\text{Total circuit resistance} = 40 + \frac{60 \times 60}{60 + 60} = 40 + 30 = 70\ \text{k}\Omega$$

$$\therefore \quad \text{Circuit current} = \frac{100\ \text{V}}{70\ \text{k}\Omega}$$

$$\therefore \quad \text{Voltage at point } C = \frac{100\ \text{V}}{70\ \text{k}\Omega} \times 30\ \text{k}\Omega = \mathbf{42.8\ V}$$

(*d*) *When switch is at point D*

$$\text{Total circuit resistance} = 70 + \frac{30 \times 60}{30 + 60} = 70 + 20 = 90\ \text{k}\Omega$$

$$\therefore \quad \text{Circuit current} = \frac{100\ \text{V}}{90\ \text{k}\Omega}$$

$$\therefore \quad \text{Voltage at point } D = \frac{100\ \text{V}}{90\ \text{k}\Omega} \times 20\ \text{k}\Omega = \mathbf{22.2\ V}$$

Comments. Note that potential measurements are being made in a high-impedance circuit; the

circuit resistance is comparable to meter resistance. As a rule, the resistance of the voltmeter should be 100 times the resistance across which voltage is to be measured. Since such a condition is not realised in this problem, the meter readings differ appreciably from those without the meter connected.

24.7 Vacuum Tube Voltmeter (VTVM)

A vacuum tube voltmeter consists of any ordinary voltmeter and electron tubes. It is extensively used for measuring both a.c. and d.c. voltages. The vacuum tube voltmeter has high internal resistance (> 10 MΩ) and draws extremely small current from the circuit across which it is connected. In other words, the loading effect of this instrument is very small. Therefore, a *VTVM* measures the exact voltage even across a high resistance. In fact, the ability of *VTVM* to measure the voltages accurately has made this instrument the most popular with technicians for trouble shooting radio and television receivers as well as for laboratory work involving research and design.

(*i*) **Simple VTVM circuit.** Fig. 24.11 shows the simple circuit of a vacuum tube voltmeter. It consists of a triode having meter *M* connected in the plate circuit. The meter is calibrated in volts. R_1 is the grid leak resistor. The voltage to be measured is applied at the grid of triode in such a way that grid is always negative *w.r.t.* cathode. This voltage at the grid is transformed by the triode into corresponding plate current. The meter *M* connected in the plate circuit directly gives the value of the voltage under measurement. It may be seen that as grid draws extremely small current (< 1 μA), therefore, internal resistance of *VTVM* is very large. This circuit has the disadvantage that if the applied voltages change (especially filament voltage), the plate current will also change. Consequently, the meter will give wrong reading.

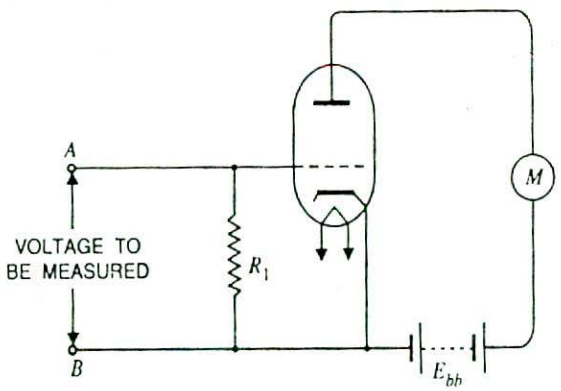


Fig. 24.11

(*ii*) **Balanced bridge Type VTVM.** The disadvantage of above circuit is overcome in the balanced bridge type *VTVM* shown in Fig. 24.12. Here, two similar triodes V_1 and V_2 are used. The meter *M* is connected between the plates of triodes and indicates the voltage to be measured. The variable resistance *r* in the plate circuit of V_2 is for zero adjustment of the meter. The voltage to be measured is applied at the grid of triode V_1 in such a way that grid is always negative with respect to cathode.

Operation. When no voltage is applied at the input terminals *AB*, the plate currents flowing in both valves are equal as the triodes are similar. Therefore, plates of both valves are at the same potential. Consequently, the current through the meter *M* is zero and the meter reads zero volt. However, in actual practice, there are always some constructional differences in plates, grids and cathodes of the two valves. The result is that two plate currents differ slightly and the meter may give

some reading. In such a case, the meter needle is brought to zero by changing resistance r.

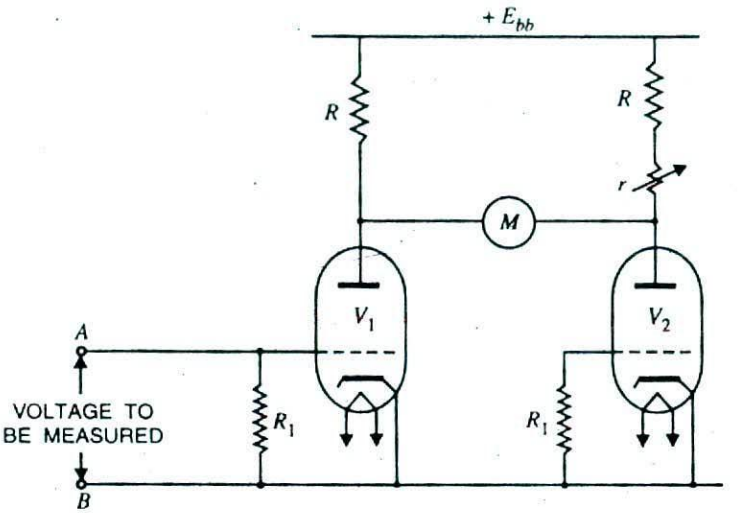


Fig. 24.12

The voltage to be measured is applied at the grid of triode V_1, making the grid negative *w.r.t.* cathode. This changes the plate current of triode V_1 and the plates of two valves no longer remain at the same potential. Therefore, a small current flows through the meter M which directly gives the value of the voltage being measured. It may be noted that actually triode V_1 is used for voltage measurement, the purpose of V_2 is simply to prevent zero drift. By using two similar tubes, any change in plate current due to supply fluctuations will equally affect the two plate currents. Therefore, net change in potential drop across voltmeter is zero.

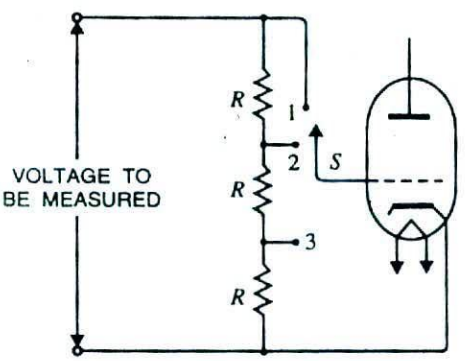


Fig. 24.13

Range selection. In practice, a *VTVM* is made a multirange instrument by employing a potentiometer at the input circuit as shown in Fig. 24.13. By throwing the range selector switch S to a suitable position, the desired voltage range can be obtained. Thus when the range selector switch S is thrown to position 1, the voltage applied to the grid is three times as compared to position 3. Although only three voltage ranges have been considered, a commercial *VTVM* may have more ranges.

24.8 Applications of VTVM

A *VTVM* is far superior to a multimeter and performs a number of measuring functions. A few

important applications of *VTVM* are discussed below :

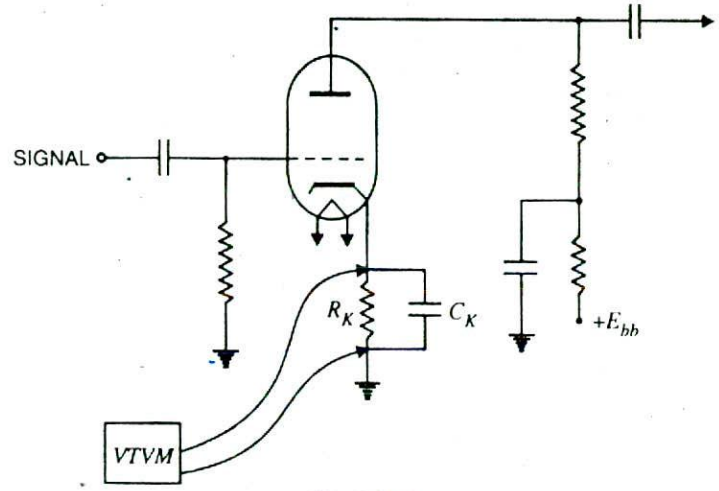


Fig. 24.14

(*i*) **d.c. voltage measurements.** A *VTVM* can accurately measure the d.c. voltages in an electronic circuit. The d.c. voltage to be measured is applied at the input (*i.e.* grid of V_1) terminals in such a way that grid of the input valve V_1 is always negative. Fig. 24.14 shows the circuit of an amplifier stage and measurement of d.c. voltage across cathode resistor R_K.

(*ii*) **d.c. current measurements.** A conventional *VTVM* does not incorporate a current scale. However, current values can be found indirectly. For instance, in Fig. 24.14, the d.c. current through R_K can be found by noting the voltage across R_K and dividing it by the resistance R_K.

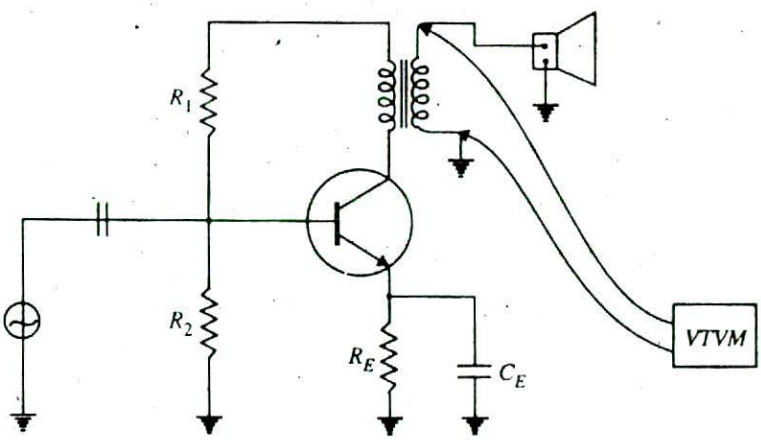


Fig. 24.15

(*iii*) **a.c. voltage measurements.** For measuring a.c. voltage, a rectifier is used in conjunction with a *VTVM*. The rectifier converts a.c. into d.c. for application to the grid of valve V_1. In fact, rectifier circuit is a part of *VTVM*. Fig. 24.15 shows the transistor power amplifier stage and measurement of a.c. voltage across the speaker.

(*iv*) **Resistance measurements.** A *VTVM* can be used to measure resistances and has the ability to measure resistances upto 1000 megaohms whereas the ordinary ohmmeter will measure only upto

about 10 megaohms. Fig. 24.16 shows the circuit of *VTVM* ohmeter. By throwing the selector switch *S* to any suitable position, the desired resistance range can be obtained. The unknown resistor whose value is to be measured is connected between points *A* and *B*. If the unknown resistance has high

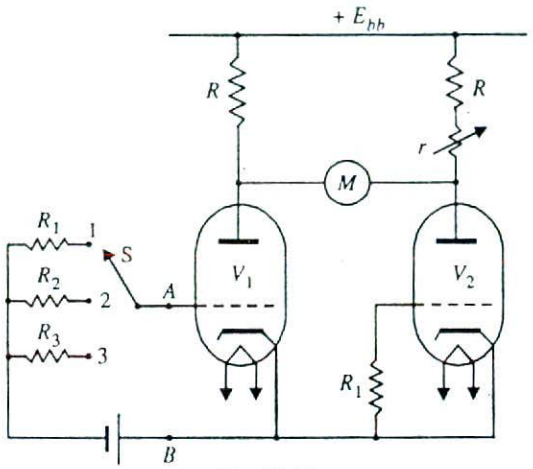


Fig. 24.16

value, a higher negative bias will be applied to triode V_1. Reverse will happen if the unknown resistance has low value. The imbalance in the plate currents of the two valves will cause a current through the meter *M* which will directly give the value over the resistance scale of the meter.

24.9 Merits and Demerits of VTVM

A *VTVM* is an extremely important electronic equipment and is widely used for making different measurements in electronic circuits.

Merits

(*i*) A *VTVM* draws extremely small current from the measuring circuit. Therefore, it gives accurate readings.

(*ii*) There is little effect of temperature variations.

(*iii*) Because a *VTVM* uses triodes, the voltage to be measured is amplified. This permits the use of less sensitive meter.

(*iv*) It has a wide frequency response.

Demerits

(*i*) It cannot make current measurements directly.

(*ii*) Accurate readings can be obtained only for sine waves.

24.10 Cathode Ray Oscilloscope

The cathode ray oscilloscope (commonly abbreviated as *CRO*) is an electronic device which is capable of giving a visual indication of a signal waveform. No other instrument used in the electronic industry is as versatile as the cathode ray oscilloscope. It is widely used for trouble shooting radio and television receivers as well as for laboratory work involving research and design. With an oscilloscope, the waveshape of a signal can be studied with respect to amplitude distortion and deviation from the normal. In addition, the oscilloscope can also be used for measuring voltage, frequency and phase shift.

In an oscilloscope, the electrons are emitted from a cathode accelerated to a high velocity and

brought to focus on a fluorescent screen. The screen produces a visible spot where the electron beam strikes. By deflecting the electron beam over the screen in response to the electrical signal, the electrons can be made to act as an *electrical pencil of light* which produces a spot of light wherever it strikes. An oscilloscope obtains its remarkable properties as a measuring instrument from the fact that it uses as an indicating needle a beam of electrons. As electrons have negligible mass, therefore, they respond almost instantaneously when acted upon by an electrical signal and can trace almost any electrical variation no matter how rapid. A cathode ray oscilloscope contains a *cathode ray tube* and necessary power equipment to make it operate.

24.11 Cathode Ray Tube

A cathode ray tube (commonly abbreviated as *CRT*) is the heart of the oscilloscope. It is a vacuum tube of special geometrical shape and converts an electrical signal into visual one. A cathode ray tube makes available plenty of electrons. These electrons are accelerated to high velocity and are brought to focus on a fluorescent screen. The electron beam produces a spot of light wherever it strikes. The electron beam is deflected on its journey in response to the electrical signal under study. The result is that electrical signal waveform is displayed visually. Fig. 24.17 shows the various parts of cathode ray tube.

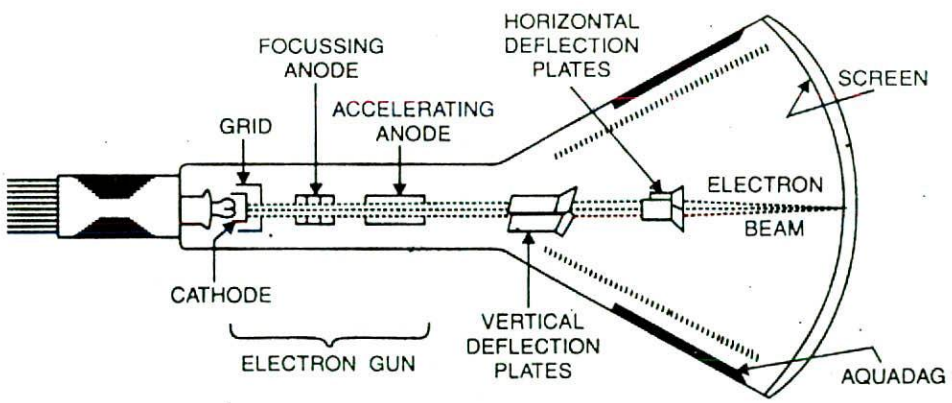


Fig. 24.17

(*i*) **Glass envelope.** It is conical highly evacuated glass housing and maintains vacuum inside and supports the various electrodes. The inner walls of *CRT* between neck and screen are usually coated with a conducting material, called *aquadag*. This coating is electrically connected to the accelerating anode so that electrons which accidently strike the walls are returned to the anode. This prevents the walls of the tube from charging to a high negative potential.

(*ii*) **Electron gun assembly.** The arrangement of electrodes which produce a focussed beam of electrons is called the *electron gun*. It essentially consists of an indirectly heated *cathode*, a *control grid*, a *focusing anode* and an *accelerating anode*. The control grid is held at negative potential *w.r.t.* cathode whereas the two anodes are maintained at high positive potential *w.r.t.* cathode.

The cathode consists of a nickel cylinder coated with oxide coating and provides plenty of electrons. The control grid encloses the cathode and consists of a metal cylinder with a tiny circular opening to keep the electron beam small in size. The focussing anode focuses the electron beam into a sharp pin-point by controlling the positive potential on it. The positive potential (about 10,000 V) on the accelerating anode is much higher than on the focusing anode. For this reason, this anode accelerates the narrow beam to a high velocity. Therefore, the electron gun assembly forms a narrow, accelerated beam of electrons which produces a spot of light when it strikes the screen.

(*iii*) **Deflection plate assembly.** The deflection of the beam is accomplished by two sets of deflecting plates placed within the tube beyond the accelerating anode as shown in Fig. 24.17. One set is the *vertical deflection plates* and the other set is the *horizontal deflection plates*.

The vertical deflection plates are mounted horizontally in the tube. By applying proper potential to these plates, the electron beam can be made to move up and down vertically on the fluorescent screen. The horizontal deflection plates are mounted in the vertical plane. An appropriate potential on these plate can cause the electron beam to move right and left horizontally on the screen.

(*iv*) **Screen.** The screen is the inside face of the tube and is coated with some fluorescent material such as zinc orthosilicate, zinc oxide etc. When high velocity electron beam strikes the screen, a spot of light is produced at the point of impact. The colour of the spot depends upon the nature of fluorescent material. If zinc orthosilicate is used as the fluorescent material, green light spot is produced.

Action of CRT. When the cathode is heated, it emits plenty of electrons. These electrons pass through control grid on their way to screen. The control grid influences the amount of current flow as in standard vacuum tubes. If negative potential on the control grid is high, fewer electrons will pass through it and the electron beam on striking the screen will produce a dim spot of light. Reverse will happen if the negative potential on the control grid is reduced. Thus, the intensity of light spot on the screen can be changed by changing the negative potential on the control grid. As the electron beam leaves the control grid, it comes under the influence of focussing and accelerating anodes. As the two anodes are maintained at high positive potential, therefore, they produce a field which acts as an *electrostatic lens* to converge the electron beam at a point on the screen.

As the electron beam leaves the accelerating anode, it comes under the influence of vertical and horizontal deflection plates. If no voltage is applied to the deflection plates, the electron beam will produce spot of light at the centre (point *O* in Fig. 24.18) of the screen. If the voltage is applied to vertical plates *only* as shown in Fig. 24.18, the electron beam and hence the spot of light will be deflected upwards (point O_1). The spot of light will be deflected downwards (point O_2) if the potential on the plates is reversed. Similarly, the spot of light can be moved horizontally by applying voltage across the horizontal plates.

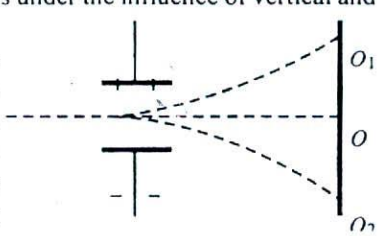


Fig. 24.18

24.12 Deflection Sensitivity of CRT

The shift of the spot of light on the screen per unit change in voltage across the deflection plates is known as *deflection sensitivity* of *CRT*. For instance, if a voltage of 100 V applied to the vertical plates produces a vertical shift of 3 mm in the spot, then deflection sensitivity is 0.03 mm/V. In general,

$$\text{Spot deflection} = \text{Deflection sensitivity} \times \text{Applied voltage}$$

The deflection sensitivity depends not only on the design of the tube but also on the voltage applied to the accelerating anode. The deflection sensitivity is low at high accelerating voltages and vice-versa.

Example 24.6. *The deflection sensitivity of a CRT is 0.01 mm/V. Find the shift produced in the spot when 400 V are applied to the vertical plates.*

Solution. As voltage is applied to the vertical plates only, therefore, the spot will be shifted vertically.

$$\text{Spot shift} = \text{deflection sensitivity} \times \text{applied voltage}$$

$$= 0.01 \times 400 = \mathbf{4\ mm}$$

Example 24.7. *The deflection sensitivity of a CRT is 0.03 mm/V. If an unknown voltage is applied to the horizontal plates, the spot shifts 3 mm horizontally. Find the value of unknown voltage.*

Solution. Deflection sensitivity = 0.03 mm/V

Spot shift = 3 mm

Now, spot shift = deflection sensitivity × applied voltage

$$\therefore \quad \text{Applied voltage} = \frac{\text{spot shift}}{\text{deflection sensitivity}} = \frac{3 \text{ mm}}{0.03 \text{ mm/V}} = \mathbf{100\ V}$$

24.13 Applying Signal Across Vertical Plates

If a sinusoidal voltage is applied to the vertical deflection plates, it will make the plates alternately positive and negative. Thus, in the positive half of the signal, upper plate will be positive and lower plate negative while in the negative half-cycle, the plate polarities will be reversed.

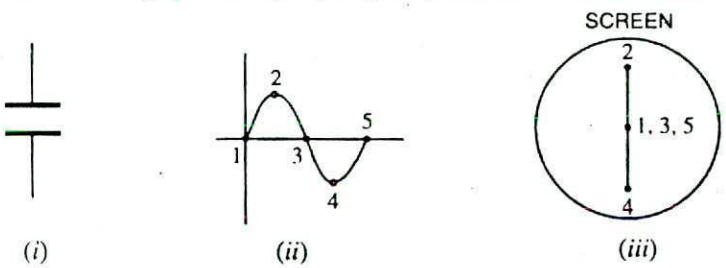


Fig. 24.19

The result is that the spot moves up and down at the same rate as the frequency of the applied voltage. As the frequency of applied voltage is 50 Hz, therefore, due to persistence of vision, we will see a continuous vertical line 2 - 1 - 4 on the screen as shown in Fig. 24.19 (*iii*). The line gives no indication of the manner in which the voltage is alternating since it does not reveal the waveform.

24.14 Display of Signal Waveform on CRO

One interesting application of *CRO* is to present the wave shape of the signal on the screen. As discussed before, if sinusoidal signal is applied to the vertical deflection plates, we get a vertical line. However, it is desired to see the signal voltage variations with time on the screen. This is possible only if we could also move the beam horizontally from left to right at a uniform speed while it is moving up and down. Further, as soon as a full cycle of the signal is traced, the beam should return quickly to the left hand side of the screen so that it can start tracing the second cycle.

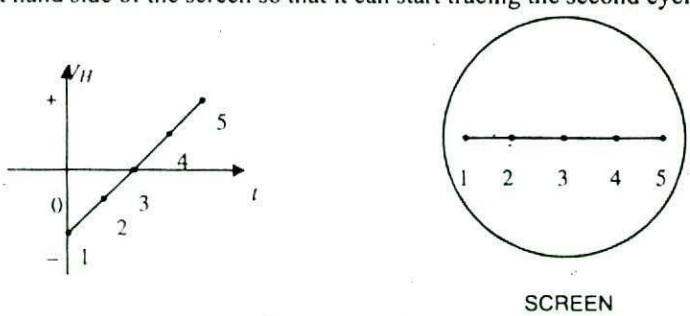


Fig. 24.20

In order that the beam moves from left to right at a uniform rate, a voltage that varies linearly with time should be applied to the horizontal plates. This condition is exactly met in the saw tooth wave shown in Fig. 24.20 (*i*).

When time $t = 0$, the negative voltage on the horizontal plates keep the beam to the extreme left on the screen as shown in Fig. 24.20 (*ii*). As the time progresses, the negative voltage decreases linearly with time and the beam moves towards right forming a horizontal line. In this way, the saw tooth wave applied to horizontal plates moves the beam from left to right at a uniform rate.

24.15 Signal Pattern on Screen

If the signal voltage is applied to the vertical plates and saw tooth wave to the horizontal plates, we get the exact pattern of the signal as shown in Fig. 24.21. When the signal is at the instant 1, its amplitude is zero. But at this instant, maximum negative voltage is applied to horizontal plates. The result is that the beam is at the extreme left on the screen as shown. When the signal is at the instant 2, its amplitude is maximum. However, the negative voltage on the horizontal plates is decreased. Therefore, the beam is deflected upwards by the signal and towards the right by the saw tooth wave. The result is that the beam now strikes the screen at point 2. On similar reasoning, the beam strikes the screen at points 3, 4 and 5. In this way, we have the exact signal pattern on the screen.

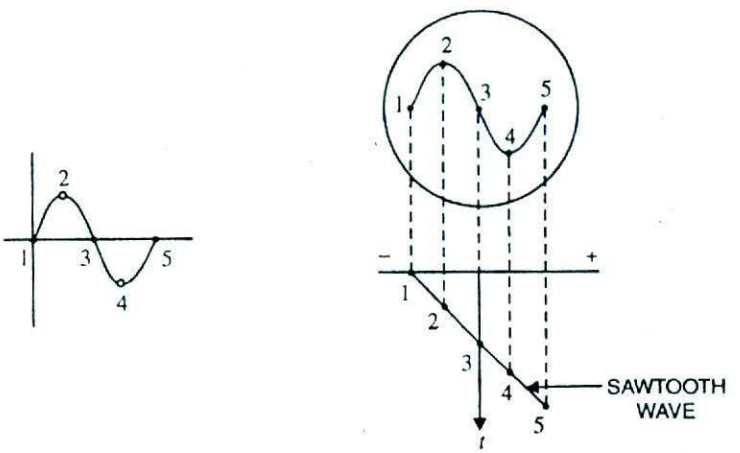


Fig. 24.21

24.16 Various Controls of CRO

In order to facilitate the proper functioning of *CRO*, various controls are provided on the face of *CRO*. A few of them are given below:

(*i*) *Intensity control.* The knob of intensity control regulates the bias on the control grid and affects the electron beam intensity. If the negative bias on the grid is increased, the intensity of electron beam is decreased, thus reducing the brightness of the spot.

(*ii*) *Focus control.* The knob of focus control regulates the positive potential on the focussing anode. If the positive potential on this anode is increased, the electron beam becomes quite narrow and the spot on the screen is a pin-point.

(*iii*) *Horizontal position control.* The knob of horizontal position control regulates the amplitude of d.c. potential which is applied to the horizontal deflection plates, in addition to the usual saw tooth wave. By adjusting this control, the spot can be moved to right or left as required.

(*iv*) *Vertical position control.* The knob of vertical position control regulates the amplitude of d.c. potential which is applied to the vertical deflection plates in addition to the signal. By adjusting this control, the image can be moved up or down as required.

24.17 Applications of CRO

The modern cathode ray oscilloscope provides a powerful tool for solving problems in electrical measurements. Some important applications of *CRO* are :

1. Examination of waveforms
2. Voltage measurement
3. Frequency measurement

1. Examination of waveform. One of the important uses of *CRO* is to observe the wave shapes of voltages in various types of electronic circuits. For this purpose, the signal under study is applied to vertical input (*i.e.*, vertical deflection plates) terminals of the oscilloscope. The sweep circuit is set to internal so that sawtooth wave is applied to the horizontal input *i.e.* horizontal deflection plates. Then various controls are adjusted to obtain sharp and well defined signal waveform on the screen.

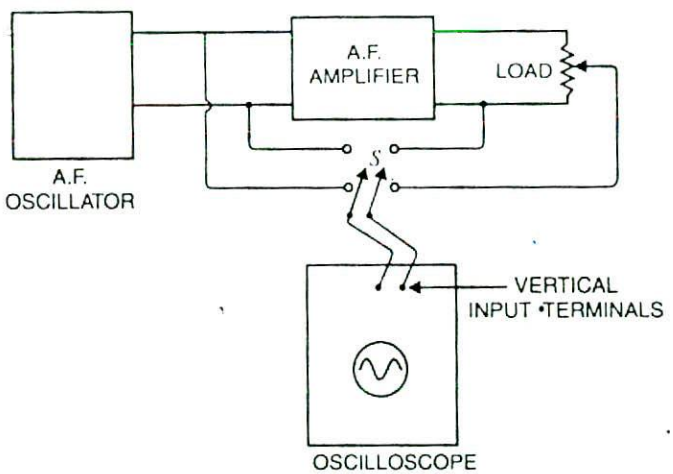


Fig. 24.22

Fig. 24.22 shows the circuit for studying the performance of an audio amplifier. With the help of switch *S*, the output and input of amplifier is applied in turn to the vertical input terminals. If the waveforms are identical in shape, the fidelity of the amplifier is excellent.

2. Voltage measurement. As discussed before, if the signal is applied to the vertical deflection plates only, a vertical line appears on the screen. The height of the line is proportional to peak-to-peak voltage of the applied signal. The following procedure is adopted for measuring voltages with *CRO*.

(*i*) Shut off the internal horizontal sweep generator.

(*ii*) Attach a transparent plastic screen to the face of oscilloscope. Mark off the screen with vertical and horizontal lines in the form of graph.

(*iii*) Now, calibrate the oscilloscope against a known voltage. Apply the known voltage, say 10 V, to the vertical input terminals of the oscilloscope. Since the sweep circuit is shut off, you will get a vertical line. Adjust the vertical gain till a good deflection is obtained. Let the deflection sensitivity be V volts/mm.

(*iv*) Keeping the vertical gain unchanged, apply the unknown voltage to be measured to the vertical input terminals of *CRO*.

(*v*) Measure the length of the vertical line obtained. Let it be *l* mm.

Then, Unknown voltage $= l \times V$ volts

3. Frequency measurement. The unknown frequency can be accurately determined with the help of a *CRO*. The steps of the procedure are as under :

(*i*) A known frequency is applied to horizontal input and unknown frequency to the vertical input.

(*ii*) The various controls are adjusted.

(*iii*) A pattern with loops is obtained.

(*iv*) The number of loops cut by the horizontal line gives the frequency on the vertical plates (f_v) and the number of loops cut by the vertical line gives the frequency on the horizontal plates (f_H).

$$\frac{f_v}{f_H} = \frac{\text{No. of loops cut by horizontal line}}{\text{No. of loops cut by vertical line}}$$

For instance, suppose during the frequency measurement test, a pattern shown in Fig. 24.23 is obtained. Let us further assume that frequency applied to horizontal plates is 2000 Hz. If we draw horizontal and vertical lines, we find that one loop is cut by the horizontal line and two loops by the vertical line. Therefore,

$$\frac{f_v}{f_H} = \frac{\text{No. of loops cut by horizontal line}}{\text{No. of loops cut by vertical line}}$$

$$\frac{f_v}{2000} = \frac{1}{2}$$

or $f_v = 2000 \times 1/2 = 1000$ Hz

i.e. Unknown frequency is 1000 Hz

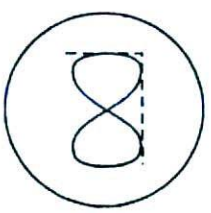


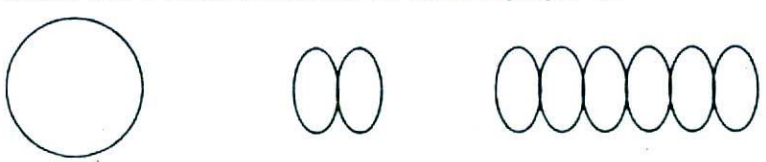
Fig. 24.23

Example 24.8. *In an oscilloscope, 200 V, 50 Hz signal produces a deflection of 2 cm corresponding to a certain setting of vertical gain control. If another voltage produces 3 cm deflection, what is the value of this voltage ?*

Solution. Deflection sensitivity = 200 V/2 cm = 100 V/cm

Unknown voltage = D. S. × deflection = 100×3 = **300 V**

Example 24.9. *When signals of different frequencies were applied to the vertical input terminals of oscilloscope, the patterns shown in Fig. 24.24 were obtained. If the frequency applied to horizontal plates in each case is 1000Hz, determine the unknown frequency.*



(*i*) (*ii*) (*iii*)

Fig. 24.24

Solution.

(*i*) The number of loops cut by horizontal and vertical line is one.

$$\therefore \quad \frac{f_v}{f_H} = \frac{1}{1} \quad \text{or} \quad f_v = f_H = \mathbf{1000\ Hz}$$

(*ii*) The number of loops cut by horizontal line is 2 and the number of loops cut by vertical line is 1.

$$\therefore \quad \frac{f_v}{f_H} = \frac{2}{1} \quad \text{or} \quad f_v = 2 \times f_H = 2 \times 1000 = \mathbf{2000\ Hz}$$

(*iii*) The number of loops cut by the horizontal line is 6 and that by vertical line is 1.

$$\therefore \quad \frac{f_v}{f_H} = \frac{6}{1}$$

or $$f_v = 6 f_H = 6 \times 1000 = \mathbf{6000\ Hz}$$

Multiple-Choice Questions

1. An ammeter is connected in ..... with the circuit element whose current we wish to measure.
   (*i*) series
   (*ii*) parallel
   (*iii*) series or parallel
   (*iv*) none of the above
2. A galvanometer in series with a high resistance is called .....
   (*i*) an ammeter (*ii*) a voltmeter
   (*iii*) a wattmeter (*iv*) none of the above
3. An ammeter should have ..... resistance.
   (*i*) infinite (*ii*) very large
   (*iii*) very low (*iv*) none of the above
4. A voltmeter is connected in ..... with the circuit component across which potential difference is to be measured.
   (*i*) parallel
   (*ii*) series
   (*iii*) series or parallel
   (*iv*) none of the above
5. A voltmeter should have ..... resistance.
   (*i*) zero (*ii*) very high
   (*iii*) very low (*iv*) none of the above
6. The sensitivity of a multimeter is given in .....
   (*i*) Ω (*ii*) amperes
   (*iii*) kΩ/V (*iv*) none of the above
7. If the full-scale deflection current of a multimeter is 50 μA, its sensitivity is .....
   (*i*) 10 kΩ/V (*ii*) 100 kΩ/V
   (*iii*) 50 kΩ/V (*iv*) 20 kΩ/V
8. If a multimeter has a sensitivity of 1000 Ω per volt and reads 50 V full scale, its internal resistance is.....
   (*i*) 20 kΩ (*ii*) 50 kΩ
   (*iii*) 10 kΩ (*iv*) none of the above
9. A *VTVM* has ..... input resistance than that of a multimeter.
   (*i*) more (*ii*) less
   (*iii*) same (*iv*) none of the above
10. The input resistance of a *VTVM* is about .....
    (*i*) 1000 Ω (*ii*) 10 kΩ
    (*iii*) 20 kΩ (*iv*) 10 MΩ
11. If the negative potential on the control grid of *CRT* is increased, the intensity of spot .....
    (*i*) is increased
    (*ii*) is decreased
    (*iii*) remains the same
    (*iv*) none of the above
12. For display of signal pattern ..... voltage is applied to the horizontal plates of a *CRO*.
    (*i*) sinusoidal (*ii*) rectangular
    (*iii*) sawtooth (*iv*) none of the above
13. Two multimeters A and B have sensitivities of 10 kΩ/V and 30 kΩ/V respectively. Then .....
    (*i*) multimeter A is more sensitive
    (*ii*) multimeter B is more sensitive
    (*iii*) both are equally sensitive
    (*iv*) none of the above
14. A galvanometer of resistance G is shunted

by a very small resistance S. The resistance of the resulting ammeter is .....

(*i*) $\frac{GS}{G+S}$ (*ii*) $G+S$

(*iii*) $G-S$ (*iv*) none of the above

15. A *VTVM* is never used to measure .....

(*i*) voltage (*ii*) current

(*iii*) resistance (*iv*) none of the above

16. The sensitivity of a voltmeter which uses a 100 μA meter movement is .....

(*i*) 1 kΩ/V (*ii*) 10 kΩ/V

(*iii*) 5 kΩ/V (*iv*) data insufficient

17. What is the total resistance of a voltmeter on the 10 V range when the meter movement is rated for 50 μA of full-scale current ?

(*i*) 10 kΩ (*ii*) 20 kΩ

(*iii*) 200 kΩ (*iv*) none of the above

18. The material used to coat inside face of *CRT* is .....

(*i*) carbon (*ii*) sulphur

(*iii*) silicon (*iv*) phosphor

19. When an ammeter is inserted in the circuit, the circuit current will .....

(*i*) increase

(*ii*) decrease

(*iii*) remain the same

(*iv*) none of the above

20. A series ohmmeter circuit uses a 3 V battery and a 1 mA meter movement. What is the half-scale resistance for this movement ?

(*i*) 3 kΩ (*ii*) 1.5 kΩ

(*iii*) 4.5 kΩ (*iv*) 6 kΩ

21. The most accurate device for measuring voltage is .....

(*i*) voltmeter (*ii*) multimeter

(*iii*) *CRO* (*iv*) *VTVM*

22. The horizontal plates of a *CRO* are supplied with ..... to observe the waveform of a signal.

(*i*) sinusoidal wave

(*ii*) cosine wave

(*iii*) sawtooth wave

(*iv*) none of the above

23. A *CRO* is used to measure .....

(*i*) voltage (*ii*) frequency

(*iii*) phase (*iv*) all of above

24. If 2 % of the main current is to be passed through a galvanometer of resistance G, then resistance of the shunt required is .....

(*i*) $G/50$ (*ii*) $G/49$

(*iii*) $49\,G$ (*iv*) $50\,G$

25. Which of the following is likely to have the largest resistance ?

(*i*) voltmeter of range 10 V

(*ii*) moving coil galvanometer

(*iii*) ammeter of range 1 A

(*iv*) a copper wire of length 1 m and diameter 3 mm

26. An ideal ammeter has ..... resistance.

(*i*) low (*ii*) infinite

(*iii*) zero (*iv*) high

27. The resistance of an ideal voltmeter is .....

(*i*) low (*ii*) infinite

(*iii*) zero (*iv*) high

28. To send 10% of the main current through a moving coil galvanometer of resistance 99 Ω, the shunt required is .....

(*i*) 11 Ω (*ii*) 9.9 Ω

(*iii*) 100 Ω (*iv*) 9 Ω

29. A voltmeter has a resistance of G ohms and range V volts. The value of resistance required in series to convert it into voltmeter of range nV is .....

(*i*) nG (*ii*) $\frac{G}{n}$

(*iii*) $\frac{G}{n-1}$ (*iv*) $(n-1)\,G$

30. An ammeter has a resistance of G ohms and range of I amperes. The value of resistance required in parallel to convert it into an ammeter of range nI is .....

(*i*) nG (*ii*) $(n-1)\,G$

(*iii*) $\frac{G}{n-1}$ (*iv*) $\frac{G}{n}$

Answers to Multiple-Choice Questions

1. (*i*)	**2.** (*ii*)	**3.** (*iii*)	**4.** (*i*)	**5.** (*ii*)
6. (*iii*)	**7.** (*iv*)	**8.** (*ii*)	**9.** (*i*)	**10.** (*iv*)
11. (*ii*)	**12.** (*iii*)	**13.** (*ii*)	**14.** (*i*)	**15.** (*ii*)
16. (*ii*)	**17.** (*iii*)	**18.** (*iv*)	**19.** (*ii*)	**20.** (*i*)
21. (*iii*)	**22.** (*iii*)	**23.** (*iv*)	**24.** (*ii*)	**25.** (*i*)
26. (*iii*)	**27.** (*ii*)	**28.** (*i*)	**29.** (*iv*)	**30.** (*iii*)

Chapter Review Topics

1. What is a multimeter ? How does it work ?
2. What type of measurements can be made with a multimeter ? Explain with suitable diagrams.
3. Briefly explain the advantages of 20 kΩ/volt multimeter as compared to a 10 kΩ/volt multimeter.
4. What are the applications of a multimeter ?
5. Discuss the advantages and disadvantages of a multimeter.
6. What is a *VTVM* ? Explain balanced bridge Type *VTVM* with a neat circuit diagram.
7. What are the applications of *VTVM* ?
8. Discuss the advantages and disadvantages of *VTVM*.
9. Briefly explain the differences between a *VTVM* and a multimeter.
10. Explain the construction and working of a cathode ray tube.
11. How will you make the following measurements with a *CRO* :
    (*i*) voltage (*ii*) frequency ?
12. Write short notes on the following :
    (*i*) Limitations of multimeter
    (*ii*) Advantages of oscilloscope
    (*iii*) Vacuum tube voltmeter
    (*iv*) Oscilloscope controls

Problems

1. A voltmeter is used to measure voltage across 20 kΩ resistor as shown in Fig. 24.25. What will be the voltage value if (*i*) voltmeter has infinite resistance (*ii*) voltmeter has a sensitivity of 1000 Ω per volt and reads 100 V full scale ? **[(*i*) 50 V (*ii*) 45 V]**

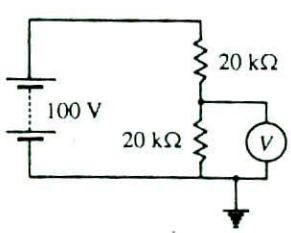


Fig. 24.25

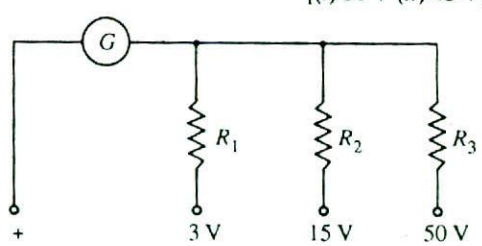


Fig. 24.26

2. The three range voltmeter is arranged as shown in Fig. 24.26. The ranges are 0 to 3 V, 0 to 15 V and 0 to 50 V as marked. If the full scale deflection current is 10 mA, what should be the values of R_1, R_2 and R_3 ? The resistance of the meter is 5 Ω. **[305 Ω, 1505 Ω, 5005 Ω]**
3. If the sensitivity of voltmeter in Fig. 24.25 is 500 Ω/volt (Full-scale reading being 100 V), what will be the reading of the voltmeter ? **[41.7 V]**

4. What is the lowest full-scale voltage that could be displayed with a 100 μA meter movement with an internal resistance of 150 Ω ? What would be the sensitivity of this meter in ohms per volt ?
[15 mV, 10,000 Ω/V]

5. If a 20,000 Ω/V meter with 5 kΩ internal resistance is used in an ohmmeter with a 3-V-battery, what internal resistance is required in the meter to produce proper zeroing? **[60 kΩ]**

Discussion Questions

1. Why is sensitivity of best multimeter not more than 20 kΩ per volt ?
2. Why do we generally prefer *VTVM* to multimeter for measurements in electronic circuits ?
3. Why does oscilloscope give more accurate measurements than a *VTVM* ?
4. What is the basic difference between vacuum tubes and cathode ray tube ?
5. How can a multimeter be used for continuity checking ?
6. Which would usually have more linear scales, dc or ac meters ?
7. Which is more sensitive, a 0 – 59 μA or a 0 – 1 mA meter ?
8. On a multirange ohmmeter, where is 0 Ω mark ?
9. What component prevents meter damage in a *VTVM*?
10. Could a 0 – 1 mA-movement 100 – V voltmeter and a 0 – 50 μA – movement 100 – V voltmeter be used in series across 125 V ?

25

Integrated Circuits

Introduction

The circuits discussed so far in the text consisted of separately manufactured components (*e.g.* resistors, capacitors, diodes, transistors *etc.*) joined by wires or plated conductors on printed boards. Such circuits are known as *discrete circuits* because each component added to the circuit is discrete (*i.e.* distinct or separate) from the others. Discrete circuits have two main disadvantages. Firstly, in a large circuit (*e.g.* TV circuit, computer circuit) there may be hundreds of components and consequently discrete assembly would occupy a large space. Secondly, there will be hundreds of soldered points posing a considerable problem of reliability. To meet these problems of space conservation and reliability, engineers started a drive for miniaturized circuits. This led to the development of micro-electronics in the late 1950*s*.

Micro-electronics is the branch of electronics engineering which deals with micro-circuits. A micro-circuit is simply a miniature assembly of electronic components. One type of such circuit is the *integrated circuit*, generally abbreviated as *IC*. An integrated circuit has various components such as resistors, capacitors, diodes, transistors etc. fabricated on a small semiconductor chip. How circuits containing hundreds of components are fabricated on a small semiconductor chip to produce an *IC* is a fascinating feat of micro-electronics. This has not only fulfilled the ever-increasing demand of industries for electronic equipment of smaller size, lighter weight and low power requirements, but it has also resulted in high degree of reliability. In this chapter, we shall focus our attention on the various aspects of integrated circuits.

25.1 Integrated Circuit

An **integrated circuit** *is one in which circuit components such as transistors, diodes, resistors, capacitors etc. are automatically part of a small semiconductor chip.*

An integrated circuit consists of a number of circuit components (*e.g.* transistors, diodes, resistors etc.) and their inter connections in a single small package to perform a complete electronic function. These components are formed and connected within a small chip of semi-conductor material. The following points are worth noting about integrated circuits :

(*i*) In an *IC*, the various components are automatically part of a small semi-conductor chip and the individual components cannot be removed or replaced. This is in contrast to

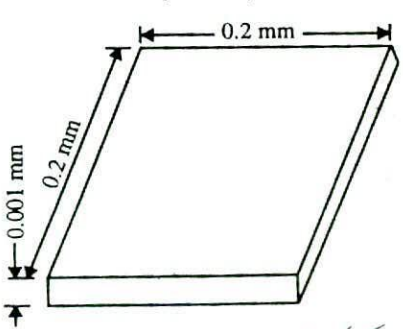


Fig. 25.1

discrete assembly in which individual components can be removed or replaced if necessary.

(*ii*) The size of an **IC* is extremely small. In fact, ICs are so small that you normally need a microscope to see the connections between the components. Fig. 25.1. shows a typical semi-conductor chip having dimensions 0.2 mm × 0.2 mm × 0.001 mm. It is possible to produce circuits containing many transistors, diodes, resistors etc on the surface of this small chip.

(*iii*) No components of an *IC* are seen to project above the surface of the chip. This is because all the components are formed within the chip.

25.2 Advantages and Disadvantages of Integrated Circuits

Integrated circuits free the equipment designer from the need to construct circuits with individual discrete components such as transistors, diodes, and resistors. With the exception of a few very simple circuits, the availability of a large number of low-cost integrated circuits have largely rendered discrete circuitry obsolete. It is, therefore, desirable to mention the significant advantages of integrated circuits over discrete circuits. However, integrated circuits have some disadvantages and continuous efforts are on to overcome them.

Advantages : Integrated circuits possess the following advantages over discrete circuits :

(*i*) Increased reliability due to lesser number of connections.

(*ii*) Extremely small size due to the fabrication of various circuit elements in a single chip of semi-conductor material.

(*iii*) Lesser weight and **space requirement due to miniaturized circuit.

(*iv*) Low power requirements.

(*v*) Greater ability to operate at extreme values of temperature.

(*vi*) Low cost because of simultaneous production of hundreds of alike circuits on a small semi-conductor wafer.

(*vii*) The circuit lay out is greatly simplified because integrated circuits are constrained to use minimum number of external connections.

Disadvantages : The disadvantages of integrated circuits are :

(*i*) If any component in an *IC* goes out of order, the whole *IC* has to be replaced by the new one.

(*ii*) In an *IC*, it is neither convenient nor economical to fabricate capacitances exceeding 30 *pF*. Therefore, for high values of capacitance, discrete components exterior to *IC* chip are connected.

(*iii*) It is not possible to fabricate inductors and transformers on the surface of semi-conductor chip. Therefore, these components are connected exterior to the semi-conductor chip.

(*iv*) It is not possible to produce high power *ICs* (greater than 10 W).

(*v*) There is a lack of flexibility in an IC *i.e.*, it is generally not possible to modify the parameters within which an integrated circuit will operate.

25.3 IC Classifications

Four basic types of constructions are employed in the manufacture of integrated circuits, namely ;

(*i*) mono-lithic (*ii*) thin-film (*iii*) thick-film (*iv*) hybrid.

Monolithic *ICs* are by far the most common type used in practice. Therefore, in this chapter we shall confine our attention to the construction of this type of *ICs* only. It may be worthwhile to

---

* Since it combines both active (*e.g.*, transistors, diodes etc) and passive elements (*e.g.*, resistors, capacitors etc.) in a monolithic structure, the complete unit is called an integrated circuit.

** Typically, this is about 10% of the space required by comparable discrete assembly.

mention here that regardless of the type of method used to fabricate active and passive components, the basic characteristics and circuit operation of an *IC* are the same as for any of their counterparts in a similar circuit using separate circuit components.

25.4 Making Monolithic IC

A **monolithic IC** *is one in which all circuit components and their inter-connections are formed on a single thin wafer called the substrate.*

The word monolithic is from Greek and means "one stone." The word is appropriate because all the components are part of one chip. Although we are mainly interested in using *ICs*, yet it is profitable to know something about their fabrication. The basic production processes for the monolithic *ICs* are as follow :

(*i*) ***p*-Substrate.** This is the first step in the making of an *IC*. A cylindrical *p*-type *silicon crystal is grown having typical dimensions 25 cm long and 2.5 cm diameter [See Fig. 25.2 (*i*)]. The crystal is then cut by a diamond saw into many thin wafers like Fig. 25.2 (*ii*), the typical thickness of the wafer being 200 μm. One side of wafer is polished to get rid of surface imperfections. This wafer is called the substrate. The *ICs* are produced on this wafer.

Fig. 25.2

(*ii*) **Epitaxial *n* layer.** The next step is to put the wafers in a diffusion furnace. A gas mixture of silicon atoms and pentavalent atoms is passed over the wafers. This forms a thin layer of *n*-type

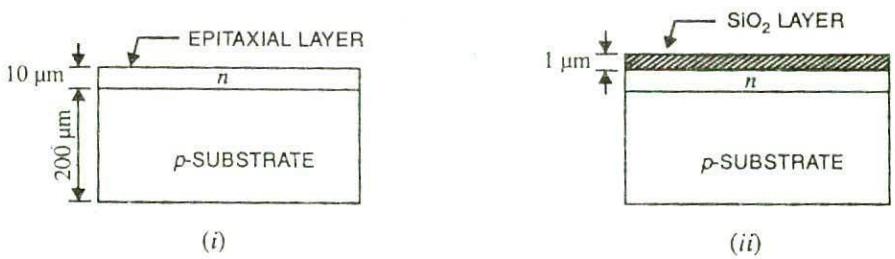


Fig. 25.3

semi-conductor on the heated surface of substrate [See Fig. 25.3 (*i*)]. This thin layer is called the ***epitaxial layer* and is about 10 μm thick. It is in this layer that the whole integrated circuit is formed.

(*iii*) **Insulating layer.** In order to prevent the contamination of the epitaxial layer, a thin SiO_2 layer about 1μm thick is deposited over the entire surface as shown in Fig. 25.3 (*ii*). This is achieved by passing pure oxygen over the epitaxial layer. The oxygen atoms combine with silicon atoms to

* Since silicon possesses characteristics which are best suited to *IC* manufacturing processes.

** The word "epitaxial" is derived from the Greek language and means arranged upon.

form a layer of silicon dioxide (SiO_2).

(*iv*) **Producing components.** By the process of *diffusion, appropriate materials are added to the substrate at specific locations to produce diodes, transistors, resistors and capacitors. The production of these components on the wafer is discussed in Art 25.5.

(*v*) **Etching.** Before any impurity is added to the substrate, the oxide layer (*i.e.* SiO_2 layer) is etched. The process of etching exposes the epitaxial layer and permits the production of desired components. The terminals are processed by etching the oxide layer at the desired locations.

(*vi*) **Chips.** In practice the wafer shown in Fig. 25.4 is divided into a large number of areas. Each of these areas will be a separate chip. The manufacturer produces hundreds of alike *ICs* on the wafer over each area. To separate the individual *ICs*, the wafer is divided into small chips by a process similar to glass cutting. This is illustrated in Fig. 25.4. It may be seen that hundreds of alike *ICs* can be produced from a small wafer. This simultaneous mass production is the reason for the low cost of integrated circuits.

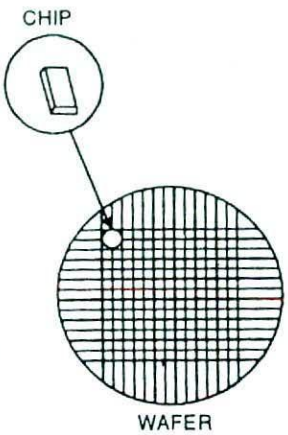


Fig. 25.4

After the chip is cut, it is bonded to its mounting and connections are made between the *IC* and external leads. The *IC* is then encapsulated to prevent it from becoming contaminated by the surrounding atmosphere.

25.5 Fabrication of Components on Monolithic IC

The notable feature of an *IC* is that it comprises a number of circuit elements inseparably associated in a single small package to perform a complete electronic function. This differs from discrete assembly where separately manufactured components are joined by wires. We shall now see how various circuit elements (*e.g.* diodes, transistors, resistors etc.) can be constructed in an *IC* form.

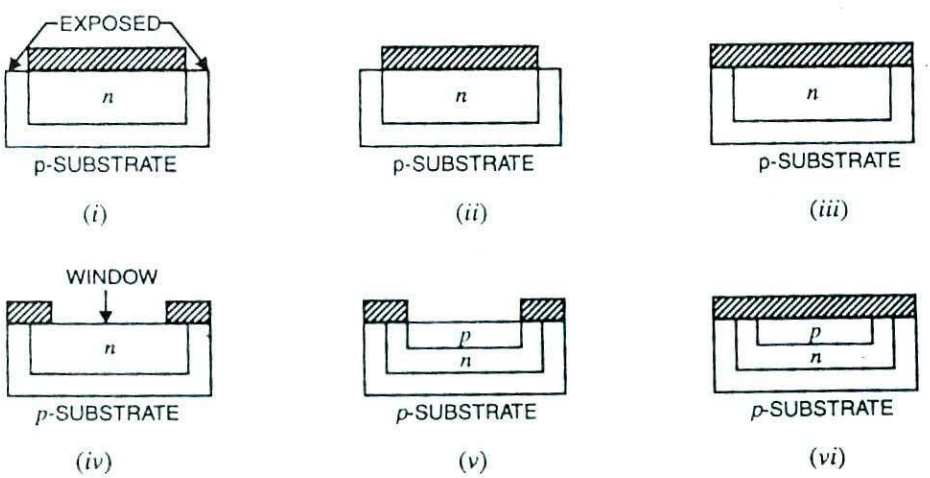


Fig. 25.5

(*i*) **Diodes.** One or more diodes are formed by diffusing one or more small *n*-type deposits at

* In *IC* construction, diffusion is the process of deliberately adding controlled impurities at specific locations of substrate by thermal processes.

appropriate locations on the substrate. Fig. 25.5 shows how a diode is formed on a portion of substrate of a monolithic *IC*. Part of SiO_2 layer is etched off, exposing the epitaxial layer as shown in Fig. 25.5 (*i*). The wafer is then put into a furnace and trivalent atoms are diffused into the epitaxial layer. The trivalent atoms change the exposed epitaxial layer from *n*-type semi-conductor to *p*-type. Thus we get an island of *n*-type material under the SiO_2 layer as shown in Fig. 25.5 (*ii*).

Next pure oxygen is passed over the wafer to form a complete SiO_2 layer as shown in Fig. 25.5 (*iii*). A hole is then etched at the centre of this layer ; thus exposing the *n*-epitaxial layer [See Fig. 25.5 (*iv*)]. This hole in SiO_2 layer is called a **window**. Now we pass trivalent atoms through the window. The trivalent atoms diffuse into the epitaxial layer to form an island of *p*-type material as shown in Fig. 25.5 (*v*). The SiO_2 layer is again formed on the wafer by blowing pure oxygen over the wafer [See Fig. 25.5 (*vi*)]. Thus a *p-n* junction diode is formed on the substrate.

Fig. 25.6

The last step is to attach the terminals. For this purpose, we etch the SiO_2 layer at the desired locations as shown in Fig 25.6 (*i*). By depositing metal at these locations, we make electrical contact with the anode and cathode of the integrated diode. Fig. 25.6 (*ii*) shows the electrical circuit of the diode.

(*ii*) **Transistors.** Transistors are formed by using the same principle as for diodes. Fig. 25.7 shows how a transistor is formed on a portion of the substrate of a monolithic *IC*. For this purpose, the steps used for fabricating the diode are carried out upto the point where *p* island has been formed and sealed off [See Fig. 25.5 (*vi*) above]. This Fig. is repeated as Fig. 25.7 (*i*) and shall be taken as the starting point in order to avoid repetition.

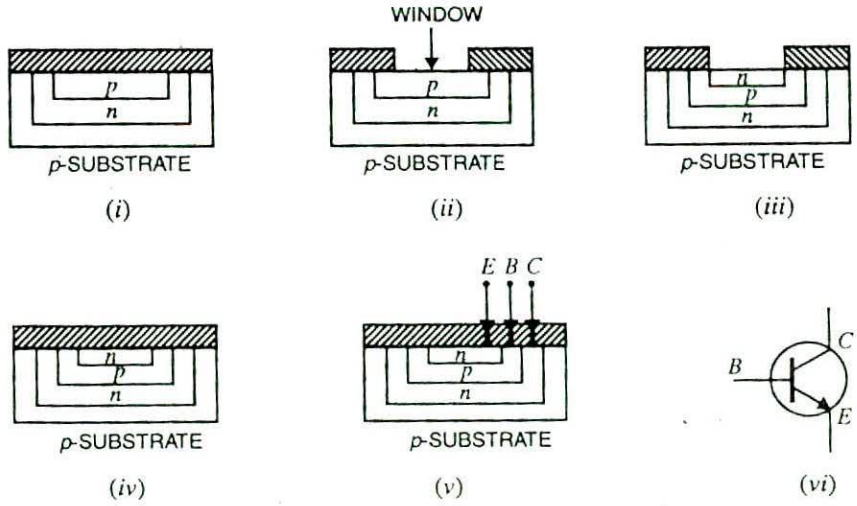


Fig. 25.7

A window is now formed at the centre of SiO_2 layer, thus exposing the *p*-epitaxial layer as shown in Fig. 25.7(*ii*). Then we pass pentavalent atoms through the window. The pentavalent atoms diffuse into the epitaxial layer to form an island of *n*-type material as shown in Fig. 25.7 (*iii*). The SiO_2 layer is re-formed over the wafer by passing pure oxygen [See Fig. 25.7 (*iv*)]. The terminals are processed by etching the SiO_2 layer at appropriate locations and depositing the metal at these locations as shown in Fig. 25.7 (*v*). In this way, we get the integrated transistor. Fig. 25.7 (*vi*) shows the electrical circuit of a transistor.

(*iii*) **Resistors.** Fig. 25.8 shows how a resistor is formed on a portion of the substrate of a monolithic *IC*. For this purpose, the steps used for fabricating diode are carried out upto the point where *n* island has been formed and sealed off [Refer back to Fig. 25.5 (*iii*)]. This figure is repeated as Fig 25.8 (*i*) and shall be taken as the starting point in order to avoid repetition.

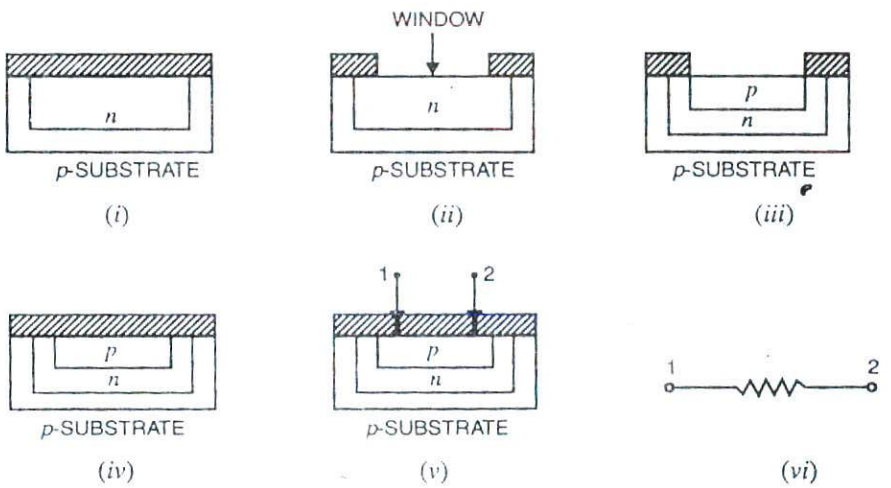


Fig. 25.8

A window is now formed at the centre of SiO_2 layer, thus exposing the *n*-epitaxial layer as shown in Fig. 25.8 (*ii*). Then we diffuse a *p*-type material into the *n*-type area as shown in Fig. 25.8 (*iii*). The SiO_2 layer is re-formed over the wafer by passing pure oxygen [See Fig. 25.8 (*iv*)]. The terminals are processed by etching SiO_2 layer at two points above the *p* island and depositing the metal at these locations [See Fig. 25.8 (*v*)]. In this way, we get an integrated resistor. Fig. 25.8 (*vi*) shows the electrical circuit of a resistor.

The value of resistor is determined by the material, its length and area of cross-section. The high-resistance resistors are long and narrow while low-resistance resistors are short and of greater cross-section.

(*iv*) **Capacitors.** Fig. 25.9 shows the process of fabricating a capacitor in the monolithic *IC*. The first step is to diffuse an *n*-type material into the substrate which forms one plate of the capacitor as shown in Fig. 25.9 (*i*). Then SiO_2 layer is re-formed over the wafer by passing pure oxygen as shown in Fig. 25.9 (*ii*).

The SiO_2 layer formed acts as the dielectric of the capacitor. The oxide layer is etched and terminal 1 is added as shown in Fig. 25.9 (*iii*). Next a large (compared to the electrode at terminal 1) metallic electrode is deposited on the SiO_2 layer and forms the second plate of the capacitor. The oxide layer is etched and terminal 2 is added. This gives an integrated capacitor. The value of capacitor formed depends upon the dielectric constant of SiO_2 layer, thickness of SiO_2 layer and the

area of corss-section of the smaller of the two electrodes.

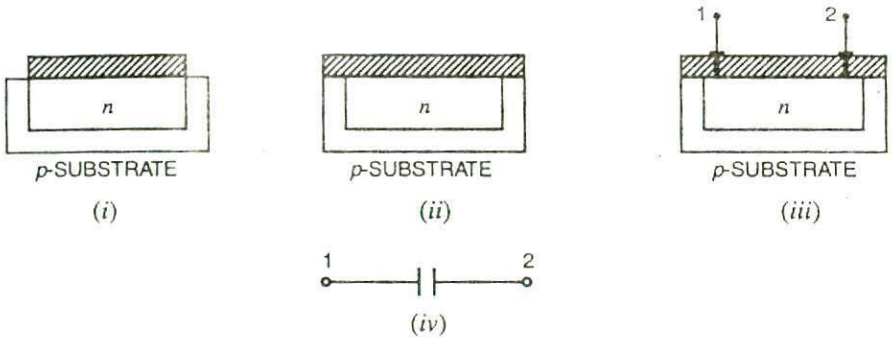


Fig. 25.9

25.6 Simple Monolithic *ICs*

It has been seen above that individual components can be integrated in a monolithic *IC*. We shall now see how an electronic circuit comprising different components is produced in an *IC* form. The key point to keep in mind is that regardless of the complexity of the circuit, it is mainly a process of etching windows, forming *p* and *n* islands, and connecting the integrated components.

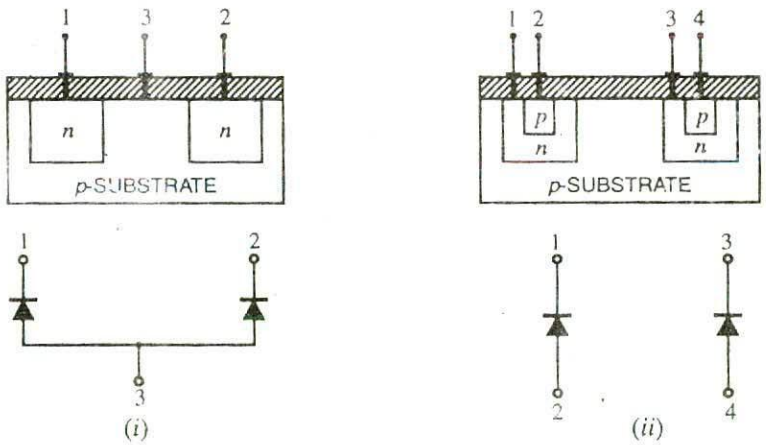


Fig. 25.10

(*i*) **Two-diode IC.** Fig. 25.10 (*i*) shows a two-diode *IC* with a common anode whereas Fig. 25.10 (*ii*) shows a two-diode *IC* with individual anode.

Two points are worth noting. Firstly, any circuit [like the one shown in Fig 25.10 (*i*) or Fig 25.10 (*ii*)] is not integrated individually ; rather hundreds of alike circuits are simultaneously fabricated on a wafer. The wafer is then cut into chips so that each chip area represents one circuit. This is the key factor for low cost of *ICs* and is exerting considerable influence on electronics engineers to switch over to *IC* technology. Secondly, *ICs* are usually not as simple as shown in Fig. 25.10. In fact, actual *ICs* contain a large number of components.

(*ii*) **Another simple IC.** Fig.25.11 shows an *IC* consisting of a capacitor, resistor, diode and transistor connected in series. The interconnection of the circuit elements is accomplished by extending the metallic deposits from terminal to terminal of adjacent components.

It is interesting to see that *p* substrate isolates the integrated components from each other. Thus

referring to Fig. 25.11, depletion layers exist between p substrate and the four n islands touching it. As the depletion layers have virtually no current carriers, therefore, the integrated components are insulated from each other.

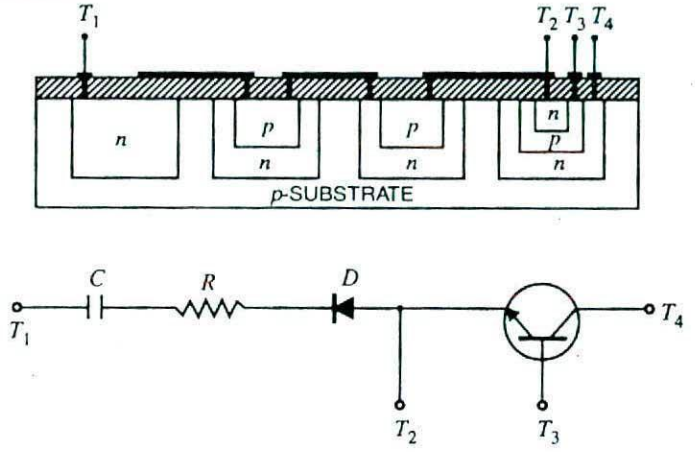


Fig. 25.11

25.7 *IC* Packings

In order to protect *ICs* from external environment and to provide mechanical protection, various forms of encapsulation are used for integrated circuits. Just as with semi-conductor devices, *IC* packages are of two types *viz.*

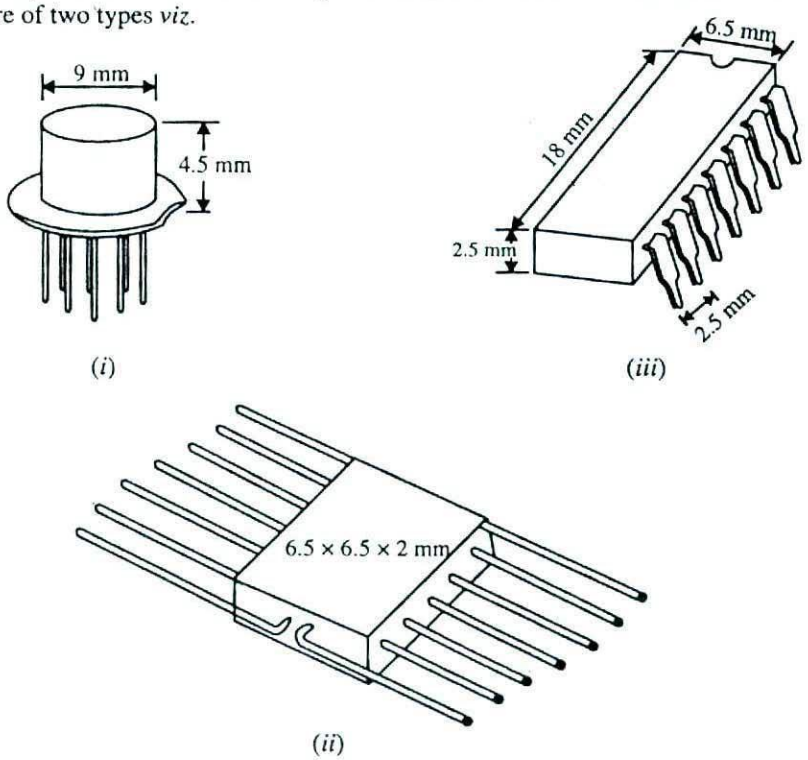


Fig. 25.12

(*i*) hermatic (metal or ceramic with glass) (*ii*) non-hermatic (plastics)

Plastics are cheaper than hermatic but are still not regarded as satisfactory in extremes of temperature and humidity. Although *ICs* appeared in the market several years ago, yet the standardisation of packages started only in the recent years. The three most popular types of *IC* packages are shown in Fig. 25.12.

(*i*) Fig. 25.12 (*i*) shows *TO-5 package** which resembles a small signal transistor in both appearance and size but differs in that it has either 8, 10 or 12 pigtail-type leads. The close leads spacing and the difficulty of removal from a printed circuit board has diminished the popularity of this package with the users.

(*ii*) Fig. 25.12 (*ii*) shows a *flat pack* container with 14 leads, seven on each side.

(*iii*) Fig. 25.12 (*iii*) shows the *dual-in-line* (**DIL**) pack in 14-lead version. The 14-pin DIL is the most popular form and has seven connecting pairs per side. The pairs of pins of this pack are in line with one another, the pins being 2.5 mm apart to allow IC to be fitted directly into the standard printed circuit boards.

25.8 *IC* Symbols

In general, no standard symbols exist for *ICs*. Often the circuit diagram merely shows a block with numbered terminals. However, sometimes standard symbols are used for operational amplifiers or digital logic gates. Some of the symbols used with *ICs* are shown below.

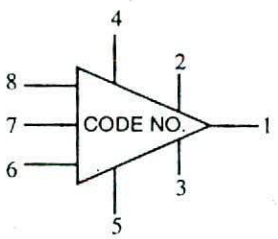


Fig. 25.13

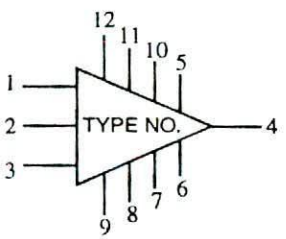


Fig. 25.14

Fig. 25.13 shows the symbol of an *IC r-f* amplifier containing 3 transistors, 3 resistors and 8 terminals. Similarly, Fig. 25.14 shows an *IC* audio amplifier which contain 6 transistors 2 diodes, 17 resistor and has 12 terminals.

25.9 Scale of Integration

An *IC* chip may contain as large as 100,000 semiconductor devices or other components. The relative number of these components within the chip is given by referring to its scale of integration. The following terminology is commonly used.

Scale of integration	Abbreviation	Number of components
Small	**SSI	1 to 20
Medium	MSI	20 to 100
Large	LSI	100 to 1000
Very large	VLSI	1000 to 10,000
Super large	SLSI	10,000 to 100,000

* This was the earliest type of package and it was natural for the semi-conductor manufactures to use modified transistor cases.

** SSI stands for small scale integration

25.10 Some Circuits Using ICs

Integrated circuits are fairly complex because they contain a large number of circuit components within a small semiconductor chip. While studying circuits using *ICs*, we are more concerned with the external connections to the *IC* rather than what is actually going on inside.

(*i*) **IC Fixed 5-volt Voltage Regulator.** The *IC* voltage regulator is a device that is used to hold the output voltage from a dc power supply constant as the input voltage or load current changes. For example, LM 309 (fixed postive) provides a + 5 V d.c. output. This regulator is frequently used in digital circuits. Fig. 25.15 shows the circuit of the voltage regulator using LM 309. It is a three terminal device with terminals labelled as input, output and ground terminal. It provides a fixed 5 V between the output and ground terminals.

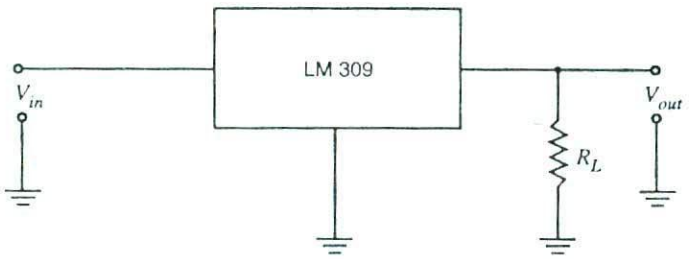


Fig. 25.15

The LM 309 has a number of advantages over the zener diode. First, it is much more accurate than the zener diode. Secondly, there is built-in overload protection. The LM 309 also has overheating protection. If the internal temperature becomes excessive, it shuts off until the temperature is reduced, at which point it will start up again.

(*ii*) **IC Adjustable Voltage Regulator.** Sometimes, we want a voltage regulator whose voltage we can vary. An example of such a voltage regulator is LM 317 whose schematic diagram is shown in Fig. 25.16. By varying the value of R_2, the output voltage of the regulator can be adjusted. The following equation is used to determine the regulated d.c. output voltage for an LM 317 regulator circuit.

$$V_{out} = 1.25\left(\frac{R_2}{R_1} + 1\right)$$

Example 25.1. *In LM 317 voltage regulator shown in Fig. 25.16, R_2 is adjusted to 2.4 kΩ. If the value of R_1 is 240 Ω, determine the regulated d.c. output voltage for the circuit.*

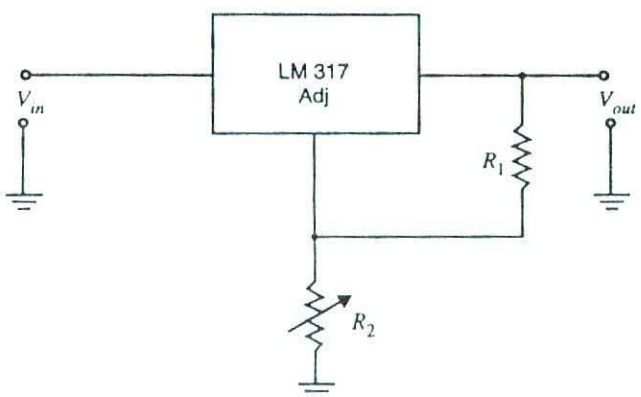


Fig. 25.16

Solution.
$$V_{out} = 1.25\left(\frac{R_2}{R_1}+1\right)$$
$$= 1.25\left(\frac{2.4\ \text{k}\Omega}{240\ \Omega}+1\right) = 13.75\ \text{V}$$

Multiple-Choice Questions

1. An *IC* has ..... size.
   (*i*) very large
   (*ii*) large
   (*iii*) extremely small
   (*iv*) none of the above
2. *ICs* are generally made of .....
   (*i*) silicon (*ii*) germanium
   (*iii*) copper (*iv*) none of the above
3. ..... *ICs* are the most commonly used.
   (*i*) thin film (*ii*) monolithic
   (*iii*) hybrid (*iv*) none of the above
4. The most popular form of *IC*package is .....
   (*i*) DIL (*ii*) flatpack
   (*iii*) TO-5 (*iv*) none of the above
5. ..... cannot be fabricated on an *IC*.
   (*i*) transistors
   (*ii*) diodes
   (*iii*) resistors
   (*iv*) large inductors and transformers
6. An audio amplifier is an example of .....
   (*i*) digital *IC*
   (*ii*) linear *IC*
   (*iii*) both digitial and linear *IC*
   (*iv*) none of the above
7. The active components in an *IC* are .....
   (*i*) resistors
   (*ii*) capacitors
   (*iii*) transistors and diodes
   (*iv*) none of the above
8. We use ..... *ICs* in computers.
   (*i*) digital
   (*ii*) linear
   (*iii*) both digital and linear
   (*iv*) none of the above
9. The SiO_2 layer in an *IC* acts as .....
   (*i*) a resistor
   (*ii*) an insulating layer
   (*iii*) mechanical output
   (*iv*) none of the above
10. *ICs* are used in ....
    (*i*) linear devices only
    (*ii*) digital devices only
    (*iii*) both linear and digital devices
    (*iv*) none of the above
11. A transistor takes ..... inductor on a silicon *IC* chip.
    (*i*) less space than
    (*ii*) more space than
    (*iii*) same space as
    (*iv*) none of the above
12. The most popular types of *ICs* are .....
    (*i*) thin-film (*ii*) hybrid
    (*iii*) thick-film (*iv*) monolithic
13. Digital *ICs* process .....
    (*i*) linear signals only
    (*ii*) digital signals only
    (*iii*) both digital and linear signals
    (*iv*) none of the above
14. Operational amplifiers use .....
    (*i*) linear *ICs*
    (*ii*) digital *ICs*
    (*iii*) both linear and digital *ICs*
    (*iv*) none of the above
15. Which of the following is most difficult to fabircate in an *IC* ?
    (*i*) diode (*ii*) transistor
    (*iii*) *FET* (*iv*) capacitor

Answers to Multiple-Choice Questions

1. (*iii*)	**2.** (*i*)	**3.** (*ii*)	**4.** (*ii*)	**5.** (*iv*)
6. (*ii*)	**7.** (*iii*)	**8.** (*i*)	**9.** (*ii*)	**10.** (*iii*)
11. (*i*)	**12.** (*iv*)	**13.** (*iii*)	**14.** (*ii*)	**15.** (*iv*)

Chapter Review Topics

1. What is an integrated circuit ? Discuss the relative advantages and disadvantages of *ICs* over discrete assembly.
2. How will you make a monolithic *IC* ?
3. Explain how (*i*) a diode (*ii*) a transistor (*iii*) a resistor and (*iv*) a capacitor can be constructed in a monolithic integrated circuit.
4. Explain how electronic circuit consisting of different components can be constructed in a monolithic *IC*.
5. Write short notes on the following :

   (*i*) Epitaxial layer (*ii*) *IC* packages (*iii*) *IC* symbols

Discussion Questions

1. Why are *ICs* so cheap ?
2. Why do *ICs* require low power ?
3. Why cannot we produce *ICs* of greater power ?
4. Why are *ICs* more reliable than discrete assembly ?
5. Why is DIL *IC* package the most popular ?

26

Hybrid Parameters

Introduction

In order to predict the behaviour of a small-signal transistor amplifier, it is important to know its operating characteristics *e.g.*, input impedance, output impedance, voltage gain *etc*. In the text so far, these characteristics were determined by using *β and circuit resistance values. This method of analysis has two principal advantages. Firstly, the values of circuit components are readily available and secondly the procedure followed is easily understood. However, the major drawback of this method is that accurate results cannot be obtained. It is because the input and output circuits of a transistor amplifier are not completely independent. For example, output current is affected by the value of load resistance rather than being constant at the value βI_b. Similarly, output voltage has an effect on the input circuit so that changes in the output cause changes in the input.

One of the methods that takes into account all the effects in a transistor amplifier is the hybrid parameter approach. In this method, four parameters (one measured in ohm, one in mho, two dimensionless) of a transistor are measured experimentally. These are called hybrid or *h* parameters of the transistor. Once these parameters for a transistor are known, formulas can be developed for input impedance, voltage gain etc.in terms of *h* parameters. There are two main reasons for using *h* parameter method in describing the characteristics of a transistor. Firstly, it yields exact results because the inter-effects of input and output circuits are taken into account. Secondly, these parameters can be measured very easily. To begin with, we shall apply *h* parameter approach to general circuits and then extend it to transistor amplifiers.

26.1 Hybrid Parameters

*Every **linear circuit having input and output terminals can be analysed by four parameters (one measured in ohm, one in mho and two dimensionless) called* **hybrid** *or* ***h*** **Parameters.**

Hybrid means "mixed". Since these parameters have mixed dimensions, they are called hybrid parameters. Consider a linear circuit shown in Fig. 26.1. This circuit has input voltage and current labelled v_1 and i_1. This circuit also has output voltage and current labelled v_2 and i_2. Note that both input and output currents (i_1 and i_2) are assumed to flow *into* the box ; input and output voltages (v_1 and v_2) are assumed *positive* from the upper to the lower terminals. These are standard conventions and do not necessarily correspond to the actual directions and polarities. When we analyse circuits in

* Since transistor is generally connected in *CE* arrangement, current amplification factor β is mentioned here.

** A linear circuit is one in which resistances, inductances and capacitances remain fixed when voltage across them changes.

which the voltages are of opposite polarity or where the currents flow out of the box, we simply treat these voltages and currents as negative quantities.

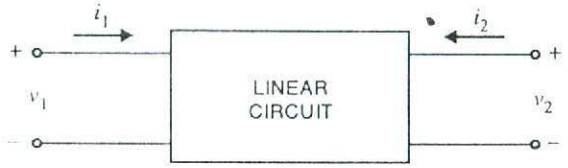


Fig. 26.1

It can be proved by advanced circuit theory that voltages and currents in Fig. 26.1 can be related by the following sets of equations :

$$v_1 = h_{11}\, i_1 + h_{12}\, v_2 \quad ...(i)$$

$$i_2 = h_{21}\, i_1 + h_{22}\, v_2 \quad ...(ii)$$

In these equations, the *h*s are fixed constants for a given circuit and are called *h* parameters. Once these parameters are known, we can use equations (*i*) and (*ii*) to find the voltages and currents in the circuit. If we look at *eq.*(*i*), it is clear that *h_{11} has the dimension of ohm and h_{12} is dimensionless. Similarly, from *eq.* (*ii*), h_{21} is dimensionless and h_{22} has the dimension of mho. The following points may be noted about *h* parameters :

(*i*) Every linear circuit has four *h* parameters ; one having dimension of ohm, one having dimension of mho and two dimensionless.

(*ii*) The *h* parameters of a given circuit are constant. If we change the circuit, *h* parameters would also change.

(*iii*) Suppose that in a particular linear circuit, voltages and currents are related as under:

$$v_1 = 10 i_1 + 6 v_2$$

$$i_2 = 4 i_1 + 3 v_2$$

Here we can say that the circuit has *h* parameters given by $h_{11} = 10\ \Omega$; $h_{12} = 6$; $h_{21} = 4$ and $h_{22} = 3$ ℧.

26.2 Determination of h Parameters

The major reason for the use of *h* parameters is the relative ease with which they can be measured. The *h* parameters of a circuit shown in Fig. 26.1 can be found out as under :

(*i*) If we short-circuit the output terminals (See Fig. 26.2), we can say that output voltage $v_2 = 0$. Putting $v_2 = 0$ in equations (*i*) and (*ii*), we get,

$$v_1 = h_{11}\, i_1 + h_{12} \times 0$$

$$i_2 = h_{21}\, i_1 + h_{22} \times 0$$

$$\therefore \quad h_{11} = \frac{v_1}{i_1} \quad \text{for } v_2 = 0 \textit{ i.e.} \text{ output shorted}$$

$$\text{and} \quad h_{21} = \frac{i_2}{i_1} \quad \text{for } v_2 = 0 \textit{ i.e.} \text{ output shorted}$$

Let us now turn to the physical meaning of h_{11} and h_{21} . Since h_{11} is a ratio of voltage and current (*i.e.* v_1/i_1), it is an impedance and is called ** "*input impedance with output shorted*". Similarly, h_{21}

* The two parts on the R.H.S. of *eq.* (*i*) must have the unit of voltage. Since current (amperes) must be multiplied by resistance (ohms) to get voltage (volts), h_{11} should have the dimension of resistance *i.e.* ohms.

** Note that v_1 is the input voltage and i_1 is the input current. Hence v_1/i_1 is given the name input impedance.

is the ratio of output and input current (*i.e.*, i_2/i_1), it will be dimensionless and is called "*current gain with output shorted*".

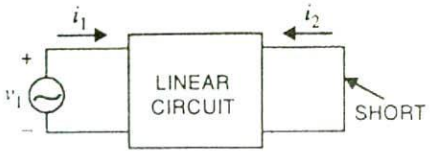


Fig. 26.2

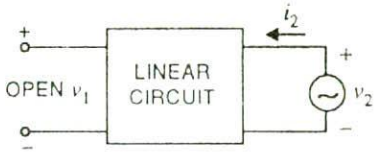


Fig. 26.3

(*ii*) The other two *h* parameters (*viz* h_{12} and h_{22}) can be found by making $i_1 = 0$. This can be done by the arrangement shown in Fig. 26.3. Here, we drive the output terminals with voltage v_2, keeping the input terminals open. With this set up, $i_1 = 0$ and the equations become:

$$v_1 = h_{11} \times 0 + h_{12}\, v_2$$

$$i_2 = h_{21} \times 0 + h_{22}\, v_2$$

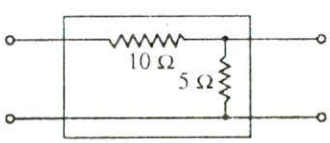
$$\therefore \quad h_{12} = \frac{v_1}{v_2} \quad \text{for } i_1 = 0 \textit{ i.e.} \text{ input open}$$

and

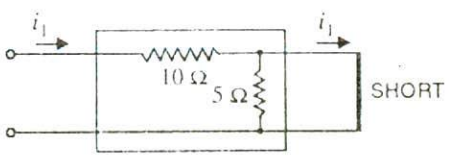
$$h_{22} = \frac{i_2}{v_2} \quad \text{for } i_1 = 0 \textit{ i.e.} \text{ input open}$$

Since h_{12} is a ratio of input and output voltages (*i.e.* v_1/v_2), it is dimensionless and is called "*voltage feedback ratio with input terminals open*". Similarly, h_{22} is a ratio of output current and output voltage (*i.e.* i_2/v_2), it will be admittance and is called *output admittance with input terminals open.*

Example. 26.1. *Find the h parameters of the circuit shown in Fig. 26.4 (i).*



(*i*)



(*ii*)

Fig. 26.4

Solution. The *h* parameters of the circuit shown in Fig. 26.4 (*i*) can be found as under :

To find h_{11} and h_{21}, short - circuit the output terminals as shown in Fig. 26.4 (*ii*). It is clear that input impedance of the circuit is 10 Ω because 5 Ω resistance is shorted out.

$$\therefore \quad h_{11} = \mathbf{10\ \Omega}$$

Now current i_1 flowing into the box will flow through 10 Ω resistor and then through the shorted path as shown. It may be noted that in our discussion, i_2 is the output current flowing into the box. Since output current in Fig. 26.4 (*ii*) is actually flowing out of the box, i_2 is negative *i.e.*,

$$i_2 = -i_1$$

$$\therefore \quad h_{21} = \frac{i_2}{i_1} = \frac{-i_1}{i_1} = -1$$

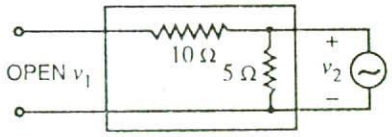


Fig. 26.4 (*iii*)

To find h_{12} and h_{22}, make the arrangement as shown in Fig. 26.4 (*iii*). Here we are driving the output terminals with a voltage v_2. This sets up a current i_2. Note that input terminals are open. Under this condition, there will be no current in 10Ω resistor and, therefore, there can be no voltage drop across it. Consequently, all the voltage appears across input terminals *i.e.*

$$v_1 = v_2$$

$$\therefore \qquad h_{12} = \frac{v_1}{v_2} = \frac{v_2}{v_2} = \mathbf{1}$$

Now the output impedance looking into the output terminals with input terminals open is simply 5 Ω. Then h_{22} will be the reciprocal of it because h_{22} is the output admittance with input terminals open.

$$\therefore \qquad h_{22} = 1/5 = \mathbf{0.2\ \text{℧}}$$

The h parameters of the circuit are :

$$h_{11} = 10\ \Omega;\ h_{21} = -1$$
$$h_{12} = 1;\ h_{22} = 0.2\ \text{℧}$$

It may be mentioned here that in practice, dimensions are not written with h parameters. It is because it is understood that h_{11} is always in ohms, h_{12} and h_{21} are dimensionless and h_{22} is in mhos.

Example 26.2. *Find the h parameters of the circuit shown in Fig. 26.5 (i).*

(*i*) **Fig. 26.5** (*ii*)

Solution. First of all imagine that output terminals are short-circuited as shown in Fig. 25.6 (*ii*). The input impedance under this condition is the parameter h_{11}.

Obviously, $h_{11} = 4 + 4 \| 4$

$$= 4 + \frac{4 \times 4}{4 + 4} = \mathbf{6\ \Omega}$$

Now the input current i_1 in Fig. 26.5 (*ii*) will divide equally at the junction of 4 Ω resistors so that output current is $i_1/2$ *i.e.*

$$i_2 = -i_1/2 = -0.5\, i_1$$

$$\therefore \qquad h_{21} = \frac{i_2}{i_1} = \frac{-0.5\, i_1}{i_1} = \mathbf{-0.5}$$

In order to find h_{12} and h_{22}, imagine the arrangement as shown in Fig. 26.5 (*iii*). Here we are driving the output terminals with voltage v_2, keeping the input terminals open. Under this condition, any voltage v_2 applied to the output will divide by a factor 2 *i.e.*

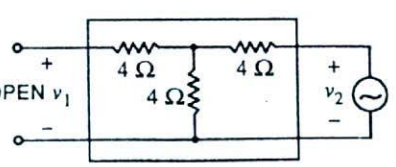


Fig. 26.5 (*iii*)

$$v_1 = \frac{v_2}{2} = 0.5\, v_2$$

$$\therefore \qquad h_{12} = \frac{v_1}{v_2} = \frac{0.5\, v_2}{v_2} = \mathbf{0.5}$$

Now the output impedance looking into the output terminals with input terminals open is simply 8 Ω. Then h_{22} will be the reciprocal of this *i.e.*

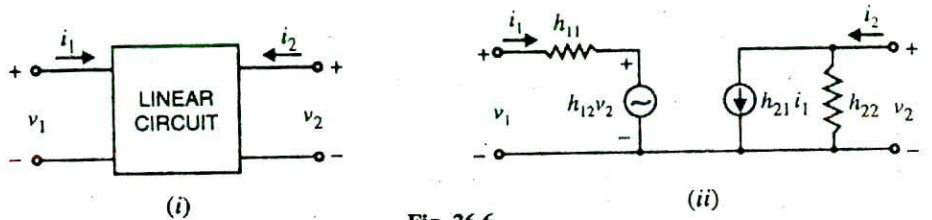
$$h_{22} = \frac{1}{8} = \mathbf{0.125\ \text{℧}}$$

26.3 h Parameter Equivalent Circuit

Fig. 26.6 (*i*) shows a linear circuit. It is required to draw the *h* parameter equivalent circuit of Fig. 26.6 (*i*). We know that voltages and current of the circuit in Fig. 26.6 (*i*) can be expressed in terms of *h* parameters as under :

$$v_1 = h_{11}\, i_1 + h_{12}\, v_2 \quad ...(i)$$

$$i_2 = h_{21}\, i_1 + h_{22}\, v_2 \quad ...(ii)$$



(*i*) (*ii*)

Fig. 26.6

Fig. 26.6 (*ii*) shows *h* parameter equivalent circuit of Fig. 26.6 (*i*) and is derived from equations (*i*) and (*ii*). The *input circuit* appears as a resistance h_{11} in series with a voltage generator $h_{12}\, v_2$. This circuit is derived from equation (*i*). The *output circuit* involves two components ; a current generator $h_{21}\, i_1$ and shunt resistance h_{22} and is derived from equation (*ii*). The following points are worth noting about the *h* parameter equivalent circuit [See Fig. 26.6 (*ii*)] :

(*i*) This circuit is called hybrid equivalent because its input portion is a Thevenin equivalent, or voltage generator with series resistance, while output side is Norton equivalent, or current generator with shunt resistance. Thus it is a mixture or a hybrid. The symbol '*h*' is simply the abbreviation of the word hybrid (hybrid means "mixed").

(*ii*) The different hybrid parameters are distinguished by different number subscripts. The notation shown in Fig. 26.6 (*ii*) is used in general circuit analysis. The first number designates the circuit in which the effect takes place and the second number designates the circuit from which the effect comes. For instance, h_{21} is the "short-circuit forward current gain" or the ratio of the current in the output (*circuit* 2) to the current in the input (*circuit* 1).

(*iii*) The equivalent circuit of Fig. 26.6 (*ii*) is extremely useful for two main reasons. First, it isolates the input and output circuits, their interaction being accounted for by the two controlled sources. Thus, the effect of output upon input is represented by the equivalent voltage generator $h_{12}v_2$ and its value depends upon output voltage. Similarly, the effect of input upon output is represented by current generator $h_{21}i_1$ and its value depends upon input current. Secondly, the two parts of the circuit are in a form which makes it simple to take into account source and load circuits.

26.4 Performance of a Linear Circuit in h Parameters

We have already seen that any linear circuit with input and output has a set of *h* parameters. We shall now develop formulas for input impedance, current gain, voltage gain etc.of a linear circuit in terms of *h* parameters.

(*i*) **Input impedance.** Consider a linear circuit with a load resistance r_L across its terminals as shown in Fig. 26.7. The input impedance Z_{in} of this circuit is the ratio of input voltage to input current *i.e.*

$$Z_{in} = \frac{v_1}{i_1}$$

Now $v_1 = h_{11}\, i_1 + h_{12}\, v_2$ in terms of *h* parameters. Substituting the value of v_1 in the above expression, we get,

$$Z_{in} = \frac{h_{11} i_1 + h_{12} v_2}{i_1} = h_{11} + \frac{h_{12} v_2}{i_1} \qquad ...(i)$$

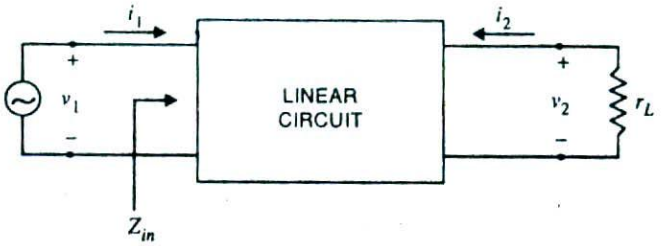


Fig. 26.7

Now, $i_2 = h_{21}\, i_1 + h_{22}\, v_2$ in terms of h parameters. Further from Fig. 26.7, it is clear that $i_2 = -v_2/r_L$. The minus sign is used here because the actual load current is opposite to the direction of i_2.

$$\therefore \quad \frac{-v_2}{r_L} = h_{21}\, i_1 + h_{22}\, v_2 \qquad \left[\because i_2 = \frac{-v_2}{r_L}\right]$$

or
$$-h_{21}\, i_1 = h_{22}\, v_2 + \frac{v_2}{r_L} = v_2\left(h_{22} + \frac{1}{r_L}\right)$$

$$\therefore \quad \frac{v_2}{i_1} = \frac{-h_{21}}{h_{22} + \frac{1}{r_L}} \qquad ...(ii)$$

Substituting the value of v_2/i_1 from exp. (*ii*) into exp. (*i*), we get,

$$\boldsymbol{Z_{in} = h_{11} - \frac{h_{12}\, h_{21}}{h_{22} + \frac{1}{r_L}}} \qquad ...(iii)$$

This is the expression for input impedance of a linear circuit in terms of h parameters and load connected to the output terminals. If either h_{12} or r_L is very small, the second term in exp. (*iii*) can be neglected and input impedance becomes :

$$\boldsymbol{Z_{in} \simeq h_{11}}$$

(*ii*) **Current Gain.** Referring to Fig. 26.7, the current gain A_i of the circuit is given by :

$$A_i = \frac{i_2}{i_1}$$

Now $\quad i_2 = h_{21}\, i_1 + h_{22}\, v_2$

and $\quad v_2 = -i_2\, r_L$

$\therefore \quad i_2 = h_{21}\, i_1 - h_{22}\, i_2\, r_L$

or $\quad i_2 (1 + h_{22}\, r_L) = h_{21}\, i_1$

or $\quad \frac{i_2}{i_1} = \frac{h_{21}}{1 + h_{22}\, r_L}$

But $i_2/i_1 = A_i$, the current gain of the circuit.

$$\therefore \quad \boldsymbol{A_i = \frac{h_{21}}{1 + h_{22}\, r_L}}$$

If $h_{22}\, r_L << 1$, then $A_i \simeq h_{21}$.

The expression $A_i \simeq h_{21}$ is often useful. To say that $h_{22}\, r_L << 1$ is the same as saying that

$r_L << 1/h_{22}$. This occurs when r_L is much smaller than the output resistance ($1/h_{22}$), shunting $h_{21}\, i_1$ generator. Under such condition, most of the generator current bypasses the circuit output resistance in favour of r_L. This means that $i_2 \simeq h_{21}\, i_1$ or $i_2/i_1 \simeq h_{21}$.

(*iii*) **Voltage gain.** Referring back to Fig. 26.7, the voltage gain of the circuit is given by;

$$A_v = \frac{v_2}{v_1}$$

$$= \frac{v_2}{i_1 Z_{in}} \qquad (\because v_1 = i_1 Z_{in}) \qquad ...(iv)$$

While developing expression for input impedance, we found that :

$$\frac{v_2}{i_1} = \frac{-h_{21}}{h_{22} + \frac{1}{r_L}}$$

Substituting the value of v_2/i_1 in exp. (*iv*), we get,

$$A_v = \frac{-h_{21}}{Z_{in}\left(h_{22} + \frac{1}{r_L}\right)}$$

Example 26.3. *Find the (i) input impedance and (ii) voltage gain for the circuit shown in Fig. 26.8.*

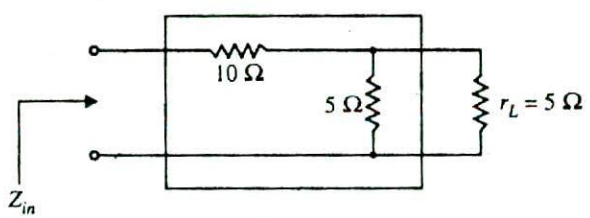


Fig. 26.8

Solution. The *h* parameters of the circuit inside the box are the same as those calculated in example 26.1. *i.e.*

$$h_{11} = 10; \qquad h_{21} = -1$$
$$h_{12} = 1 \quad \text{and} \quad h_{22} = 0.2$$

(*i*) Input impedance is given by;

$$Z_{in} = h_{11} - \frac{h_{12}\, h_{21}}{h_{22} + \frac{1}{r_L}} = 10 - \frac{1 \times -1}{0.2 + \frac{1}{5}}$$

$$= 10 + 2.5 = \mathbf{12.5\ W}$$

By inspection, we can see that input impedance is equal to 10 W plus two 5 W resistances in parallel *i.e.*

$$Z_{in} = 10 + 5 \parallel 5$$

$$= 10 + \frac{5 \times 5}{5 + 5} = 12.5\ \text{W}$$

(*ii*) Voltage gain, $A_v = \dfrac{-h_{21}}{Z_{in}\left(h_{22} + \frac{1}{r_L}\right)} = \dfrac{1}{12.5\left(0.2 + \frac{1}{5}\right)} = \mathbf{\frac{1}{5}}$

It means that output voltage is one-fifth of the input voltage. This can be readily established by inspection of Fig. 26.8. The two 5 Ω resistors in parallel give a net resistance of 2.5 Ω. Therefore, we have a voltage divider consisting of 10 Ω resistor in series with 2.5 Ω resistor.

$$\therefore \quad \text{Output voltage} = \frac{2.5}{12.5} \times \text{Input voltage}$$

$$\text{or} \quad \frac{\text{Output voltage}}{\text{Input voltage}} = \frac{2.5}{12.5} = \frac{1}{5}$$

$$\text{or} \quad A_v = \frac{1}{5}$$

Comments. The reader may note that in a simple circuit like that of Fig. 26.8, it is not advisable to use *h* parameters to find the input impedance and voltage gain. It is because answers of such circuits can be found directly by inspection. However, in complicated circuits, inspection method becomes cumbersome and the use of *h* parameters yields quick results.

26.5 The h Parameters of a Transistor

It has been seen in the previous sections that every linear circuit is associated with *h* parameters. When this linear circuit is terminated by load r_L, we can find input impedance, current gain, voltage gain, etc. in terms of *h* parameters. Fortunately, for *small* a.c. signals, the transistor behaves as a linear device because the output a.c. signal is directly proportional to the input a.c. signal. Under such circumstances, the a.c. *operation* of the transistor can be described in terms of *h* parameters. The expressions derived for input impedance, voltage gain *etc.* in the previous section shall hold good for transistor amplifier except that here r_L is the a.c. load seen by the transistor.

Fig. 26.9 shows the transistor amplifier circuit. There are four quantities required to describe the external behaviour of the transistor amplifier. These are v_1, i_1, v_2 and i_2 shown on the diagram of Fig. 26.9. These voltages and currents can be related by the following sets of equations :

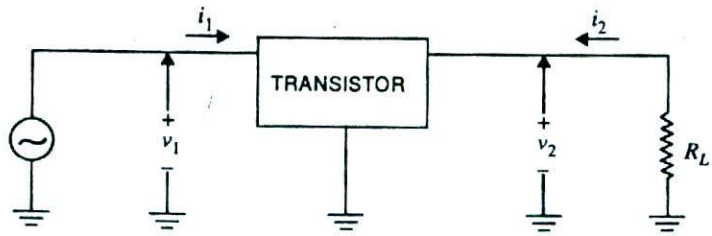


Fig. 26.9

$$v_1 = h_{11}\, i_1 + h_{12}\, v_2$$

$$i_2 = h_{21}\, i_1 + h_{22}\, v_2$$

The following points are worth noting while considering the behaviour of transistor in terms of *h* parameters :

(*i*) For small a.c. signals, a transistor behaves as a linear circuit. Therefore, its a.c. operation can be described in terms of *h* parameters.

(*ii*) The value of *h* parameters of a transistor will depend upon the transistor connection (*i.e. CB, CE* or *CC*) used. For instance, a transistor used in *CB* arrangement may have $h_{11} = 20\ \Omega$. If we use the same transistor in *CE* arrangement, h_{11} will have a different value. Same is the case with other *h* parameters.

(*iii*) The expressions for input impedance, voltage gain etc. derived in Art. 26.4 are also appli-

cable to transistor amplifier except that r_L is the a.c. load seen by the transistor *i.e.*

$$r_L = R_C \| R_L$$

(*iv*) The values of *h* parameters depend upon the operating point. If the operating point is changed, parameter values are also changed.

(*v*) The notation v_1, i_1, v_2 and i_2 is used for general circuit analysis. In a transistor amplifier, we use the notation depending upon the configuration in which transistor is used. Thus for *CE* arrangement,

$$v_1 = V_{be} \quad ; \quad i_1 = I_b \quad ; \quad v_2 = V_{ce} \quad ; \quad i_2 = I_c$$

Here V_{be}, I_b, V_{ce} and I_c are the R.M.S. values.

26.6 Nomenclature for Transistor h Parameters

The numerical subscript notation for *h* parameters (*viz.* h_{11}, h_{21}, h_{12} and h_{22}) is used in general circuit analysis. However, this nomenclature has been modified for a transistor to indicate the nature of parameter and the transistor configuration used. The *h* parameters of a transistor are represented by the following notation :

(*i*) The numerical subscripts are replaced by letter subscripts.

(*ii*) The first letter in the double subscript notation indicates the nature of parameter.

(*iii*) The second letter in the double subscript notation indicates the circuit arrangement (*i.e. CB, CE* or *CC*) used.

Table below shows the *h* parameter nomenclature of a transistor :

S.No.	h parameter	Notation in CB	Notation in CE	Notation in CC
1.	h_{11}	h_{ib}	h_{ie}	h_{ic}
2.	h_{12}	h_{rb}	h_{re}	h_{rc}
3.	h_{21}	h_{fb}	h_{fe}	h_{fc}
4.	h_{22}	h_{ob}	h_{oe}	h_{oc}

Note that first letter *i*, *r*, *f* or *o* indicates the nature of parameter. Thus h_{11} indicates input impedance and this parameter is designated by the subscript *i*. Similarly, letters *r*, *f* and *o* respectively indicate reverse voltage feedback ratio, forward current transfer ratio and output admittance. The second letters *b*, *e* and *c* respectively indicate *CB*, *CE* and *CC* arrangement.

26.7 Transistor Circuit Performance in h Parameters

The expressions for input impedance, voltage gain etc in terms of *h* parameters derived in Art 26.4 for general circuit analysis apply equally for transistor analysis. However, it is profitable to rewrite them in standard transistor *h* parameter nomenclature.

(*i*) **Input impedance.** The general expression for input impedance is

$$Z_{in} = h_{11} - \frac{h_{12}\, h_{21}}{h_{22} + \frac{1}{r_L}}$$

Using standard *h* parameter nomenclature for transistor, its value for CE arrangement will be :

$$Z_{in} = h_{ie} - \frac{h_{re}\, h_{fe}}{h_{oe} + \frac{1}{r_L}}$$

Similarly, expressions for input impedance in *CB* and *CC* arrangements can be written. It may be noted that r_L is the a.c. load seen by the transistor.

(*ii*) **Current gain.** The general expression for current gain is

$$A_i = \frac{h_{21}}{1 + h_{22}\, r_L}$$

Using standard transistor *h* parameter nomenclature, its value for *CE* arrangement is

$$A_i = \frac{h_{fe}}{1 + h_{oe}\, r_L}$$

The reader can readily write down the expressions for *CB* and *CC* arrangements.

(*iii*) **Voltage gain.** The general expression for voltage gain is

$$A_v = \frac{-h_{21}}{Z_{in}\left(h_{22} + \frac{1}{r_L}\right)}$$

Using standard transistor *h* parameter nomenclature, its value for *CE* arrangement is

$$A_v = \frac{-h_{fe}}{Z_{in}\left(h_{oe} + \frac{1}{r_L}\right)}$$

In the same way, expressions for voltage gain in *CB* and *CC* arrangement can be written.

Example 26.4. *A transistor used in CE arrangement has the following set of h parameters when the d.c. operating point is* $V_{CE} = 10$ *volts and* $I_C = 1$ *mA :*

$h_{ie} = 2000\ \Omega$; $h_{oe} = 10^{-4}$ *mho;* $h_{re} = 10^{-3}$; $h_{fe} = 50$

Determine (i) input impedance (ii) current gain and (iii) voltage gain. The a.c. load seen by the transistor is $r_L = 600\ \Omega$. *What will be approximate values using reasonable approximations?*

Solution. (*i*) Input impedance is given by;

$$Z_{in} = h_{ie} - \frac{h_{re}\, h_{fe}}{h_{oe} + \frac{1}{r_L}} = 2000 - \frac{10^{-3} \times 50}{10^{-4} + \frac{1}{600}} \quad \ldots (i)$$

$$= 2000 - 28 = \mathbf{1972\ \Omega}$$

The second term in eq. (*i*) is quite small as compared to the first.

$$\therefore \quad Z_{in} \simeq h_{ie} = \mathbf{2000\ \Omega}$$

(*ii*) Current gain, $A_i = \dfrac{h_{fe}}{1 + h_{oe} \times r_L} = \dfrac{50}{1 + (600 \times 10^{-4})} = \mathbf{47}$

If $h_{oe}\, r_L << 1$, then $A_i \simeq h_{fe} = \mathbf{50}$

(*iii*) Voltage gain, $A_v = \dfrac{-h_{fe}}{Z_{in}\left(h_{oe} + \frac{1}{r_L}\right)} = \dfrac{-50}{1972\left(10^{-4} + \frac{1}{600}\right)} = \mathbf{-14.4}$

The negative sign indicates that there is 180° phase shift between input and output. The magnitude of gain is 14.4. In other words, the output signal is 14.4 times greater than the input and it is 180° out of phase with the input.

Example 26.5. *A transistor used in CE connection has the following set of h parameters when the d.c. operating point is* $V_{CE} = 5$ *volts and* $I_C = 1$ *mA :*

$h_{ie} = 1700\ \Omega$; $h_{re} = 1.3 \times 10^{-4}$; $h_{fe} = 38$; $h_{oe} = 6 \times 10^{-6}\ \mho$

If the a.c. load r_L *seen by the transistor is 2 kΩ, find (i) the input impedance (ii) current gain and (iii) voltage gain.*

Solution. (*i*) The input impedance looking into the base of transistor is

$$Z_{in} = h_{ie} - \frac{h_{re}\, h_{fe}}{h_{oe} + \frac{1}{r_L}} = 1700 - \frac{1.3 \times 10^{-4} \times 38}{6 \times 10^{-6} + \frac{1}{2000}} \simeq \mathbf{1690\ \Omega}$$

(*ii*) Current gain, $A_i = \dfrac{h_{fe}}{1 + h_{oe} r_L} = \dfrac{38}{1 + 6 \times 10^{-6} \times 2000} = \dfrac{38}{1.012} \simeq \mathbf{37.6}$

(*iii*) Voltage gain, $A_v = \dfrac{-h_{fe}}{Z_{in}\left(h_{oe} + \frac{1}{r_L}\right)} = \dfrac{-38}{1690\left(6 \times 10^{-6} + \frac{1}{2000}\right)} = \mathbf{-44.4}$

Example 26.6. *Fig. 26.10 shows the transistor amplifier in CE arrangement. The h parameters of transistor are as under :*

$h_{ie} = 1500\ \Omega$; $h_{fe} = 50$; $h_{re} = 4 \times 10^{-4}$; $h_{oe} = 5 \times 10^{-5}\ \mho$

Find (i) a.c. input impedance of the amplifier and (ii) voltage gain.

Solution. The a.c. load r_L seen by the transistor is equivalent of the parallel combination of R_C (= 10 kΩ) and R_L (= 30 kΩ) *i.e.*

$$r_L = \frac{R_C R_L}{R_C + R_L} = \frac{10 \times 30}{10 + 30} = 7.5\ \text{k}\Omega = 7500\ \Omega$$

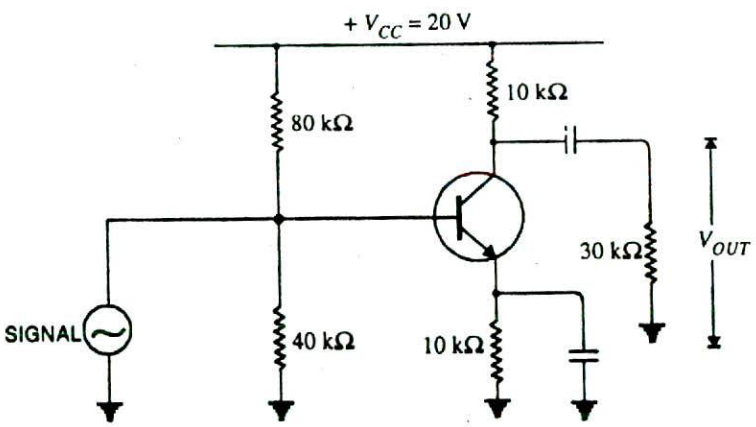


Fig. 26.10

(*i*) The input impedance looking into the base of transistor is given by ;

$$Z_{in} = h_{ie} - \frac{h_{re}\, h_{fe}}{h_{oe} + \frac{1}{r_L}} = 1500 - \frac{4 \times 10^{-4} \times 50}{5 \times 10^{-5} + \frac{1}{7500}} = 1390\ \Omega$$

This is only the input impedance looking into the base of transistor. The a.c. input impedance of the entire stage will be Z_{in} in parallel with bias resistors *i.e.*

Input impedance of stage $= 80 \times 10^3 \,\|\, 40 \times 10^3 \,\|\, 1390 = \mathbf{1320\ \Omega}$

(*ii*) Voltage gain, $A_v = \dfrac{-h_{fe}}{Z_{in}\left(h_{oe} + \frac{1}{r_L}\right)} = \dfrac{-50}{1390\left(5 \times 10^{-5} + \frac{1}{7500}\right)}$

$= \mathbf{-196}$

The negative sign indicates phase reversal. The magnitude of gain is 196.

26.8 Experimental Determination of Transistor h Parameters

The determination of h parameters of a general linear circuit has already been discussed in Art. 26.2. To illustrate how such a procedure is carried out for a CE transistor amplifier, consider the circuit of Fig. 26.11. The R.M.S. values will be considered in the discussion. Using standard transistor nomenclature :

$$V_{be} = h_{ie} I_b + h_{re} V_{ce} \quad ...(i)$$

$$I_c = h_{fe} I_b + h_{oe} V_{ce} \quad ...(ii)$$

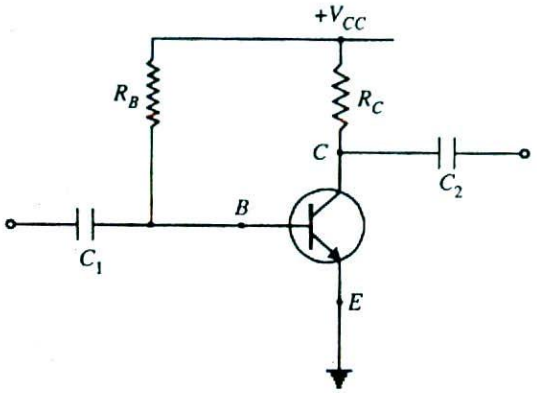


Fig. 26.11

(*i*) **Determination of h_{fe} and h_{ie}.** In order to determine these parameters, the output is a.c. short circuited as shown in Fig. 26.12 (*i*). This is accomplished by making the capacitance of C_2 deliberately large. The result is that changing component of collector current flows through C_2 instead of R_C and a.c. voltage developed across C_2 is zero *i.e.* $^*V_{ce} = 0$.

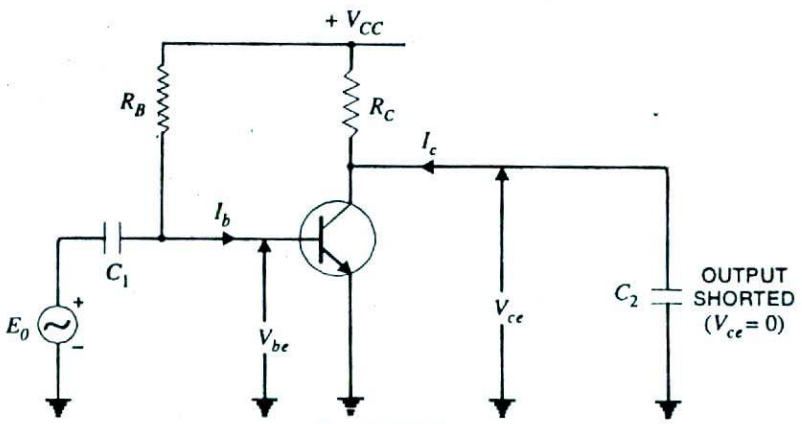


Fig. 26.12 (*i*)

Substituting $V_{ce} = 0$ in equations (*i*) and (*ii*) above, we get,

$$V_{be} = h_{ie} I_b + h_{re} \times 0$$

$$I_c = h_{fe} I_b + h_{oe} \times 0$$

---

* Note that setting $V_{ce} = 0$ does not mean that V_{CE} (the d.c. collector-emitter voltage) is zero. Only a.c. output is short-circuited.

$$\therefore \qquad h_{fe} = \frac{I_c}{I_b} \quad \text{for} \quad V_{ce} = 0$$

and $$h_{ie} = \frac{V_{be}}{I_b} \text{ for } V_{ce} = 0$$

Note that I_c and I_b are the a.c. R.M.S. collector and base currents respectively. Also V_{be} is the a.c. R.M.S. base-emitter voltage.

(*ii*) **Determination of h_{re} and h_{oe}.** In order to determine these two parameters, the input is a.c. open-circuited, a signal generator is applied across the output and resulting V_{be}, V_{ce} and I_c are measured. This is illustrated in Fig 26.12 (*ii*). A large inductor L is connected in series with R_B. Since the d.c. resistance of inductor is very small, it does not disturb the operating point. Again, a.c. current cannot flow through R_B because of large reactance of inductor. Further, the voltmeter used to measure V_{be} has a high input impedance and hence there are no paths connected to the base with any appreciable a.c. current. This means that base is *effectively a.c. open-circuited *i.e.* $I_b = 0$.

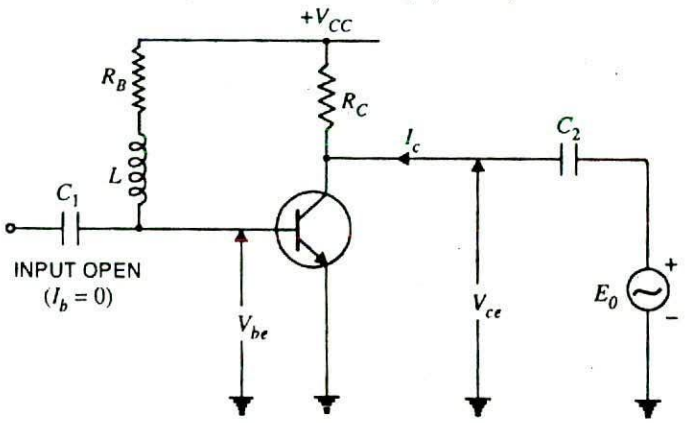


Fig. 26.12 (*ii*)

Substituting $I_b = 0$ in equations (*i*) and (*ii*), we get,

$$V_{be} = h_{ie} \times 0 + h_{re} V_{ce}$$

$$I_c = h_{fe} \times 0 + h_{oe} V_{ce}$$

$$\therefore \qquad h_{re} = \frac{V_{be}}{V_{ce}} \text{ for } I_b = 0$$

and $$h_{oe} = \frac{I_c}{V_{ce}} \text{ for } I_b = 0$$

Example 26.7. *The following quantities are measured in a CE amplifier circuit :*

(*a*) *With output a.c. short-circuited* (*i.e.* $V_{ce} = 0$)

$$I_b = 10\,\mu A;\ I_c = 1\ mA;\ V_{be} = 10\ mV$$

(*b*) *With input a.c. open-circuited* (*i.e.* $I_b = 0$)

$$V_{be} = 0.65\ mV;\ I_c = 60\,\mu A;\ V_{ce} = 1\ V$$

Determine all the four h parameters.

---

* How effectively the base is a.c. open-circuited depends upon the reactance L and the input impedance of the voltmeter used to measure V_{be}.

Solution.

$$h_{ie} = \frac{V_{be}}{I_b} = \frac{10 \times 10^{-3}}{10 \times 10^{-6}} = 1000\ \Omega$$

$$h_{fe} \triangleq \frac{I_c}{I_b} = \frac{1 \times 10^{-3}}{10 \times 10^{-6}} = 100$$

$$h_{re} = \frac{V_{be}}{V_{ce}} = \frac{0.65 \times 10^{-3}}{1} = 0.65 \times 10^{-3}$$

$$h_{oe} = \frac{I_c}{V_{ce}} = \frac{60 \times 10^{-6}}{1} = 60\ \mu\text{mho}$$

26.9 Limitations of h Parameters

The *h* parameter approach provides accurate information regarding the current gain, voltage gain, input impedance and output impedance of a transistor amplifier. However, there are two major limitations on the use of these parameters.

(*i*) It is very difficult to get the exact values of *h* parameters for a particular transistor. It is because these parameters are subject to considerable variation-unit to unit variation, variation due to change in temperature and variation due to change in operating point. In predicting an amplifier performance, care must be taken to use *h* parameter values that are correct for the operating point being considered.

(*ii*) The *h* parameter approach gives correct answers for small a.c. signals only. It is because a transistor behaves as a linear device for small signals only.

Multiple-Choice Questions

1. Hybrid means .....
   (*i*) mixed (*ii*) single
   (*iii*) unique (*iv*) none of the above
2. There are ..... *h* parameters of a transistor.
   (*i*) two (*ii*) four
   (*iii*) three (*iv*) none of the above
3. The *h* parameter approach gives correct results for .....
   (*i*) large signals only
   (*ii*) small signals only
   (*iii*) both small and large signals
   (*iv*) none of the above
4. A transistor behaves as a linear device for .....
   (*i*) small signals only
   (*ii*) large signals only
   (*iii*) both small and large signals
   (*iv*) none of the above
5. The parameter h_{ie} stands for input impedance in .....
   (*i*) *CB* arrangement with output shorted
   (*ii*) *CC* arrangement with output shorted
   (*iii*) *CE* arrangement with output shorted
   (*iv*) none of the above
6. The dimension of h_{ie} parameter is .....
   (*i*) mho (*ii*) ohm
   (*iii*) farad (*iv*) none of the above
7. The parameter h_{fe} is called ..... in *CE* arrangement with output shorted.
   (*i*) voltage gain
   (*ii*) current gain
   (*iii*) input impedance
   (*iv*) none of the above
8. If the operating point changes, the *h* parameters of a transistor .....
   (*i*) also change
   (*ii*) do not change
   (*iii*) may or may not change
   (*iv*) none of the above
9. The values of *h* parameter of a transistor in *CE* arrangement are ..... arrangement.
   (*i*) the same as for *CB*

(*ii*) the same as for *CC*
(*iii*) different from that in *CB*
(*iv*) none of the above

10. In order to determine h_{fe} and h_{ie} parameters of a transistor, ... is a.c. short-circuited.
(*i*) input
(*ii*) output
(*iii*) input as well as output
(*iv*) none of the above

11. If temperature changes, *h* parameters of a transistor .....
(*i*) may or may not change
(*ii*) do not change
(*iii*) also change
(*iv*) none of the above

12. In *CE* arrangement, the value of input impedance is approximately equal to .....
(*i*) h_{ie} (*ii*) h_{oe}
(*iii*) h_{re} (*iv*) none of the above

13. Using standard transistor *h* parameter nomenclature, the voltage gain in *CE* arrangement is .....
(*i*) $\dfrac{-h_{fe}}{Z_{in}\left(h_{oe}+\dfrac{1}{r_L}\right)}$
(*ii*) $\dfrac{-h_{fe}}{Z_{out}\left(h_{oe}+1\right)}$
(*iii*) $\dfrac{-h_{fe}}{h_{oe}+h_{re}}$
(*iv*) none of the above

14. $Z_{in} = h_{ie} - \dfrac{.....}{h_{oe}+\dfrac{1}{r_L}}$
(*i*) $h_{re}\,h_{oe}$ (*ii*) $h_{re}\,h_{fe}$
(*iii*) $r_L\,h_{oe}$ (*iv*) none of the above

15. ..... *h* parameters of a transistor are dimensionless.
(*i*) four (*ii*) three
(*iii*) two (*iv*) none of the above

Answers to Multiple-Choice Questions

1. (*i*)	**2.** (*ii*)	**3.** (*ii*)	**4.** (*i*)	**5.** (*iii*)
6. (*ii*)	**7.** (*ii*)	**8.** (*i*)	**9.** (*iii*)	**10.** (*ii*)
11. (*iii*)	**12.** (*i*)	**13.** (*i*)	**14.** (*ii*)	**15.** (*iii*)

Chapter Review Topics

1. What do you understand by hybrid parameters ? What are their dimensions ?
2. How will you measure *h* parameters of a linear circuit ?
3. Draw the *h* parameter equivalent circuit of a linear circuit.
4. What is the physical meaning of *h* parameters ?
5. Derive the general formula for :
   (*i*) input impedance (*ii*) current gain and (*iii*) voltage gain in terms of *h* parameters and the load.
6. What are the notations for *h* parameters of a transistor when used in (*i*) *CB* (*ii*) *CE* and (*iii*) *CC* arrangement ?
7. How are *h* parameters of a transistor measured ?
8. What are the drawbacks of *h* parameter approach in the design of a transistor amplifier ?

Discussion Questions

1. What is the origin of the name hybrid ?
2. How can we obtain an effective a.c. short-circuit across the output of an amplifier ? Does this affect d.c. operating conditions ?
3. When *h* parameters are specified for a particular transistor, the operating point is usually given. Why is this necessary ?
4. How can we obtain an effective a.c. open circuit at the input to an amplifier ? Does this affect d.c. operating conditions. ?
5. Under what condition is the input impedance of a transistor equal to h_{ie} ?

27

Digital Electronics

Introduction

A continuously varying signal (voltage or current) is called an *analog signal.* For example, a sinusoidal voltage is an analog signal. In the previous chapter, we studied the behaviour of diodes and transistors primarily from the analog or continuous-signal point of view. In an analog electronic circuit, the output voltage changes continuously according to the input voltage variations. In other words, the output voltage can have an infinite number of values. A signal (voltage or current) which can have only two discrete values is called a *digital signal.* For example, a square wave is a digital signal. The semiconductors devices (*e.g.* diodes, transistors etc) can be designed for two-state operation *viz*, saturation and cut off. In that case, the output voltage can have only two states (*i.e.*, values), either *low or high. An electronic circuit that is designed for two-state operation is called a **digital circuit**.

The branch of electronics which deals with digital circuits is called **digital electronics**. When most of us hear the term *digital*, we immediately think of "digital calculator" or "digital computer". This is attributed to the dramatic way the low-cost, powerful calculators and computers have become accessible to an average person. Now digital circuits are being used in many electronic products such as video games, microwave ovens and oscilloscopes. Digital techniques have also replaced a lot of the older "analog circuits" used in consumer products such as radios, TV sets and high-fidelity sound recording and playback equipment. In this chapter, we shall discuss the fundamental aspects of digital electronics.

27.1 Analog and Digital Signals

(*i*) **Analog signal.** A continuously varying signal (voltage or current) is called an *analog signal.* For example, an alternating voltage varying sinusoidally is an analog signal [See Fig. 27.1]. If such an analog signal is applied to the input of a transistor amplifier, the output voltage will also vary sinusoidally. This is the analog operation *i.e.*, the output voltage can have an infinite number of values. Due to many-valued output, the analog operation is less reliable.

(*ii*) **Digital signal.** A signal (voltage or current) that can have only two discrete values is called a *digital signal.* For example, a square wave is a digital signal [See Fig. 27.2]. It is because this signal has only two values viz, +5 V and 0 V and no other value. These values are labelled as *High* and *Low*. The High voltage is + 5 V and the Low voltage is 0 V. If proper digital signal is applied to the input of a transistor, the transistor can be driven between *cut off* and *saturation*. In other words, the transistor will have two-state operations *i.e.*, output is either low or high. Since digital operation has only

* The exact value of voltage is unimportant if the voltage is distinguishable as low or high.

two states (*i.e.*, *ON* or *OFF*), it is far more reliable than many-valued analog operation. It is because with two-states operation, all the signals are easily recognised as either low or high.

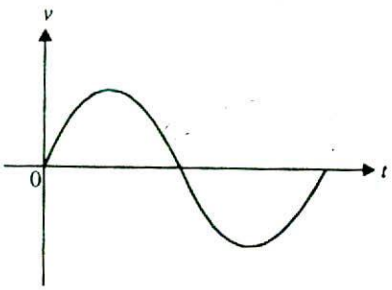


Fig. 27.1

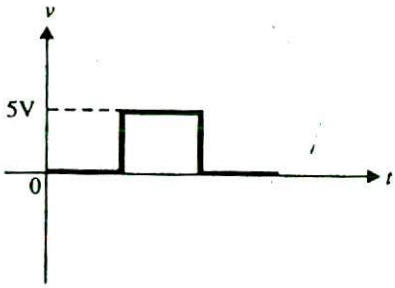


Fig. 27.2

27.2 Digital Circuit

An electronic circuit that handles only a digital signal is called a ***digital circuit.***

The output voltage of a digital circuit is either low or high and no other value. In other words, digital operation is a two-state operation. These states are expressed as (*High* or *Low*) or (*ON* or *OFF*) or (1 or 0). Therefore, a digital circuit is one that expresses the values in digits 1's or 0's. Hence the name digital. The numbering concept that uses only the two digits 1 and 0 is the *binary numbering system.* Therefore, the first step would be to discuss this number system.

27.3 Binary Number System

A number system is a code that uses symbols to count the number of items. The most common and familiar number system is the decimal number system. The decimal number system uses the symbols 0, 1, 2, 3, 4, 5, 6, 7, 8 and 9. Thus, the decimal system uses 10 digits for counting the items. A binary system uses only two digits (0 and 1) for counting the items. The reader may wonder how to count the items in a binary system. Let us see how it is done.

Counting in Decimal and Binary systems. Figure 27.3 shows the counting of stones in decimal as well as binary system. As you will see, the counting in the binary number system is performed much the same way in the decimal number system.

Stones	Decimal	Binary
No stone	0	0
•	1	1
••	2	10
•••	3	11
••••	4	100
•••••	5	101
••••••	6	110
•••••••	7	111
••••••••	8	1000
•••••••••	9	1001

Fig. 27.3

(*i*) Let us first see how items are counted in decimal system. In this system, the count starts as 0, 1, ..., 9. After 9, we are to write the next number. To do so, we use the second digit of the decimal

system (*i.e.*, 1) followed by the first digit (*i.e.*, 0). So after 9, the next number is 10. The count again continues as 10, 11, 12 ....., 19. After 19, we use the third digit of the system (*i.e.*, 2) followed by the first digit (*i.e.*, 0) and the count continues as 20, 21, ... etc. In this way, we get the number up to 99. In order to represent a number next to 99, we use three decimal digits (100). That is to say second digit of the decimal system (*i.e.*, 1) followed by two first digits (*i.e*, two zeros).

(*ii*) Let us now turn to binary system. Note that 0 and 1 count in the binary system is the same as in the decimal counting. To represent 2 stones, we use the second binary digit (*i.e.*, 1) followed by the first (*i.e.*, 0). This gives binary number 10 (read as one-zero and not ten) as an equivalent of 2 in the decimal system. Likewise, 3 in the decimal system can be represented by the binary number 11 (read as one-one and not eleven). After this, the two binary digits are exhausted. We shall use three digits to represent the next binary number. Thus, to represent 4 (four), we use the second binary digit followed by two first binary digits. This gives the binary *100 (read as one-zero-zero) as equivalent to 4 in the decimal system. Here is a simple way to find binary equivalents. *Each time the two digits 1 and 0 in one position are exhausted (counted as high as they will go), a 1 is added at the left, all digits to the right are made 0, and the count continues.* The reader may apply this simple rule to find next binary numbers.

Notes :

(*i*) Each binary digit (0 or 1) is referred to as a *bit*. A string of four bits is called as a *nibble* and eight bits make a *byte*. Thus, 1001 is a nibble and 10010110 is a binary byte.

(*ii*) The binary number system is the most useful in digital circuits because there are only two digits (0 and 1).

27.4 Place Value

Consider the decimal number 642. This can be expressed as;

$$642 = 600 + 40 + 2$$

Note that in a multidigit decimal number (*i.e.*, 642 in the present case), each position has a value that is 10 times the value of the next position to its immediate right. In other words, every position can be expressed as :

$$642 = 6 \times 10^2 + 4 \times 10^1 + 2 \times 10^0$$

Thus, we find that values of various positions in a decimal number system are powers of 10 *i.e.*, equal to the number of digits used in the system. This number is called *base* or *radix* of the system. Thus, the decimal system has base of 10 (ten).

For the decimals, the digit to the extreme right is referred to as the *least significant digit* (*LSD*) because its positional value or weight is the lowest. For the decimal number 642, 2 is the *LSD*. The left-most digit in the decimal number is the *most significant digit* (*MSD*) because its positional value or weight is the highest. For the decimal number 642, 6 is the *MSD* with a value of 600.

Binary number system. In the binary number system, only two digits (0 and 1) are used. Therefore, the *base* of this system is 2. In a binary number, each position has a value that is 2 times the value of the next position to its immediate right. In other words, every position can be expressed by 2 raised to some power. We know that binary number 1001 is equal to the decimal number 9. This can be readily shown as under :

$$1001 = 1 \times 2^3 + 0 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 = 9$$

For binary numbers, the digit at the extreme right is referred to as *least significant bit* (*LSB*). In the binary number 1001, the 1 at the right is the *LSB*. The left-most digit is called the *most significant*

---

* Note that the procedure is similar to that which was used to write 100 (hundred) in the decimal system.

bit (*MSB*). In the binary number 1001, the 1 at the left is the *MSB* with the value of 8 in decimal terms.

27.5 Decimal to Binary Conversion

There are many methods to perform this conversion. The method described here is called *double-dabble* because it requires successive divisions by 2. This method can be summarised as under :

Divide progressively the decimal number by 2 and write down the remainder after each division. Continue this process till you get a quotient of 0 and remainder of 1, the conversion is now complete. The remainders, taken in reverse order, form the binary number [See Fig. 27.4].

Note that 13 is first divided by 2, giving a quotient of 6 with a remainder of 1. This remainder becomes the 2^0 position in the binary number. The 6 is then divided by 2, giving a quotient of 3 with a remainder of 0. This remainder becomes the 2^1 position in the binary number.

Continuing this procedure, the equivalent binary number is 1101.

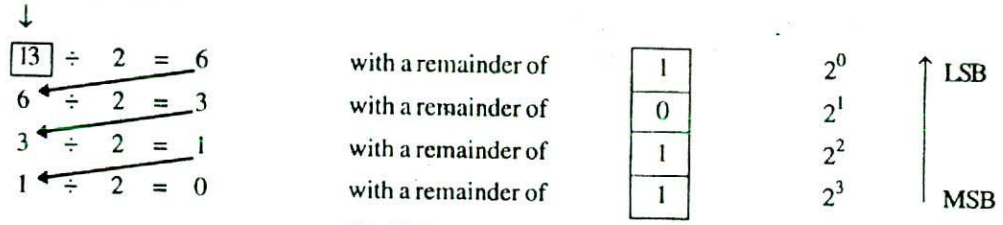


Fig. 27.4

Example 27.1. *Convert the decimal number 37 to its equivalent binary number.*

2	37
2	18 – 1
2	9 – 0
2	4 – 1
2	2 – 0
2	1 – 0
	0 – 1

Solution. Using double-dabble method, we find that the equivalent binary number is 100101. It is a usual practice to mention the base of the number system. The decimal system has a base of 10 while binary system has a base of 2.

$$\therefore \quad (37)_{10} = (100101)_2$$

Note. This notation avoids the confusion that may arise because decimal number also involves the digits 0 and 1. Thus, $(101)_{10}$ denotes the decimal number hundred one while the binary number $(101)_2$ is equivalent to decimal number 5.

Example 27.2. *Convert the decimal number 23 to its equivalent binary number.*

2	23
2	11 – 1
2	5 – 1
2	2 – 1
2	1 – 0
	0 – 1

Solution. Using double-dabble method, we find that the equivalent binary number is 10111.

$$\therefore \quad (23)_{10} = (10111)_2$$

Note that binary number 10111 has five bits.

27.6 Binary to Decimal Conversion

Binary numbers can be converted to equivalent decimal numbers quite easily. Suppose you are given the binary number 110011. Its conversion to equivalent decimal number involves the following two steps :

1	1	0	0	1	1
2^5	2^4	2^3	2^2	2^1	2^0

(*i*) Place the decimal value of each position of the binary number.

(*ii*) Add all the decimal values to get the decimal number.

Thus,
$$(110011)_2 = 1\times2^5 + 1\times2^4 + 0\times2^3 + 0\times2^2 + 1\times2^1 + 1\times2^0$$
$$= 32 + 16 + 0 + 0 + 2 + 1 = 51$$

$$\therefore \quad (110011)_2 = (51)_{10}$$

Note. In binary to decimal conversion, all positions containing 0 can be ignored. Only add the

decimal values of the positions where 1 appears. Thus, in case of the above binary number.

$$(110011)_2 = 1\times2^5 + 1\times2^4 + 1\times2^1 + 1\times2^0$$
$$= 32 + 16 + 2 + 1 = 51$$

Example 27.3. *Convert the binary number 110001 to its equivalent decimal number.*

Solution. The binary number along with its decimal values of various positions is shown.

$$\therefore \quad (110001)_2 = 1\times2^5 + 1\times2^4 + 1\times2^0 \qquad \begin{matrix} 1 & 1 & 0 & 0 & 0 & 1 \\ 2^5 & 2^4 & 2^3 & 2^2 & 2^1 & 2^0 \end{matrix}$$
$$= 32 + 16 + 1 = 49$$

or $(110001)_2 = (49)_{10}$

27.7 Logic Gates

A digital circuit with one or more input signals but only one output signal is called a **logic gate**.

Since a logic gate is a switching circuit (*i.e.* a digital circuit), its output can have only one of the two possible states *viz.*, either a high voltage (1) or a low voltage (0) — it is either *ON* or *OFF*. Whether the output voltage of a logic gate is high (1) or low (0) will depend upon the conditions at its input. Fig. 27.5 shows the basic idea of a *logic gate using switches.

(*i*) When S_1 and S_2 are open, the bulb is *OFF*.

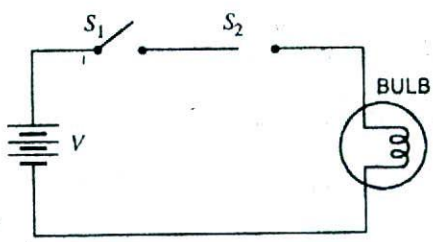
(*ii*) When S_1 is open and S_2 closed, the bulb is *OFF*.

(*iii*) When S_2 is open and S_1 closed, the bulb is *OFF*.

(*iv*) When both S_1 and S_2 are closed, the bulb is *ON*.

Note that output (*OFF* or *ON*) depends upon the conditions at the input.

The four possible combinations of switches S_1 and S_2 are shown in the table below. It is clear that when either of the switches (S_1 or S_2) or both are open, the bulb is *OFF*. In binary language, when either of the inputs or both the inputs are low (0), the output is low. When both switches are closed, the bulb is *ON*. In terms of binary language, when both the inputs are high (1), the output is high. It is usual practice to show the conditions at the input and output of a logic gate in the binary form as shown in the table below. Such a table is called **truth table**.



(*i*)

S_1	S_2	Bulb
open	open	OFF
open	closed	OFF
closed	open	OFF
closed	closed	ON

(*ii*)

Truth Table

S_1	S_2	Output
0	0	0
0	1	0
1	0	0
1	1	1

(*iii*)

Fig. 27.5

The term "logic" is usually used to refer to a decision-making process. A logic gate makes logical decisions regarding the existence of output depending upon the nature of the input. Hence, such circuits are called logic circuits.

27.8 Three Basic Logic Gates

A logic gate is a circuit that has one or more input signals but only one output signal. All logic gates can be analysed by constructing a truth table. A truth table lists all input possibilities and the

* In itself, the circuit is not actually a logic gate but the logic is similar. The actual gate circuits are made with diodes and transistors. In other words, switches S_1 and S_2 are replaced by diodes or transistors.

corresponding output for each input. The three basic logic gates that make up all digital circuits are (*i*) OR gate (*ii*) AND gate and (*iii*) NOT gate. We shall first discuss these three basic logic gates and then the combination of these gates. The following points may be noted about logic *gates :

(*i*) A binary 0 represents 0 V and binary 1 represents + 5V**. It is common to refer to binary 0 as LOW input or output and binary 1 as HIGH input or output.

(*ii*) A logic gate has only one output signal. The output will depend upon the input signal/ signals and the type of gate.

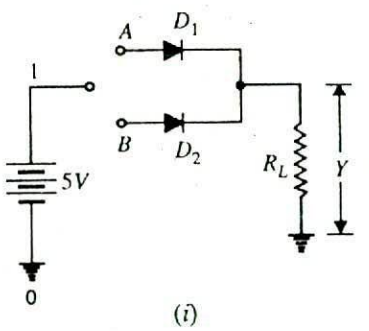
(*iii*) The operation of a logic gate may be described either by **truth table** or **Boolean algebra.**

27.9 OR Gate

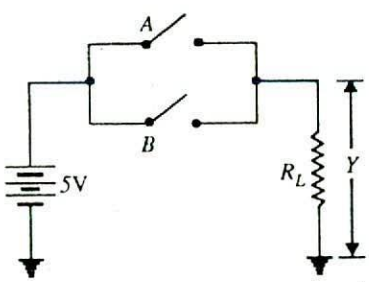
An OR gate is a logic gate that has two or more inputs but only one output. However, the output *Y* of an OR gate is LOW when *all* inputs are LOW. The output *Y* of an OR gate is HIGH if any or all the inputs are HIGH.

It is called OR gate because the output is high if any or all the inputs are high. For the same reason, an OR gate is sometimes called "any or all gate". For example, consider a 2-input OR gate. The output *Y* will he high if either or both inputs are high.

OR gate operation. Fig. 27.6 (*i*) shows one way to build a 2-input OR gate while Fig. †27.6 (*ii*) shows its simplified schematic diagram. The input voltages are labelled as *A* and *B* while the output voltage is *Y*. Note that negative terminal of the battery is grounded and corresponds to 0 state (LOW level). The positive terminal of the battery (+5 V) corresponds to 1 state (HIGH level). There are only four input-output possibilities



(*i*)



(*ii*)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

(*iii*)

Fig. 27.6

(*i*) When both *A* and *B* are connected to ground, both diodes are non-conducting. Hence, the output voltage is ideally zero (low voltage). In terms of binary, when $A = 0$ and $B = 0$, then $Y = 0$ as shown in the truth table in Fig. 27.6 (*iii*).

(*ii*) When *A* is connected to ground and *B* connected to the positive terminal of the battery, diode D_2 is forward biased and diode D_1 is non-conducting. Therefore, diode D_2 conducts and the output voltage is ideally +5 V. In terms of binary, when $A = 0$ and $B = 1$, then $Y = 1$ [See Fig. 27.6 (*iii*)].

---

* A *gate* can be regarded as a *barrier* which when closed prevents the passgae of information but if open allows the signal/signals to pass through freely.

** In digital systems, the binary information is represented by two voltage levels, generally +5 V and 0 V. So 5 V is used to represent binary 1 and 0 V is used to represent binary 0.

† As you can see in Fig. 27.6 (*ii*) that output is high when *either* or *both* of the input switches are closed but not when both are open.

(*iii*) When A is connected to the positive terminal of the battery and B to the ground, diode D_1 is on and diode D_2 is off. Again the output voltage is +5 V. In binary terms, when $A = 1$ and $B = 0$, then $Y = 1$ [See Fig. 27.6 (*iii*)].

(*iv*) When both A and B are connected to the positive terminal of the battery, both diodes are on. Since the diodes are in parellel, the output voltage is +5 V. In binary terms, when $A = 1$ and $B = 1$, then $Y = 1$ [See Fig. 27.6 (*iii*)].

It is clear from the truth table that *for OR gate, the output is high if any or all of the inputs are high. The only way to get a low output is by having all inputs low.* Fig. 27.7 shows the logic symbol or OR gate. Note that the symbol has curved line at the input.

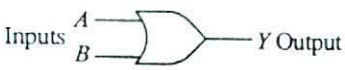


Fig. 27.7

Boolean expression. The algebra used to symbolically describe logic functions is called Boolean algebra. The "+" sign in Boolean algebra refers to the logical OR function. The Boolean expression for OR function is

$$A + B = Y$$
$$\uparrow$$
OR symbol

$A + B$	=	Y
0 + 0	=	0
0 + 1	=	1
1 + 0	=	1
1 + 1	=	1

The adjoining table shows possibilities for the inputs. According to this table, when 0 is ORed with 0, the result equals 0. Also, any variable ORed with 1 equals 1. The OR function can be summed up as under :

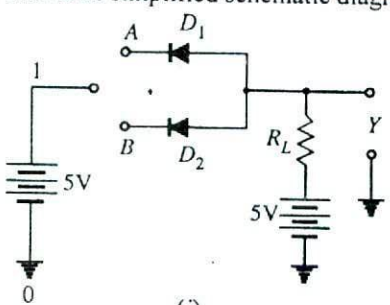
0 ORed with 0 equals 0
0 ORed with 1 equals 1
1 ORed with 1 equals 1

27.10 AND Gate

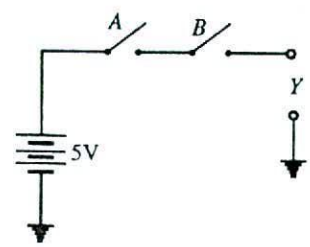
The AND gate is a logic gate that has two or more inputs but only one output. The output Y of AND gate is HIGH when all inputs are HIGH. However, the output Y of AND gate is LOW if any or all inputs are LOW.

It is called AND gate because output is high only when all the inputs are high. For this reason, the AND gate is sometimes called "all or nothing gate". For example, consider a 2-input AND gate. The output will be high when both the inputs are high.

AND gate operation. Fig. 27.8 (*i*) shows one way to build a 2-input AND gate while *Fig. 27.8 (*ii*) shows its simplified schematic diagram. There are only four input-output possibilities.



(*i*)



(*ii*)

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

(*iii*)

Fig. 27.8

* Note that two switches used to represents the OR function were connected in parallel. If the switches are connected in series [See Fig. 27.8 (*ii*)], AND function is obtained. The output is high if both the switches are closed. The output will be low if either switch is open.

(*i*) When both A and B are connected to ground, both the diodes (D_1 and D_2) are forward biased and hence they conduct current. Consequently, the two dioedes are grounded and output voltage is zero. In terms of binary, when $A = 0$ and $B = 0$, then $Y = 0$ as shown in truth table in Fig. 27.8 (*iii*).

(*ii*) When A is connected to the ground and B connected to the positive terminal of the battery, diode D_1 is forward biased while diode D_2 will not conduct. Therefore, diode D_1 conducts and is grounded. Again output voltage will be zero. In binary terms, when $A = 0$ and $B = 1$, then $Y = 0$. This fact is shown in the truth table.

(*iii*) When B is connected to the ground and A connected to the positive terminal of the battery, the roles of diodes are interchanged. Now diode D_2 will conduct while diode D_1 does not conduct. As a result, diode D_2 is grounded and again output voltage is zero. In binary terms, when $A = 1$ and $B = 0$, then $Y = 0$. This fact is indicated in the truth table.

(*iv*) When both A and B are connected to the positive terminal of the binary, both the diodes do not conduct. Now, the output voltage is +5 V because there is no current through R_L.

It is clear from the truth table that *for AND gate, the output is high if all the inputs are high. However, the output is low if any or all inputs are low.* Fig. 27.9 shows the logic symbol of AND gate. This is the symbol you should memorise and use from now on for AND gates.

Boolean expression. The Boolean expression for AND function is

$$A \,.\, B = Y$$
$$\uparrow$$
AND symbol

where the multiplication *dot stands for the AND operation. The adjoining table shows the possibilities for the inputs. Table tells us that 0 ANDed with any variable equals 0. Also, 1 ANDed with 1 equals one. The AND function can be summed up as under :

0 ANDed with 0 equals 0
0 ANDed with 1 equals 0
1 ANDed with 1 equals 1

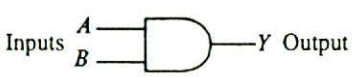
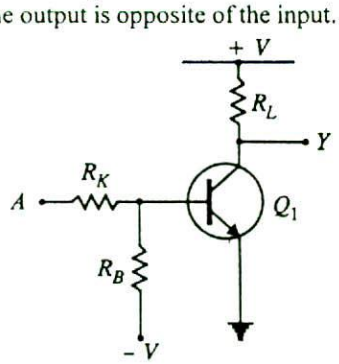


Fig. 27.9

$A \,.\, B$	=	Y
0 . 0	=	0
0 . 1	=	0
1 . 0	=	0
1 . 1	=	1

27.11 NOT Gate or Inverter

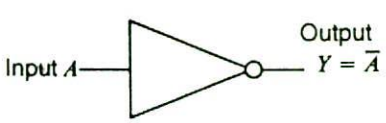
The NOT gate or inverter is the simplest of all logic gates. It has only one input and one output, where the output is opposite of the input. The NOT gate is often called inverter because it inverts the input.



(*i*)

A	Y
0	1
1	0

(*ii*)



(*iii*)

Fig. 27.10

* Note that the multiplication dot is often omitted, so expression may appear as $AB = Y$.

Figure 27.10 (*i*) shows a *typical inverter circuit. When A is connected to ground, the base of transistor Q_1 will become negative. This negative potential causes the transistor to cut off and collector current is zero and output is + V volts. In binary terms, when $A = 0$, $Y = 1$. If sufficiently large positive voltage is applied at A, the base of the transistor will become positive, causing the transistor to conduct heavily. Therefore, the output voltage is zero. In binary terms, when A = 1, Y = 0. Fig. 27.10 (*ii*) shows truth table for an inverter. It is clear from the truth table that whatever the input to the inverter, the output assumes opposite polarity. If the input is 0, the output will be 1 ; if the input is 1, the output will be 0.

Figure 27.10 (*iii*) shows the logic symbol for NOT gate or inverter. Note that small bubble on the inverter symbol represents inversion. The Boolean expression for NOT function is

$$Y = \overline{A}$$

Note that bar above the input A represents inversion.

If $A = 0$, then $Y = \overline{0}$ or $Y = 1$

If $A = 1$, then $Y = \overline{1}$ or $Y = 0$

27.12 Combination of Basic Logic Gates

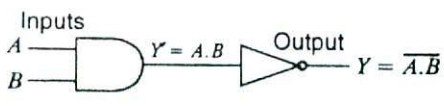
The OR, AND and NOT gates are the three basic circuits that make up all digital circuits. We shall discuss a few combinations of these basic circuits.

(*i*) **NAND gate.** It is a combination of AND gate and NOT gate. In other words, output of AND gate is connected to the input of a NOT gate as shown in Fig. 27.11 (*i*). Clearly, the output of a NAND gate is opposite to the AND gate. This is illustrated in the truth table for the NAND gate. Note that truth table for NAND gate is developed by *inverting the outputs* of the AND gate.

The Boolean expression for NAND function is

$$Y = \overline{A \cdot B}$$

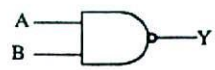
This Boolean expression can be read as Y = not A . B. To perform the Boolean algebra operation, first the inputs must be ANDed and then the inversion is performed. *Note that output from a NAND gate is always 1 except when all of the inputs are 1.* Fig. 27.11 (*iii*) shows the logic symbols for a NAND gate. The little bubble (small circle) on the right end of the symbol means to invert the AND.



(*i*)

Inputs		Output	
A	B	AND (Y')	NAND (Y)
0	0	0	1
1	0	0	1
0	1	0	1
1	1	1	0

(*ii*)



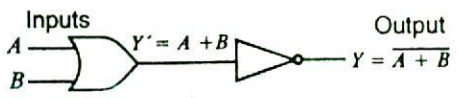
(*iii*)

Fig. 27.11

(*ii*) **NOR gate.** It is a combination of OR gate and NOT gate. In other words, output of OR gate is connected to the input of a NOT gate as shown in Fig. 27.12 (*i*). Note that output of OR gate is inverted to form NOR gate. This is illustrated in the truth table for NOT gate. It is clear that truth

* Note that resistors R_K and R_B form a voltage divider between ground and the negative voltage.

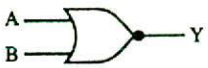
table for NOR gate is developed by *inverting the outputs* of the OR gate.



(*i*)

Inputs		Output	
A	B	OR (Y′)	NOR (Y)
0	0	0	1
1	0	1	0
0	1	1	0
1	1	1	0

(*ii*)



(*iii*)

Fig. 27.12

The Boolean expression for NOR function is

$$Y = \overline{A + B}$$

This Boolean expression can be read as Y = not A or B. To perform the Boolean algebra operation, first the inputs must be ORed and then the inversion is performed. *Note that output from a NOR gate is high (1) only when all the inputs are low (0). If any of the inputs is high (1), the output is low (0).* Fig. 27.12 (*iii*) shows the logic symbol for a NOR gate. The bubble (small circle) at the Y output indicates inversion.

27.13 NAND Gate as a *Universal Gate

The NAND gate is universal gate because its repeated use can produce other logic gates. The table below shows how NAND gates can be connected to produce inverter (*i.e.*, NOT gate), AND gate and OR gate.

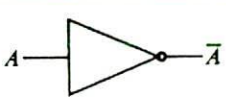
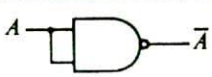
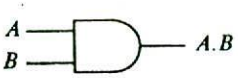
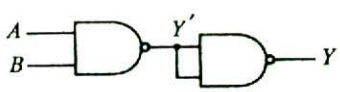
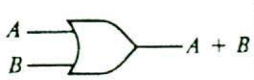
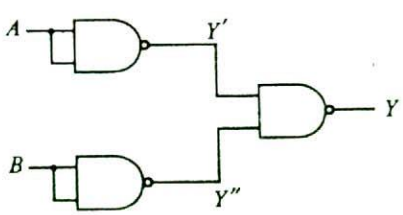
Logic Function	Symbol	Circuit using NAND gates only
Inverter		
AND		
OR		

Fig. 27.13

* It may be noted that NOR gate is also a universal gate.

(*i*) **NOT gate from NAND gate.** When two inputs of NAND gate are joined together so that it has one input, the resulting circuit is NOT gate. The truth table also shows this fact.

A	$B\ (=A)$	Y
0	0	1
1	1	0

(*ii*) **AND gate from NAND gates.** For this purpose, we use two NAND gates in a manner as shown above. The output of first NAND gate is given to the second NAND gate acting as inverter (*i.e.*, inputs of NAND gate joined). The resulting circuit is the AND gate. The output Y' of first NAND gate (AND gate followed by NOT gate) is inverted output of AND gate. The second NAND gate acting as inverter further inverts it so that the final output Y is that of AND gate. The truth table also shows this fact.

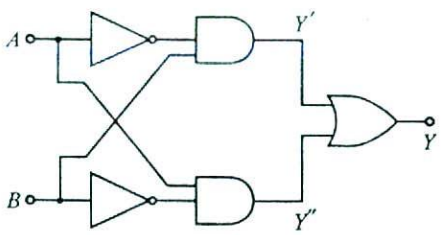
A	B	Y'	Y
0	0	1	0
1	0	1	0
0	1	1	0
1	1	0	1

(*iii*) **OR gate from NAND gates.** For this purpose, we use three NAND gates in a manner as shown above. The first two NAND gates are operated as NOT gates and their outputs are fed to the third. The resulting circuit is OR gate. This fact is also indicated by the truth table.

A	B	$Y' = \overline{A}$	$Y'' = \overline{B}$	Y
0	0	1	1	0
1	0	0	1	1
0	1	1	0	1
1	1	0	0	1

27.14 Exclusive OR Gate

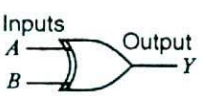
The name exclusive OR gate is usually shortened to XOR gate. The XOR gate can be obtained by using OR, AND and NOT gates as shown in Fig. 27.14 (*i*).



(*i*)

Inputs		Output	
A	B	OR	XOR
0	0	0	0
1	0	1	1
0	1	1	1
1	1	1	0

(*ii*)



(*iii*)

Fig. 27.14

Fig. 27.14 (*ii*) shows the truth table for XOR gate. The table shows that the output is HIGH (1) if any but not all of the inputs are HIGH (1). This *exclusive* feature eliminates the similarity to the OR gate. The OR gate truth table is also given so that you can compare the OR gate truth table with XOR gate truth table. The logic symbol for XOR gate is shown in Fig. 27.14 (*iii*). Note that the symbol is similar to that of OR gate except for the additional curved line at the input side.

The logic operations in the circuit are as under :

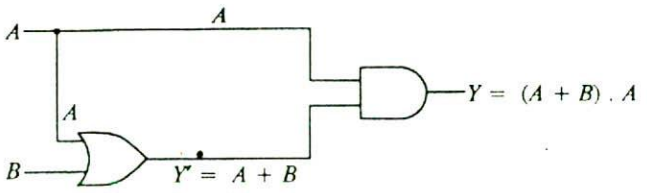
A	B	$\overline{A}$	$\overline{B}$	$\overline{A} \cdot B = Y'$	$A \cdot \overline{B} = Y''$	$Y = Y' + Y''$
0	0	1	1	0	0	0
1	0	0	1	0	1	1
0	1	1	0	1	0	1
1	1	0	0	0	0	0

Note that 0 ANDed with 1 is 0 and 1 ANDed with 1 is 1.

Example 27.4. *Obtain the truth table for the circuit shown in Fig. 27.15 (i).*

Solution. Figure 27.15 (*ii*) shows the truth table for the circuit. The truth table can be obtained

very easily if the reader remembers the following simple Boolean operations :



(i)

A	B	$Y' = A + B$	$Y = Y' . A$
0	0	0	0
1	0	1	1
0	1	1	0
1	1	1	1

(ii)

Fig. 27.15

(i) *0 *ORed with 0 = 0 ; 1 ORed with 1 = 1 ; 1 ORed with 0 = 1*

(ii) *0 **ANDed with 0 = 0 ; 0 ANDed with 1 = 0 ; 1 ANDed with 1 = 1*

Thus, when $A = 0$ and $B = 0$, then A ORed with $B = 0$ *i.e.*, $Y' = 0$. When Y' (= 0) is ANDed with A (= 0), the result is 0. Again when $A = 1$ and $B = 0$, then A ORed with B is 1 *i.e.*, $Y' = 1$. Now Y' (= 1) ANDed with A (= 1), the result is 1.

Example 27.5. *Obtain the truth table for the circuit shown in Fig. 27.16.*

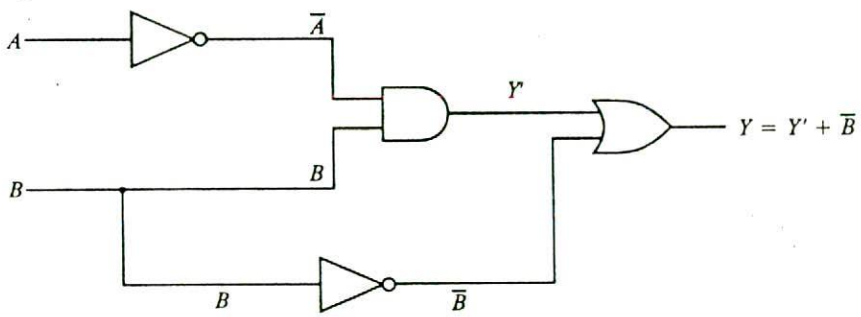


Fig. 27.16

Solution. The truth table for the circuit is shown below :

A	B	$\overline{A}$	$Y' = \overline{A} \cdot B$	$\overline{B}$	$Y = Y' + \overline{B}$
0	0	1	0	1	1
1	0	0	0	1	1
0	1	1	1	0	1
1	1	0	0	0	0

(i) When $A = 0$ and $B = 0$, then $\overline{A} = 1$. Now Y' is equal to $\overline{A}$ (= 1) ANDed with B (= 0). The result is 0. Then Y' (= 0) ORed with $\overline{B}$ (= 1) is 1 *i.e.*, $Y = 1$.

(ii) When $A = 1$ and $B = 0$, then $\overline{A} = 0$. Now Y' is equal to $\overline{A}$ (= 0) ANDed with B (= 0) and the result is 0 *i.e.*, $Y' = 0$. Then Y' (= 0) ORed with $\overline{B}$ (= 1) is 1 *i.e.*, $Y = 1$.

The reader can proceed in a similar way to find the other output values.

---

* Note that $A + B$ means A ORed with B.

** Note that $A . B$ means A ANDed with B.

27.15 Encoders and Decoders

A digital circuit can process numbers in binary form. However, most of the information we handle is in decimal form. Therefore, a digital machine must perform the following functions :

(*i*) Convert the information from decimal to digital (binary) form.

(*ii*) Process the digital information.

(*iii*) Convert the digital output back to decimal form.

The circuit that converts decimal form to digital (binary) form is called **encoder** and the circuit that converts digital form to decimal form is called **decoder.** Fig. 27. 17 shows encoding and decoding in a digital calculator. Here the input is the decimal number 5 punched in at the keyboard. The encoder changes the decimal number 5 to the digital form as the binary digit 0101. The central

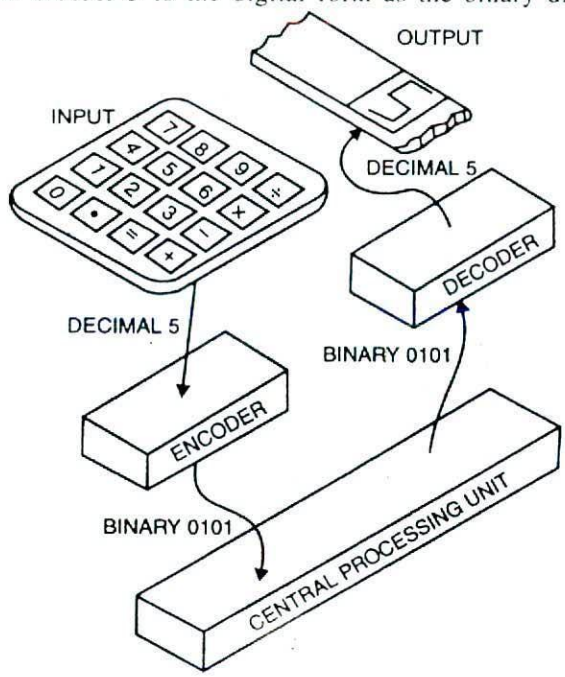


Fig. 27.17

processing unit (CPU) contains digital logic circuits for necessary calculations. Here all operations are carried out in binary form. The output of CPU is fed to the decoder which changes the binary signal back to the decimal form. The output display is in the decimal form, showing the original number 5.

27.16 Advantages and Disadvantages of Digital Electronics

The world of electronics can be classified as either digital or analog circuits. An increasing majority of applications in electronics use digital techniques to perform operations that were once performed using analog methods. It is worthwhile to give advantages and disadvantages of digital electronics.

Advantages. The chief reasons for the shift to digital technology are :

(*i*) *Digital systems are generally easier to design.* It is because the circuits that are used are *switching circuits* where *exact* values of voltages or current are not important, only the range (HIGH or LOW) in which they fall is important.

(*ii*) *Digital circuits provide greater accuracy and precision.* It is because digital circuits can handle as many digits of precision as you need simply by adding more switching circuits. In analog systems, precision is usually limited to three or four digits because the values of voltage and current are directly dependent on the circuit components.

(*iii*) *Digital circuits are less affected by noise.* Suprious fluctuations in voltage (noise) are not as critical in digital systems as in analog systems. It is because in a digital circuit, the exact value of a voltage is not important as long as the noise is not large enough to prevent us from distinguishing a HIGH from a LOW.

(*iv*) *More digital circuitry can be fabricated on IC chips.* Analog system uses such devices (high-value capacitors, inductors, transformers) that cannot be economically integrated. For this reason, analog systems cannot achieve the same degree of integration as digital circuits.

(*v*) Information storage is easy with digital circuits.

Disadvantages. (*i*) The real world is mainly analog. However, the digital circuits can handle only digital signals. This necessitates encoders and decoders which increase the cost of the equipment.

(*ii*) There are situations where using only analog techniques is simpler and more economical. For example, the process of signal amplification is most easily accomplished using analog circuitry.

However, advantages of digital techniques outweigh the disadvantages. For this reason, we are fast switching to digital techniques.

27.17 Boolean Algebra

Digital circuits perform the binary arithmetic operations with binary digits 1 and 0. These operations are called logic functions or logical operations. *The algebra used to symbolically describe logic functions is called* **Boolean algebra.** Boolean algebra is a set of rules and theorems by which logical operations can be expressed symbolically in equation form and be manipulated mathematically. As with the ordinary algebra, the *letters of alphabet (*e.g. A, B, C* etc) can be used to represent the variables. Boolean algebra differs from ordinary algebra in that Boolean constant and variables can have only two values ; 0 and 1. There are four connecting symbols used in Boolean algebra *viz.*

(*i*) equals sign (=) (*ii*) plus sign (+)

(*iii*) multiply sign (·) (*iv*) bar (–)

(*i*) **Equals sign (=).** The equals sign in Boolean algebra refers to the standard mathematical equality. In other words, the logical value on one side of the sign is identical to the logical value on the other side of the sign. Suppose we are given two logical variables such that $A = B$. Then if $A = 1$, then $B = 1$ and if $A = 0$, then $B = 0$.

(*ii*) **Plus sign (+).** The plus sign in Boolean algebra refers to the logical *OR operation*. Thus, when the statement $A + B = 1$ appears in Boolean algebra, it means A ORed with B equals 1. Consequently, either $A = 1$ or $B = 1$ or both equal 1.

(*iii*) **Multiply sign (·).** The multiply sign in Boolean algebra refers to *AND operation*. Thus, when the statement $A \cdot B = 1$ appears in Boolean algebra, it means A ANDed with B equals 1. Consequently, $A = 1$ and $B = 1$. The function $A \cdot B$ is often written as AB, omitting the dot for convenience.

(*iv*) **Bar sign (–).** The bar sign in Boolean algebra refers to *NOT operation*. The NOT has the effect of inverting (complementing) the logical value. Thus, if $A = 1$, then $\overline{A} = 0$.

* For example, A might represent a certain digital circuit input or output and at any time, we must have either $A = 0$ or $A = 1$.

27.18 Boolean Theorems

We now discuss the basic Boolean theorems that are useful in manipulating and simplifying Boolean expressions. For convenience, we divide the theorems into two groups :

(*i*) Single variable theorems.

(*ii*) Multivariable theorems.

(*i*) **Single variable theorems.** These theorems refer to the condition when only one input to the logic gate is variable. Table 27.1 gives single variable Boolean theorems.

Table 27.1

Theorem 1 :	$A + 0 = A$
Theorem 2 :	$A \cdot 1 = A$
Theorem 3 :	$A + \overline{A} = 1$
Theorem 4 :	$A \cdot \overline{A} = 0$
Theorem 5 :	$A + A = A$
Theorem 6 :	$A \cdot A = A$
Theorem 7 :	$A + 1 = 1$
Theorem 8 :	$A \cdot 0 = 0$
Theorem 9 :	$\overline{\overline{A}} = A$

Theorem 1. $(A + 0 = A)$. This theorem can be verified by ORing a variable A with a 0 and is illustrated in Fig. 27.18. Here one input to OR gate is always 0 and the other input A can be a value 1 or 0. When A is at 1, the output is 1 which is equal to A. When A is at 0, the output is 0 which is also equal to A $(= 0)$. Therefore, a variable ORed with 0 is equal to the value of the variable. This is easy to remember since 0 added to anything does not effect the value of the variable, either in regular addition or OR addition.

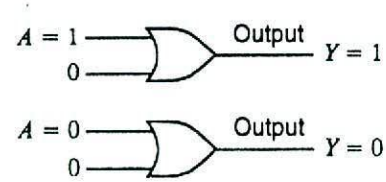


Fig. 27.18

Theorem 2. $(A \cdot 1 = A)$. This theorem can be verified by ANDing a variable A with a 1 and is illustrated in Fig. 27.19. Here one input to AND gate is always 1 and the other can be a value 1 or 0. If A is 1, the output of the AND gate is 1 because both the inputs are now 1's. If A is 0, the output of the AND gate is a 0. Therefore, a variable ANDed with a 1 is equal to the value of the variable $(A \cdot 1 = A)$. This is easy to remember because AND operation is just like ordinary multiplication.

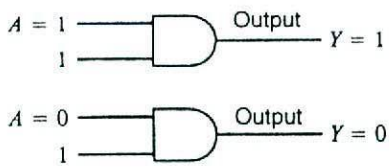


Fig. 27.19

Theorem 3. $\left(A + \overline{A} = 1\right)$. This theorem can be easily explained. If a variable A and its complement $(\overline{A})$ are ORed, the result is always 1. If A is a 0, then $0 + \overline{0} = 0 + 1 = 1$. If A is a 1, then $1 + \overline{1} = 1 + 0 = 1$. Fig. 27.20 illustrates this theorem.

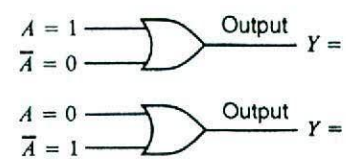


Fig. 27.20

Theorem 4. $(A \cdot \overline{A} = 0)$. This theorem states that if a variable A is ANDed with its complement, the result is zero. This is readily apparent because either A or $\overline{A}$ will always be 0. Therefore, when one of the inputs to an AND gate is 0, the output is always 0. Fig. 27.21 illustrates this theorem.

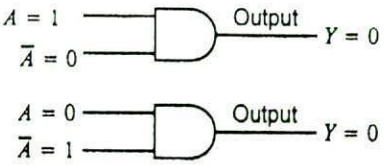


Fig. 27.21

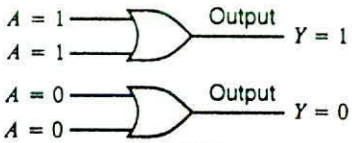


Fig. 27.22

Theorem 5. $(A + A = A)$. This theorem states that when a variable A is ORed with itself, the output is equal to the variable. Thus, if A is a 0, then $0 + 0 = 0$ and if A is a 1, then $1 + 1 = 1$. Fig. 27.22 illustrates this theorem.

Theorem 6. $(A \cdot A = A)$. This theorem states that if a variable A is ANDed with itself, the result is equal to the variable. For example, if $A = 0$, then $0 \cdot 0 = 0$ and if $A = 1$, then $1 \cdot 1 = 1$. For either case, the output of an AND gate is equal to the value of the input variable A. Fig. 27.23 illustrates this theorem.

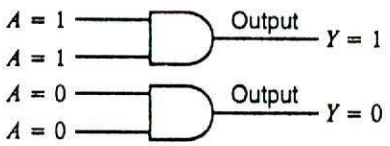


Fig. 27.23

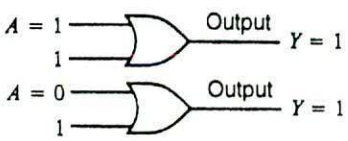


Fig. 27.24

Theorem 7. $(A + 1 = 1)$. This theorem states that when a variable A is ORed with 1, the outuput is always equal to 1. Fig. 27.24 illustrates this theorem. One input to an OR gate is always 1 and the other input A can be either 1 or 0. Now 1 on an input to OR gate produces 1 on the output regardless of the value of the variable on the other input.

Theorem 8. $(A \cdot 0 = 0)$. This theorem states that variable A ANDed with 0 always produces 0. Recall that any time one input to an AND gate is 0, the output is 0 regardless of the value of the vartable A on the other input. This theorem is illustrated in Fig. 27.25.

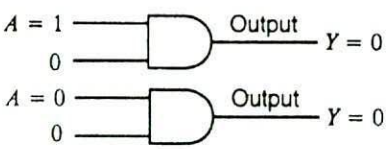


Fig. 27.25

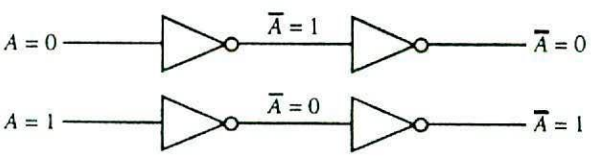


Fig. 27.26

Theorem 9. $\left(\overline{\overline{A}} = A\right)$. This theorem states that if a variable A is complemented twice, the result is the variable itself. Starting with A and inverting (complementing) it once gives $\overline{A}$. Inverting it once more gives A – the original value. This theorem is illustrated in Fig. 27.26.

Duality Principle. Before moving to multivariable theorems, this would be the right place to mention an important property of Boolean algebra called *duality principle*. It is stated below :

The duality principle states that a Boolean expression remains valid if operators OR and AND are interchanged and 1's and 0's in the expression are also interchanged.

In order to understand this principle, consider the Boolean Theorem 1 *viz.*

$$A + 0 = A$$

According to duality principle, this Boolean expression remains valid if OR function is replaced by AND function and 0 by 1. In that case, the Boolean expression becomes :

$$A \cdot 1 = A$$

Note that this is Boolean Theorem No. 2. Therefore, Boolean Theorem 2 is dual of Boolean Theorem 1 and *vice-versa*. Applying duality principle, Theorem 4 is dual of Theorem 3 and *vice-versa*, Theorem 6 is dual of Theorem 5 and *vice-versa*, Theorem 8 is dual of Theorem 7 and *vice-versa*. To apply duality principle to a Boolean expression, we simply interchange OR and AND operator and replace 1's by 0's and 0's by 1's.

(*ii*) **Multivariable theorems.** These theorems refer to the condition when more than one input to the logic gate are variable. Table 27.2 gives multivariable Boolean theorems.

Table 27.2

Theorem 10 :	$A + B = B + A$	} *Commutative Law*
Theorem 11 :	$A \cdot B = B \cdot A$	
Theorem 12 :	$A + (B + C) = (A + B) + C$	} *Associative Law*
Theorem 13 :	$A \cdot (B \cdot C) = (A \cdot B) \cdot C$	
Theorem 14 :	$A \cdot (B + C) = A \cdot B + A \cdot C$	} *Distributive Law*
Theorem 15 :	$(A + B) \cdot (C + D) = A \cdot C + B \cdot C + A \cdot D + B \cdot D$	
Theorem 16 :	$A + A \cdot B = A$	} *De Morgan's Theorems*
Theorem 17 :	$\overline{(A + B)} = \overline{A} \cdot \overline{B}$	
Theorem 18 :	$\overline{(A \cdot B)} = \overline{A} + \overline{B}$	

The following points may be noted about these theorems :

(*a*) Theorems 10 and 11 obey **commutative law**. *This law states that the order in which the variables are ORed or ANDed makes no difference.*

Fig. 27.27

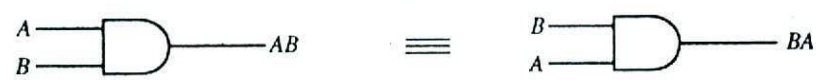


Fig. 27.28

Figure 27.27 illustrates the commutative law as applied to the OR gate while Fig. 27.28 illustrates the commutative law as applied to an AND gate.

(*b*) Theorems 12 and 13 obey **associative law.** *This law states that in the ORing or ANDing of several variables, the result is the same regardless of the grouping of the variables.*

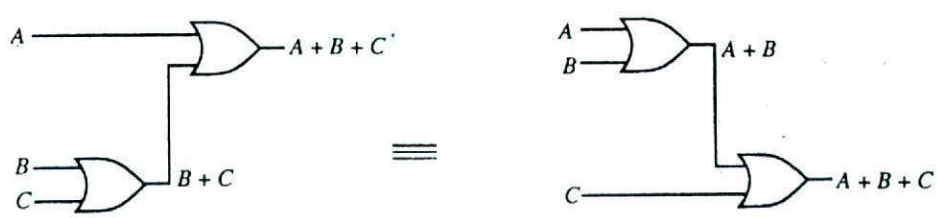


Fig. 27.29

Fig. 27.30

Figure 27.29 illustrates the associative law as applied to the OR gate, while Fig. 27.30 illustrates the associative law as applied to an AND gate.

(*c*) Theorems 14 and 15 obey **distributive law**. *This law states that a Boolean expression can be expanded by multiplying term-by-term just the same as in ordinary algebra.*

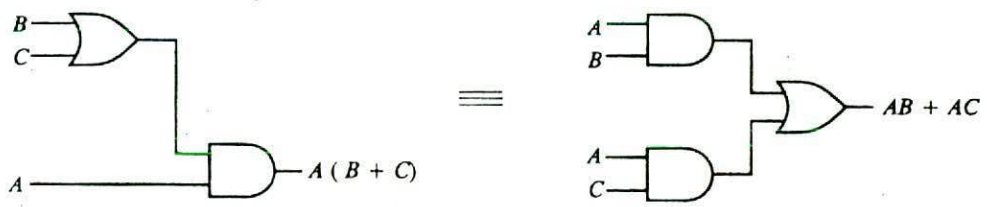


Fig. 27.31

Fig. 27.31 illustrates the distributive law in terms of gate implementation.

(*d*) We will prove Theorem 16 by factoring and using Theorems 2, 7, 10 and 14.

$$\begin{aligned} A + A \cdot B &= A \cdot 1 + A \cdot B && \text{...Theorem 2} \\ &= A \cdot (1 + B) && \text{...Theorem 14} \\ &= A \cdot (B + 1) && \text{...Theorem 10} \\ &= A \cdot 1 && \text{...Theorem 7} \\ &= A && \text{...Theorem 2} \end{aligned}$$

(*e*) Theorems 17 and 18 are the two most important theorems of Boolean algebra and were contributed by the great mathematician named *DeMorgan*. Therefore, these theorems are called De Morgan's theorems.

27.19 De Morgan's Theorems

DeMorgan's theorems are extremely useful in simplifying expressions in which a product or sum of variables is inverted.

The two theorems are :

(*i*) $\overline{(A+B)} = \overline{A} \cdot \overline{B}$

(*ii*) $\overline{(A.B)} = \overline{A} + \overline{B}$

(*i*) The first De Morgan's theorem may be stated as under :

When the OR sum of two variables is inverted, this is equal to inverting each variable individually and then ANDing these inverted variables i.e.,

$$\overline{(A+B)} = \overline{A} \cdot \overline{B}$$

In this expression, A and B are the two variables. The L.H.S. is the complement of the OR sum of the two variables. The R.H.S is the AND product of individual inverted variables.

(*ii*) The second De Morgan's theorem may be stated as under :

When the AND product of two variables is inverted, this is equal to inverting each variable individually and then ORing them i.e.,

$$(\overline{A \cdot B}) = \overline{A} + \overline{B}$$

In this expression, A and B are the two variables. The L.H.S. is the complement of the AND product of the two variables. The R.H.S. is the OR sum of the individual inverted variables.

27.20 Operator Precedence

The operator precedence for evaluating Boolean expression is (*i*) parentheses (*ii*) NOT (*iii*) AND and (*iv*) OR. In other words, the expression inside the parenthesis must be evaluated before all other operations. The next operation that holds precedence is the complement, then follows the AND and finally the OR. For example, consider the Boolean expression :

$$A + \overline{B} \,.\, (C + D)$$

The sequence of operations will be :

(*i*) The expression inside the parenthesis (*i.e.* $C + D$) will be evaluated first.

(*ii*) Then $\overline{B}$ will be evaluated.

(*iii*) Then the results of the two (*i.e.* $\overline{B}$ and $C + D$) will be ANDed.

(*iv*) Finally, the result of the product will be ORed with A.

Example 27.6. *Using Boolean algebraic techniques, simplify the following expression* :

$$Y = A \cdot B \cdot \overline{C} \cdot \overline{D} + \overline{A} \cdot B \cdot \overline{C} \cdot \overline{D} + \overline{A} \cdot B \cdot C \cdot \overline{D} + A \cdot B \cdot C \cdot \overline{D}$$

Solution. $$Y = A \cdot B \cdot \overline{C} \cdot \overline{D} + \overline{A} \cdot B \cdot \overline{C} \cdot \overline{D} + \overline{A} \cdot B \cdot C \cdot \overline{D} + A \cdot B \cdot C \cdot \overline{D} \quad ...(i)$$

Step 1 : Take out the common factors as below :

$$Y = B\,\overline{C}\,\overline{D}\,(A + \overline{A}) + B\,C\,\overline{D}\,(A + \overline{A})$$

Step 2 : Apply Theorem 3 $(A + \overline{A} = 1)$:

$$Y = B\,\overline{C}\,\overline{D} + B\,C\,\overline{D}$$

Step 3 : Again factorize :

$$Y = B\,\overline{D}\,(C + \overline{C})$$

Step 4 : Apply Theorem 3 $(C + \overline{C} = 1)$:

$$Y = B\,\overline{D} \cdot 1 = B\overline{D}$$

This is the simplified form of exp. (*i*).

Example 27.7. *Using Boolean techniques, simplify the following expression* :

$$Y = AB + A\,(B + C) + B\,(B + C)$$

Solution. $$Y = AB + A\,(B + C) + B\,(B + C) \quad ...(i)$$

Step 1 : Apply Theorem 14 (distributive law) to second and third terms:

$$Y = AB + AB + AC + BB + BC$$

Step 2 : Apply Theorem 6 $(B \cdot B = B)$:

$$Y = AB + AB + AC + B + BC$$

Step 3 : Apply Theorem 5 $(AB + AB = AB)$:

$$Y = AB + AC + B + BC$$

Step 4 : Factor B out of last 2 terms :

$$Y = AB + AC + B(1 + C)$$

Step 5 : Apply commutative law and Theorem 7 $(1 + C = C + 1 = 1)$:

$$Y = AB + AC + B \cdot 1$$

Step 6 : Apply Theorem 2 $(B \cdot 1 = B)$:

$$Y = AB + AC + B$$

Step 7 : Factor B out of first and third terms :

$$Y = B(A + 1) + AC$$

Step 8 : Apply Theorem 7 $(A + 1 = 1)$:

$$Y = B \cdot 1 + AC$$

Step 9 : Apply Theorem 2 $(B \cdot 1 = B)$:

$$Y = B + AC$$

This is the simplified form of exp. (*i*).

Example 27.8. *Simplify the following Boolean expressions to a minimum number of literals* :

(*i*) $Y = A + \overline{A}B$ (*ii*) $Y = AB + \overline{A}C + BC$

Solution. (*i*)

$$Y = A + \overline{A}B$$

$$= A + AB + \overline{A}B \qquad [\because A = A + AB \text{ from Theorem 16}]$$

$$= A + B(A + \overline{A})$$

$$= A + B \qquad [\because A + \overline{A} = 1 \text{ from Theorem 3}]$$

$\therefore$ $Y = A + B$

(*ii*)

$$Y = AB + \overline{A}C + BC$$

$$= AB + \overline{A}C + BC \cdot (A + \overline{A})$$

$$= AB + \overline{A}C + ABC + \overline{A}BC$$

$$= AB(1 + C) + \overline{A}C\ (1 + B)$$

$$= AB + \overline{A}C$$

$\therefore$ $Y = AB + \overline{A}C$

Example 27.9. *Determine output expression for the circuit shown below and simplify it using De Morgan's theorem.*

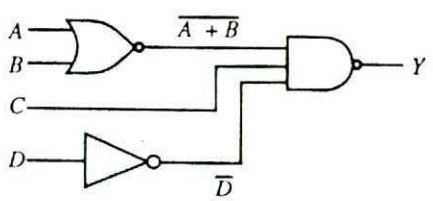


Fig. 27.32

Solution. The output expression for the circuit shown above is :

$$Y = \overline{[\overline{(A + B)} \cdot C \cdot \overline{D}]}$$

Using De Morgan's theorem :

$$Y = (A + B) + \overline{C} + D$$

$\therefore$ $Y = A + B + \overline{C} + D$

Example 27.10. *Find the complement of the expressions given below :*

(*i*) $Y = AB\overline{C} + A\overline{B}\overline{C}$

(*ii*) $Y = \overline{A} + (B\overline{C} + \overline{B}C)$

Solution. (*i*) $Y = AB\overline{C} + A\overline{B}\overline{C}$

$$\overline{Y} = \overline{(AB\overline{C} + A\overline{B}\overline{C})}$$

Applying De Morgan's theorem :

$$\overline{Y} = \overline{(AB\overline{C})} \cdot \overline{(A\overline{B}\overline{C})}$$

Again applying De Morgan's theorem to the each expression inside the brackets :

$$\overline{Y} = (\overline{A} + B + C) \cdot (\overline{A} + \overline{B} + C)$$

(*ii*) $Y = \overline{A}(BC + \overline{B}C)$

$$\overline{Y} = \overline{\overline{A}(BC + \overline{B}C)}$$

Applying De Morgan's theorem :

$$\overline{Y} = A + \overline{(B\overline{C} + \overline{B}C)}$$

Again applying De Morgan's theorem to the expression inside the brackets :

$$\overline{Y} = A + \overline{(B\overline{C})} \cdot \overline{(\overline{B}C)}$$

Applying De Morgan's theorem for the third time we get :

$$\overline{Y} = A + (\overline{B} + C) \cdot (B + \overline{C})$$

or $$\overline{Y} = A + \overline{B}\overline{C} + BC$$

Example 27.11. *Simplify the following Boolean expressions :*

(*i*) $Y = (A + B + C) \cdot (A + B)$

(*ii*) $Y = AB + ABC + AB\overline{C}$

(*iii*) $Y = 1 + A(B \cdot \overline{C} + BC + \overline{B}\,\overline{C}) + A\overline{B}C + AC$

(*iv*) $Y = \overline{(A + \overline{B} + C) + (B + \overline{C})}$

Solution. (*i*) $Y = (A + B + C) \cdot (A + B)$

$$= A \cdot A + A \cdot B + B \cdot A + B \cdot B + C \cdot A + C \cdot B$$

Using $A \cdot A = A$, we get,

$$Y = A + AB + AB + B + AC + BC$$

$$= A + AB + B + AC + BC \qquad [\because AB + AB = AB]$$

$$= A + B + AC + BC \qquad [\because A + AB = A]$$

$$= A(1 + C) + B(1 + C)$$

$$= A \cdot 1 + B \cdot 1 \qquad [\because 1 + C = 1]$$

$\therefore$ $$Y = A + B$$

(*ii*) $$Y = AB + ABC + AB\overline{C}$$

$$= AB + AB(C + \overline{C})$$

$$= AB + AB \qquad [\because C + \overline{C} = 1]$$

$\therefore$ $$Y = AB$$

(*iii*) $$Y = 1 + A(B \cdot \overline{C} + BC + \overline{B}\,\overline{C}) + A\overline{B}C + AC$$

Using $1 + A = 1$, we get,

$$Y = 1 + A\overline{B}C + AC \qquad [\because 1 + A(B\overline{C} + BC + \overline{B}\,\overline{C}) = 1]$$

$$= 1 + AC$$

$\therefore$ $$Y = 1$$

Thus, because of the first term Y reduces to 1. Therefore, any Boolean expression ORed with 1, results in 1.

(*iv*) $$Y = \overline{(A + \overline{B} + C) + (B + \overline{C})}$$

Applying De Morgan's theorem :

$$Y = \overline{(A + \overline{B} + C)} \cdot \overline{(B + \overline{C})}$$

Again applying De Morgan's theorem :

$$Y = (\overline{A} \cdot B \cdot \overline{C}) \cdot (\overline{B} \cdot C) = 0 \qquad [\because B \cdot \overline{B} = 0,\ C \cdot \overline{C} = 0]$$

Example 27.12. *Simplify the following Boolean expression* :

$$Y = A\,\overline{B}\,D + A\,\overline{B}\,\overline{D}$$

Solution. $$Y = A\,\overline{B}\,D + A\,\overline{B}\,\overline{D}$$

Factor out the common variables $A\,\overline{B}$ (using Theorem 14), we get :

$$Y = A\,\overline{B}(D + \overline{D})$$

Using Theorem 3, $D + \overline{D} = 1$:

$\therefore$ $$Y = A\,\overline{B} \cdot 1$$

Using Theorem 2, we get :

$$Y = A\,\overline{B}$$

Example 27.13. *Simplify the following Boolean expression* :

$$Y = (\overline{A} + B)(A + B)$$

Solution. $$Y = (\overline{A} + B)(A + B)$$

The expression can be expanded by multiplying out the terms. [Theorem 15].

$$Y = \overline{A} \cdot A + \overline{A} \cdot B + B \cdot A + B \cdot B$$

Using Theorem 4, $\overline{A} \cdot A = 0$. Also $B \cdot B = B$ [Theorem 6].

$\therefore$ $$Y = 0 + \overline{A} \cdot B + B \cdot A + B$$

$$= \overline{A} \cdot B + AB + B$$

Factoring out the variable B [Theorem 14], we have,

$$Y = B(\overline{A} + A + 1)$$

Using Theorem 7, $A + 1 = 1$.

$\therefore$ $$Y = B(\overline{A} + 1)$$

Again using Theorem 7, $\overline{A} + 1 = 1$.

$\therefore$ $$Y = B \cdot 1$$

Finally, using Theorem 2, we have,

$$Y = B$$

Multiple-Choice Questions

1. The binary number 10101 is equivalent to decimal number .....
   (*i*) 19 (*ii*) 12
   (*iii*) 27 (*iv*) 21
2. The universal gate is .....
   (*i*) NAND gate (*ii*) OR gate
   (*iii*) NOT gate (*iv*) none of the above
3. The inverter is .....
   (*i*) NOT gate (*ii*) OR gate
   (*iii*) AND gate (*iv*) none of the above
4. The inputs of a NAND gate are connected together. The resulting circuit is .....
   (*i*) OR gate (*ii*) AND gate
   (*iii*) NOT gate (*iv*) none of the above
5. The NOR gate is OR gate followed by .....
   (*i*) AND gate (*ii*) NAND gate
   (*iii*) NOT gate (*iv*) none of the above
6. The NAND gate is AND gate followed by .....
   (*i*) NOT gate (*ii*) OR gate
   (*iii*) AND gate (*iv*) none of the above
7. Digital circuit can be made by the repeated use of .....
   (*i*) OR gates (*ii*) NOT gates
   (*iii*) NAND gates (*iv*) none of the above
8. The only function of NOT gate is to .....
   (*i*) stop a signal
   (*ii*) invert input signal
   (*iii*) act as a universal gate
   (*iv*) none of the above
9. When an input signal 1 is applied to a NOT gate, the output is .....
   (*i*) 0 (*ii*) 1
   (*iii*) either 0 or 1 (*iv*) none of the above
10. In Boolean algebra, the bar sign (–) indicates .....
    (*i*) OR operation
    (*ii*) AND operation
    (*iii*) NOT operation
    (*iv*) none of the above
11. The given Boolean expression is

    $$Y = A\overline{B} + B\overline{A}$$

    If $A = 1$ and $B = 1$, then $Y =$
    (*i*) 1 (*ii*) 0
    (*iii*) either 1 or 0 (*iv*) none of the above
12. In Boolean algebra, the plus sign (+) indicates .....
    (*i*) AND operation
    (*ii*) OR operation
    (*iii*) NOT operation
    (*iv*) none of the above
13. $\overline{(A + B)}$ = ...
    (*i*) $\overline{A} + \overline{B}$ (*ii*) $\overline{A} - \overline{B}$
    (*iii*) $\overline{A} \cdot \overline{B}$ (*iv*) none of the above
14. $\overline{(A \cdot B)}$ = ...
    (*i*) $\overline{A} + \overline{B}$ (*ii*) $\overline{A} \cdot \overline{B}$
    (*iii*) $\overline{A} - \overline{B}$ (*iv*) none of the above
15. $A + A \cdot B$ = ...
    (*i*) B (*ii*) A
    (*iii*) $\overline{A} + B$ (*iv*) none of the above

Answers to Multiple-Choice Questions

1. (*iv*)	**2.** (*i*)	**3.** (*i*)	**4.** (*iii*)	**5.** (*iii*)
6. (*i*)	**7.** (*iii*)	**8.** (*ii*)	**9.** (*i*)	**10.** (*iii*)
11. (*ii*)	**12.** (*ii*)	**13.** (*iii*)	**14.** (*i*)	**15.** (*ii*)

Chapter Review Topics

1. Write a short note on analog and digital signals.
2. What is a digital circuit ?
3. What is binary number system ?
4. How will you make decimal to binary conversion ?
5. How will you make binary to decimal conversion ?
6. What is a logic gate ?
7. What are the three basic logic gates ?
8. Describe OR function with a 2-input OR gate.
9. Explain AND function with a 2-input AND gate.
10. What is a NAND gate ?
11. What is a NOR gate ?
12. How will you obtain NOT gate from NAND gate ?
13. What is indicated by plus (+), dot (.) and bar (—) in a Boolean expression ?
14. State De Morgan's theorems.
15. What are encoders and decoders ?

Problems

1. Convert decimal number 23 into equivalent binary number. $[(10111)_2]$
2. Simplify the expression $Y = A\,C\,D + \overline{A}\,B\,C\,D.$ $[Y = A\overline{C} + \overline{B}D]$
3. Simplify the expression $Y = \overline{(\overline{A} + C) \cdot (B + \overline{D})}$ to one having only single variables inverted. $[Y = A\overline{C} + \overline{B}D]$
4. Find the complement function of $Y = \overline{A}\,B\,\overline{C} + \overline{A}\,\overline{B}\,C.$ $[(A + \overline{B} + C)(A + B + \overline{C})]$
5. Simplify the expression $Y = A \cdot B + A \cdot \overline{B}$. $[Y = A]$
6. Simplify the expression $Y = A \cdot B \cdot C + B \cdot C.$ $[Y = B \cdot C]$
7. Simplify the following Boolean expression to a minimum number of literals :
$$Y = A(\overline{A} + B)$$ $[Y = AB]$
8. Simplify the following Boolean function to a minimum number of literals :
$$Y = \overline{A}\,\overline{B}\,C + \overline{A}\,B\,C + A\,\overline{B}$$ $[Y = \overline{A}\,C + A\overline{B}]$
9. Simplify the expression : $Y = (A + B)(\overline{A} + C)(B + C)$ $[Y = (A + B)(\overline{A} + C)]$
10. Find the complement of the function :
$$Y = A(\overline{B}\,\overline{C} + B\,C)$$ $[\overline{Y} = \overline{A} + (B + C)(\overline{B} + \overline{C})]$

Discussion Questions

1. Why is logic circuit name so ?
2. What is the importance of digital techniques ?
3. Why is analog system unreliable ?
4. What is the importance of NAND gate ?
5. What is Boolean algebra ?
6. What is the importance of De Morgan's theorems in Boolean Algebra ?

7. What is the meaning of + sign in Boolean expression ?
8. Give two differences between decimal and binary systems.
9. What are the disadvantages of digital circuits ?
10. What are the advantages of Boolean theorems ?
11. What is the meaning of sign . in Boolean expression ?
12. What is a universal gate ? Why is it so named?
13. Most of information we handle is in decimal form. Will a digital circuit process this information as such?
14. What role is played by encoder and decoder?