

Index

- abstraction levels, circuit design, 7, 8
- accelerometers, 4–5
- active current mirrors, 145–58; common-mode properties, 154–58; differential pair with, 148, 150, 151, 154, 190; large-signal analysis of, 149–51; small-signal analysis, 151–54; small-signal behavior in, 145–48
- active devices, 611–16; back-end processing, 614–16; basic transistor fabrication, 611–14; fabrication, 611–16
- ADC. *See* analog-to-digital converter
- amplification mode: noninverting amplifiers, 432–433, 436, 437; unity-gain sampler, 424–25, 429–30
- amplifiers: auxiliary, 312; cascade of, 170; continuous-time feedback, 405–7; current, 254–56; differential, 100–34; frequency response of, 166–200; noise in single-stage, 224–33; noninverting, 432–38; nonlinear, 448–63; one-pole feedforward, 348; operational, 291–344; output port, 66–67; single-stage, 47–99, 224–33; switched-capacitor, 423–39; transconductance, 254–56; transimpedance, 254–56; types of, 254–56; variable gain, 126–28; voltage, 254–56, 461
- amplitude: distribution, 206–7; limiting, 487–95; output, 512
- analog design, 600; introduction to, 1–8; in microprocessors and memories, 5–6; octagon, 48; robust, 7–8
- analog layout techniques, 635–60; multifinger transistors, 635–37; passive devices, 644–53; reference distribution, 642–44; symmetry, 637–42
- analog-to-digital converter (ADC), 1–2
- antenna effect, 634–35
- asymmetry, 120–24, 151–52. *See also* symmetry
- auxiliary amplifiers, 312
- average power, 202–3

- back-end processing, 614–16
- bandgap references, 377–404; case study, 397–400; defined, 389; floating, 398–99; general considerations, 377; speed and noise issues, 393–97; temperature-independent references, 384–90. *See also* reference distribution
- bandwidth: large-signal, 295; modification, 252–54; noise, 239; small-signal, 293–95
- Barkhausen's Criteria, 346, 483, 487
- biasing: constant- G_m , 392–93; supply-independent, 377–81
- binary data, 2–3

- Bode plots, 346–47, 349, 357, 359, 362, 364, 547, 561
- body effect, 23–25; source follower, 71
- bonding pads, 657–59
- bootstrapping, 566–67
- bottom-plate sampling, 423
- bounce, 663–65, 668
- BSIMs, 591–92, 596–97
- bulk, 12; NFETs and PFETs, 36
- bulk voltage, 23–25
- bypass capacitors, 673

- cancellation, offset, 471–78
- capacitance: fringe, 626; load, 169–70; mutual, 675; parallel, 626–27; parasitic, 171; self-, 675
- capacitance modeling, MOS device models, 598
- capacitive coupling, reducing, 654
- capacitor nonlinearity, 457–58
- capacitors: accelerometer, 4–5; behavior of MOS devices as, 38–39; bypass, 673; layout in passive devices, 650–52; metal-poly, 620–21; monolithic, 423–24; MOS, 621–24; in passive MOS devices, 619–24; poly-diffusion, 619–20; poly-poly, 620; voltage-dependent, 521–22. *See also* capacitor nonlinearity; switched-capacitor circuits
- cascode current mirrors, 139–45
- cascode current source, 140–45
- cascode devices, layout, 638
- cascode differential pair, 126
- cascode operational amplifiers, 292, 298–99; folded, 301–7; telescopic, 297–99, 303–4, 306
- cascode stage, 83–92; frequency response, 185–87; gain boosting in, 310–11; input-output characteristic, 84; model, 186; output impedance, 85–86, 88; shielding property, 89–90; single-stage amplifiers, 232–33; small-signal characteristics, 84–85
- cascode: folded, 90–92; low-voltage, 143–45; self-biased, 398; triple, 307
- center frequency in voltage-controlled oscillators (VCOs), 511
- CG stage. *See* common-gate stage
- channel, long versus short, 38
- channel charge injection, 418–20; cancellation, 421–23
- channel-length modulation, 25–27
- channel resistance, of MOS capacitors, 622–24
- channeling, 609–10

- charge injection, channel, 418–20, 421–23
- charge modeling, MOS device models, 598
- charge-pump phase-locked loops (CPPLLs), 549–62;
 - basic, 555–62; charge pumps, 550–55;
 - dynamics, 557–61; linearity, 557;
 - lock acquisition, 549–62;
 - phase/frequency detector, 550–55;
 - stability issues, 561–62; transfer function, 557–61
- charge pumps: in charge-pump phase-locked loops (CPPLLs), 550–55; PFD/CP nonidealities, 562–67
- charge redistribution in noninverting amplifier, 434
- chemical vapor deposition (CVD), 611
- circuit design, abstraction levels, 7, 8
- circuit symbols, MOS, 12–13
- circuits: bandgap reference, 377–404; closed-loop, 250–53;
 - common-gate, 250; differential, 452–54; digital, 12;
 - feedback, 247–54; guard rings for, 663; half, 113–18;
 - noise represented in, 218–24; open-loop, 250,
 - 253–54; precision multiply-by-two, 438–39, 622;
 - RLC, 496–99; sampling, 410–14;
 - switched-capacitor, 405–47
- clamp transistors, 332–33
- clock: amplification and offset modes controlled by, 472;
 - edges, 427; feedthrough, 420–22
- closed-loop circuits, 250–53
- closed-loop frequency response, 351–55
- closed-loop gain, 248–49, 252; in operational amplifiers, 293;
 - and voltage-voltage feedback, 272–73
- closed-loop transfer function, 247
- CMFB. *See* common-mode feedback
- CMOS (complementary MOS) devices, 6–7; processing
 - technology, 604–30
- CMOS inverters, 581; driving load capacitance, 668; ring
 - oscillators using, 490
- CMOS oscillators. *See* oscillators
- CMOS technology: compatibility with bandgap references,
 - 386; diodes realized in, 523
- collector current variation, 385–86
- Colpitts oscillators, 502–5
- common-centroid layout, 640–41
- common-drain stage, 67. *See also* source follower
- common-gate circuit, with feedback, 250
- common-gate (CG) stage, 76–83; frequency compensation
 - using, 370–71; and frequency response, 183; at high
 - frequencies, 183; input impedance, 80–83;
 - input-output characteristic, 77; input-referred noise,
 - 229–31; output impedance, 80–83; with parasitic
 - capacitance, 171; single-stage amplifiers, 228–31;
 - transfer function, 171
- common mode (CM), input-output characteristic, 105
- common-mode behavior, differential pair, 105–6
- common-mode input, 116–18
- common-mode feedback (CMFB): modifying, 323–24;
 - operational amplifiers, 314; switched-capacitor,
 - 442–43; topology, 317
- common-mode level, sensing and controlling, 319–22
- common-mode noise rejection, 101
- common-mode properties, active current mirrors, 154–58
- common-mode range, extending, 325–26
- common-mode rejection: alternative definition, 478–79; in
 - voltage-controlled oscillators (VCOs), 512
- common-mode response, differential amplifiers, 118–24
- common-mode signals, response of differential
 - pairs to, 187–93
- common-source (CS) stage, 48–67; with current-source load,
 - 58–59; with diode-connected load, 53–58; distortion
 - in, 449; with feedback, 248, 251–52; frequency
- response, 172–78; gain stage added to, 219;
 - high-frequency model, 172; input impedance in, 177;
 - and input-referred noise, 219–221; with resistive
 - degeneration, 458–59; single-stage amplifiers,
 - 225–28; with source degeneration, 60–67; and source
 - impedance stimulation, 223–24; transfer function,
 - 172–77; with triode load, 59–60; using *n*-well
 - resistors, 618; zero calculated in, 176–77
- compensation, frequency, 355–61
- complementary switches, 422
- conduction, subthreshold, 27–28
- constant-field scaling, 579
- constant- G_m biasing, 392–93
- contact spiking, 615–16
- contact windows, 615
- continuous-time: feedback amplifiers, 405–7; integrator, 439;
 - resistors, 439
- control voltage, 126–29
- conversion, differential, 120–24
- corner frequency, flicker noise, 217–18
- correlated sources of noise, 207–9
- coupling: capacitive, 654; one-dimensional cross-, 641–42;
 - substrate, 660–65
- cross-coupled oscillators, 499–501, 522
- CS stage. *See* common-source stage
- current: amplifiers, 254–56; copying, 137; drain, 148–49;
 - generating PTAT (proportional to absolute
 - temperature), 390–92; generation versus voltage
 - amplification, 225; meters, 256–58; mismatch,
 - 469–70, 565–67; notation, 8; resistive biasing,
 - 135–36; scaling, 643–44; steering, 515–20;
 - tail, 120–21. *See also* biasing
- current-current feedback, 269–70; loading in, 281
- current mirrors: active, 135–65, 145–58; basic, 135–39;
 - cascode, 139–45; passive, 135–65
- current-source load: common-source stage with, 58–59;
 - differential pair with, 146
- current sources: applications, 135–36; cascode, 140–45;
 - NMOS device used by source follower as, 69; noise
 - represented in, 221–22
- current-voltage feedback, 263–66; loading in, 275–78
- curvature correction, 390
- CVD. *See* chemical vapor deposition
- Czocharlski method, 606
- DAC (digital-to-analog converter), 3
- dangling bonds, 215
- data: binary, 2–3; four-level, 2–3; stored on hard disks,
 - 3; transmission of over long distances, 4
- dead zone in phase-locked loops (PLLs), 563–64
- deep triode region, MOSFETs operating in, 460–61.
 - See also* triode region
- degeneration, resistive, 458–63
- delay-locked loops (DLLs), 570–72
- delay variation: by interpolation, 518–20; by positive
 - feedback, 515–18
- deposition, 611
- design rules, 632–34
- designing operational amplifiers, 299–300
- device models, choice of, 92–93
- devices. *See* active devices; MOS devices; NMOS devices;
 - passive devices; PMOS devices
- DIBL. *See* drain-induced barrier lowering
- differential amplifiers, 100–34; biased by current mirrors,
 - 138–39; common-mode response, 118–24;
 - Gilbert cell, 126–29

- differential circuits, 103; nonlinearity of, 452–54
differential conversion, 120–24
differential input, 116–18
differential pairs: with active current mirror, 148, 150, 151, 154, 190; basic, 103–18; cascode, 126; common-mode behavior, 105–6; with common-mode feedback, 314–15; with current-source load, 146; degeneration, 460–62; distortion in, 449; frequency response, 187–93; half circuit, 126; input voltage, 107–10; input-output characteristic, 104; layout, 638–40; lemma, 114; with MOS loads, 124–26; noise in, 233–39; with offset, 465–70; output voltage, 106–7; PMOS, 479; qualitative analysis, 104–7; quantitative analysis, 107–18; small-signal behavior, 110–14; used in tuning ring oscillators, 512–20
differential realization, in noninverting amplifier, 435
differential sampling circuits, 422–23
differential signals: response of differential pairs to, 187–93; versus single-ended, 100–2
digital communications, 2–3
digital signal processor (DSP), 1–2
digital-to-analog converter (DAC), 3
diode-connected device, 137
diode-connected load, CS stage with, 53–58
diodes: layout in passive devices, 652–53; realized in CMOS technology, 523; varactor, 521–25
DIP. *See* dual-in-line package
discrete-time: integrators, 440; resistors, 439
disk drive electronics, 3
dispersion, 657
dissipation, power, 512
distortion: in common-source stage, 449; in differential pair, 449; even-order, 470–71
distribution: amplitude, 206–7; reference, 642–44
drain, 10, 11
drain current, 15–17, 148–49; combining, 149; of common-source device, 62; saturation of, 19
drain-induced barrier lowering (DIBL), 585, 586
drain-source voltage, output impedance variation with, 589–91
DSP (digital signal processor), 1–2
dual-in-line package (DIP), 666
dummy switches, 421–22
dummy transistors, 639–40
- electromigration, 626
electrostatic discharge (ESD), 659–60
enclosure, 633–34
ESD. *See* electrostatic discharge
etching, 611
even-order distortion, 470–71
excess phase, in phase-locked loops (PLLs), 542–43
extension, 633–34
- fabrication: active devices, 611–16; interconnects, 624–27; of CMOS devices, 611–27; passive devices, 616–24; transistor, 611–14
feedback, 246–90; circuits, 247–54; common-gate circuit with, 250; common-mode, 314–24; common-source stage with, 248, 251–52; current-current, 269–70, 281; current-voltage, 263–66, 275–78; effect of negative on nonlinearity, 454–57; effect on noise, 284–85; error, 246; general considerations, 246–58; increasing output impedance by, 310; networks, 246; oscillatory, 484; polarity, 389; positive, 515–18; series, 256; shunt, 256; switched-capacitor common-mode, 442–43; system, 246–58; topologies, 258–80; two-pole, 485–86; voltage-current, 266–69, 275–80; voltage-voltage, 258–63, 272–75. *See also* feedback circuits; negative feedback; positive feedback
feedback circuits: bandwidth modification, 252–54; gain desensitization, 247–50; nonlinearity reduction, 254; sense and return mechanisms, 256–58; terminal impedance modification, 250–52
feedback loop, 535; tuned stages, 499
feedforward: amplifiers, one-pole, 348; networks, 246
field oxide, 608
filter, low-pass, 210–211
fingers, transistor, 635–37
five-stage ring oscillators, 491
flicker noise, 215–18; corner frequency, 217–18
flipflops, 551–53
floating: impedance, 166; references, 398–99
folded cascode operational amplifiers, 301–7; noise in, 337–38; slewing in, 331–32
folded cascodes, 90–92
folding, 35; reduction of gate resistance by, 214; white noise, 206; wide transistors, 635–37
folding/folded structures, 31
four-level data, 2–3
four-stage ring oscillators, 491
frequency: center, 511; corner, 217–18; multiplication, 573–74; synthesis, 574–75. *See also* frequency compensation; frequency response; phase/frequency detectors (PFDs)
frequency compensation, 345–48, 355–61; common-gate stage used in, 370–71; Miller compensation, 362–64, 367; other techniques, 369–73; two-stage operational amplifiers, 361–69
frequency response: amplifier, 166–200; cascode stage, 185–87; closed-loop, 351–55; common-gate stage, 183–85; common-source stage, 172–78; differential pair, 187–93; general considerations, 166–71; Miller effect, 166–69, 171, 172, 174, 175, 185; and source followers, 182–85
fringe capacitance, 626
- G models, 272
gain: boosting, 309–13; closed-loop, 272–73, 293; common-mode, 154–58; crossover point, 346, 352; desensitization, 247–50; open-loop, 270, 273–75, 292; small-signal, 145–51; stage, added to common-source stage, 219; voltage, 151–54
gate: resistance, 214–15; shadowing, 639; voltage, 144
gates, 10, 11; OR, 532–33
Gilbert cell, 126–29
gradient, 640
ground bounce, 663–65
guard rings, 663
- half-circuit concept, 151–52, 187–89
half circuits, 113–18; differential pair, 126; folded cascode operational amplifiers, 303
high frequencies, common-gate stage at, 183
high-frequency model: cascode stage, 185; common-source stage, 172
hot carrier effects, 589
hybrid models, 270–72, 281

- I/V characteristics, derivation, 15–23
- impedance: floating, 166; input, 177, 179, 261–63, 265–66, 266–68; modification, 250–52; output, 173, 259–60, 264–65, 266–68, 310, 386–89, 393–97, 589–91; source, 223–24. *See also* input impedance; output impedance
- inductance: mutual, 673–75; self-, 668–73
- inductors, monolithic, 495, 521, 524
- injection, channel charge, 418–20, 421–23
- input: common-mode, 116–18; differential, 116–18
- input characteristics: of nonlinear systems, 448; of phase/frequency detectors (PFDs), 553–55; of sampling circuits, 419. *See also* input/output characteristic; output characteristics
- input differential voltage, 107–10
- input impedance: in a common-source stage, 177; and current-voltage feedback, 265–66; source follower, 73, 179; and voltage-current feedback, 266–68; and voltage-voltage feedback, 261–63
- input nodes: in cascode stage, 185–87; in common-gate stage, 183–85; in common-source stage, 172–77; and differential pairs, 187–93; and source followers, 178–82. *See also* nodes; output nodes
- input-output characteristic, 47–48, 49, 54; cascode stage, 84; common-gate stage, 77; common mode, 105; common-source stage with diode-connected load, 56; differential pair, 104; large-signal, 150; source follower, 68. *See also* input characteristics; output characteristics
- input-output transfer function, 169
- input poles: in cascode stage, 185–87; in common-gate stage, 183–85; in common-source stage, 172–77; and differential pairs, 187–93; and source followers, 178–82. *See also* poles; output poles
- input range limitations, 325–26
- input-referred noise, 219–24; of a differential pair, 233–39
- input-referred thermal noise: common-gate stage, 229–31; voltage, 225–28
- input voltage: notation, 8; versus voltage gain of source follower, 69
- integrated circuits, 6; layout and packaging, 631–75; notations, 8
- integrators: discrete-time, 440; parasitic-insensitive, 441; switched-capacitor, 439–42
- interconnects: fabrication, 624–27; layout in passive devices, 653–57; parallel capacitance, 626–27; series resistance, 624–25
- interface, dangling bonds at, 215
- interpolation, delay variation by, 518–20
- inverters. *See* CMOS inverters
- ion implantation, 608–10
- jitter: in phase-locked loops (PLLs), 563–64, 567–70; reducing in phase-locked loops (PLLs), 576–77; in voltage-controlled oscillators (VCOs), 568–70
- junction capacitances, scaling, 580–82
- kT/C noise, 421
- large-signal analysis, of active current mirrors, 149–51
- large-signal bandwidth, operational amplifiers, 295
- large-signal behavior: cascode current source, 140–45; folded-cascode stage, 91–92
- large-signal input-output characteristic, 150
- latch-up, 627–28
- layout, 631–60; analog, 635–60; antenna effect, 634–35; cascode devices, 638; common-centroid, 640–41; design rules, 632–34; differential pairs, 638–40; general considerations, 631–32; minimum enclosure, 633–34; minimum extension, 633–34; minimum spacing, 633–34; minimum width, 632–33; multifinger transistors, 635–37; PMOS device, 631–32; symmetry, 637–42
- LC oscillators, 495–509; Colpitts, 502–5; cross-coupled, 499–501; one-port, 505–9; tuning in, 521–25
- LC tanks, 496–98
- lemma: differential pair, 114; noise calculation, 224; voltage gain, 66–68
- length, 11
- level shifters, source followers as, 178–82
- linear settling, 327, 333–34
- linearity: in charge-pump phase-locked loops (CPPLLs), 557; operational amplifiers, 296; tuning, 511–12. *See also* nonlinearity
- linearization, 61; techniques, 458–63
- lithography sequence, 607
- load capacitance, 169–70
- loading, effect of, 270–84; in current-current feedback, 281; in current-voltage feedback, 275–78; summarizing effects of, 283–84; two-port network models, 270–72; in voltage-current feedback, 278–80; in voltage-voltage feedback, 272–75
- loads, MOS, differential pair with, 124–26
- lock acquisition, in charge-pump phase-locked loops (CPPLLs), 549–62
- locking, 533–42
- long-channel devices, versus short-channel devices, 38
- loop gain, 248; Bode plots, 346, 349, 357, 359, 362, 547, 561; in charge-pump phase-locked loops (CPPLLs), 559–62; computation, 249; and current-voltage feedback, 264, 275–78; in feedback loop, 500; in two- and three-pole systems, 486–87. *See also* closed-loop gain; open-loop gain
- loops, phase-locked, 532–78
- low-pass filter, 210, 211
- low-voltage cascode, 143–45
- mathematical model, voltage-controlled oscillators, 525–30
- memories, 5–6
- metal 1, 614–15
- metal-oxide-silicon field-effect transistors. *See* MOSFETs
- metal-poly capacitors, 620–21
- meters, current and voltage, 256–58
- microprocessors, 5–6
- Miller compensation, 362–64, 367
- Miller effect, 166–69, 171, 172, 174, 175, 185
- Miller's theorem, 166–69, 193–95
- mismatch, 120–24, 463–79; and common-mode gain, 157; current, 469–70, 565–67; DC offsets, 465–79; MOSFET, 463–79; threshold voltage, 471
- mobility degradation with vertical field, 585–87
- models: cascode stage, 186; choice of, 92–93; G, 272–73; high-frequency, 172; high-frequency, of cascode stage, 185; hybrid, 270–72, 281; mathematical, of voltage-controlled oscillators, 525–30; MOS device, 28–38, 591–99; MOS device BSIM series, 596–97; MOS device Level 1, 592; MOS device Level 2, 593–95; MOS device Level 3, 595–96; MOS small-signal, 33–36; MOS SPICE, 36–37; small-signal, 61, 65–66; small-signal of CS stage, 52; two-port network, 270, Y, 270–72, 278; Z, 270–72, 276
- monolithic: capacitors, 423–24; inductors, 495, 521, 524

- MOS: circuit symbols, 12–13; I/V characteristics, 13–23
- MOS capacitors, 621–24; channel resistance of, 622–24
- MOS device models, 591–99; BSIM series, 591–92, 596–97; charge and capacitance modeling, 598; Level 1, 592; Level 2, 593–95; Level 3, 595–96; temperature dependence, 599
- MOS devices: active, 611–16; behavior as a capacitor, 38–39; capacitances, 29–33; fabricating, 611–27; layout, 28–29; models, 28–38, 591–99; passive, 616–24; processing technology, 604–30; small-signal model, 33–36; subthreshold characteristics, 27–28; as switches, 413–23; transconductance, 22, 28. *See also* NMOS devices; PMOS devices
- MOS loads, differential pair with, 124–26
- MOS SPICE models, 36–37
- MOS technology. *See* MOSFETs
- MOSFETs (metal-oxide-silicon field-effect transistors), 6; common-mode sensing using, 319; as controlled linear resistor, 18–19; layout, 28–29; mismatches in, 463–79; ohmic sections, 213–14; operating in deep triode region, 460–61; parameter variations, 599–600; physics, 9–38; reducing effect of mismatched, 397–400; relationship between drain current and terminal voltage, 15–17; saturated, 19–21; scaling, 579–83; small-signal model, 33–36; structure, 10–12; as switches, 10, 410–14; thermal noise, 212–15; transconductance, 392
- multifinger transistors, 635–37
- multiply-by-two circuits, 438–39; with MOS capacitor, 622
- multipole systems, 349–51
- mutual capacitance, 675
- mutual inductance, 673–75
- n*-type MOS devices. *See* NMOS devices
- natural signals, processing of, 1–2
- negative feedback: effect of on nonlinearity, 454–57; system, 345–46. *See also* feedback; feedback circuits; positive feedback
- negative resistance, 505–9
- negative-TC (temperature coefficient) voltage, 381–82
- NFETs: bulk, 36; threshold voltage, 14. *See also* NMOS devices
- NMOS (*n*-type MOS) devices, 6; bulk voltage, 23–25; in cross-coupled oscillators, 524–25; in gain-boosting amplifiers, 311; latch-up in, 627–28; in operational amplifiers, 301–5; parameters of Level 1 SPICE models, 37; versus PMOS devices, 37; process corners based on speed of, 600; processing technology, 604–30; structure, 10–12; as switches, 410–14, 416; used by source follower as current source, 69
- nodes: association with poles, 169–71; in cascode stage, 185–87; in common-gate stage, 183–85; and differential pairs, 187–93; input, 172–77; interaction between, 170; output, 172–77; and source followers, 178–82. *See also* input nodes; output nodes
- noise, 201–45; amplitude distribution, 206–7; average power, 202–3; bandwidth, 239; calculation lemma, 224; cascode stage, 232–33; common-gate stage, 228–31; common-mode, 101; common-source stage, 225–28; corner frequency, 217–18; correlated and uncorrelated sources, 207–9; in differential pairs, 233–39; effect of feedback on, 184–85; flicker, 215–18; input-referred, 219–24; kT/C , 421; in operational amplifiers, 296, 336–40; output-referred, 219; predicting properties of, 201–2; reduced by offset cancellation, 476–78; reference generator, 393–97; representation in circuits, 218–24; in self-inductance, 668–69; in source followers, 231–32; sources, 218–19; spectrum, 203–6; statistical characteristics, 201–9; thermal, 209–15; types of, 209–18; white, 204–5
- noisy lines, 101
- noninverting amplifiers, 432–38; precision considerations, 435–36; speed considerations, 436–38
- nonlinear systems, input-output characteristic, 47–48
- nonlinearity, 448–63; capacitor, 457–58; definition of, 450; of differential circuits, 452–54; effect of negative feedback on, 454–57; general considerations, 448–52; reduction, 254. *See also* linearity
- Norton equivalent, 66–67
- notations, 8
- offset: DC, 465–70; operational amplifier, 296, 386–89
- offset cancellation, 471–76; noise reduced by, 476–78
- ohmic sections, MOSFET, 213–14
- one-dimensional cross-coupling, 641–42
- one-pole feedforward amplifiers, 348
- one-pole systems, 252–54
- one-port oscillators, 505–9
- one-stage operational amplifiers, 296–307
- op amps. *See* operational amplifiers
- open-loop circuits, 250, 253–54
- open-loop gain, 248–49, 270; in operational amplifiers, 292; and voltage-voltage feedback, 273–75
- open-loop transfer function, 247
- operational amplifiers, 291–344; cascode, 292, 298–99; closed-loop gain, 293; common-mode feedback, 314; designing, 299–300; folded cascode, 301–7, 331–32, 337–38; gain, 291–92; gain boosting, 309–13; input range limitations, 325–26; large-signal bandwidth, 295; linearity, 296; noise and offset, 296; noise in, 336–40; offset and output impedance, 386–89; one-stage, 296–307; open-loop gain, 292; output swing, 295, 298; performance parameters, 291–96; power supply rejection, 334–36; slew rate, 326–34; small-signal bandwidth, 293; supply rejection, 296; telescopic, 331, 336–37, 356–61; telescopic cascode, 297–99, 303–4, 306; topology comparison, 313–14; triple cascode, 307; two-stage, 307–9, 338–40, 361–69, 368–69
- optical receivers, 4
- OR gates, 532–33
- oscillators, 482–531; Colpitts, 502–5; cross-coupled 499–501, 522; general considerations, 482–84; LC, 495–509, 521–25; one-port, 505–9; ring, 484–95; voltage controlled (VCOs), 482–531, 510–30
- output amplitude, in voltage-controlled oscillators (VCOs), 512
- output characteristics: nonlinear systems, 448; of phase/frequency detectors (PFDs), 553–55; sampling circuit, 419. *See also* input characteristics; input/output characteristic
- output impedance, 173; boosting, 310–11; cascode stage, 85–86, 88; and current-voltage feedback, 264–65; operational amplifier, 386–89; reference generator, 393–97; source follower, 70, 73, 180–82; variation with drain-source voltage, 589–91; and voltage-current feedback, 266–68; and voltage-voltage feedback, 259–60
- output nodes: in cascode stage, 185–87; in common-gate

- stage, 183–85; in common-source stage, 172–77; and differential pairs, 187–93; and source followers, 178–82
- output phase, in phased-locked loops (PLLs), 533–36
- output poles: in cascode stage, 185–87; in common-gate stage, 183–85; in common-source stage, 172–77; and differential pairs, 187–93; and source followers, 178–82. *See also* input poles; poles
- output port, 66–67
- output-referred noise, 219
- output signal purity, in voltage-controlled oscillators (VCOs), 512
- output spectrum theorem, 205–6
- output swing, 106–7, 295, 298
- output voltage, 66–67, 149–50; notation, 8; swing, 106–7, 295, 298
- oxidation, 608
- oxide spacers, 614

- p*-type MOS devices. *See* PMOS devices
- packaging, 666–75; dual-in-line package, 666; mutual inductance, 673–75; parasitics, 667–68; self- and mutual capacitance, 675; self-inductance, 668–73
- pads, bonding, 657–59
- parallel capacitance, of interconnects, 626–27
- parameter variations, in MOSFETs, 599–600
- parasitic: capacitance, 171; -insensitive integrators, 441; packaging, 667–68
- passive current mirrors, 135–65
- passive devices: analog layout techniques, 644–53; capacitor layout, 650–52; diode layout, 652–53; fabrication, 616–24; interconnect layout, 653–57; MOS, 616–24; pads and electrostatic discharge (ESD) protection, 657–660; resistor layout, 645–50
- passive MOS devices, 616–24; capacitors in, 619–24; resistors, 616–18
- PDs. *See* phase detectors
- PFDs. *See* phase/frequency detectors
- PFETs, bulk, 36. *See also* PMOS devices
- phase crossover point, 346, 352
- phase detectors (PDs), 532–33
- phase/frequency detectors (PFDs): in charge-pump phase-locked loops (CPPLLs), 550–55; PFD/CP nonidealities, 562–67
- phase-locked loops (PLLs), 532–78; applications, 572–77; dynamics, 542–49; excess phase, 542–43; frequency multiplication, 573–74; frequency synthesis, 574–75; jitter, 563–64, 567–70; jitter reduction, 576–77; nonideal effects, 562–70; phase detectors (PD), 532–33; response to small transients in locked condition, 539–42; settling speed, 545–46; simple, 532–49; skew reduction, 575–76; transfer function, 542–49; waveforms in locked condition, 536–39
- phase margin, 351–55
- photolithography, 606–8
- photoresists, 607
- pinch-off behavior, 20, 25; effect of scaling on, 582
- plates: bottom, 423–24; top, 423
- PLLs. *See* phase-locked loops
- PMOS (*p*-type MOS) devices, 6; in cross-coupled oscillators, 524–25; differential pairs, 479; diode-connected, 56; in gain-boosting amplifiers, 311–12; latch-up in, 627–28; layout, 631–32; versus NMOS devices, 37; in operational amplifiers, 301–6; parameters of Level 1 SPICE models, 37; process corners based on speed of, 600; processing technology, 604–30; in ring oscillators, 494–95; source follower, 74; structure, 10–12; as switches, 414, 415, 416, 419; threshold phenomenon, 15
- poles: association with nodes, 169–71; in cascode stage, 185–87; in common-gate stage, 183–85; and differential pairs, 187–93; dominant, 358–61; input, 172–77; multipole systems, 349–51; nondominant, 361; output, 172–77; plotting location of, 347–48; and source followers, 178–82; two-pole feedback systems, 485–86. *See also* input poles; output poles
- poly-diffusion capacitors, 619–20
- poly-poly capacitors, 620
- positive feedback, tuning, 515–18. *See also* feedback; feedback circuits; negative feedback
- positive-TC (temperature coefficient) voltage, 382–84
- power dissipation, in voltage-controlled oscillators (VCOs), 512
- power spectral density (PSD), 204–5
- power supply rejection, operational amplifiers, 334–36
- precision: in noninverting amplifiers, 435–36; in sampling circuits, 417–21; in unity-gain sampler/buffers, 428–29
- precision multiply-by-two circuits, 438–39, 622
- process corners, 599–600
- processing: back-end, 614–16; CMOS devices, 604–30; deposition and etching, 611; ion implantation, 608–10; latch-up, 627–28; oxidation, 608; photolithography, 606–8; wafers, 605–6
- PTAT (proportional to absolute temperature) current generation, 390–92

- qualitative analysis, differential pairs, 104–7
- quantitative analysis, differential pairs, 107–18

- receivers: optical, 4; wireless, 3–4
- reduction, nonlinearity, 254
- reference distribution, 642–44. *See also* bandgap references
- reference generator, output impedance, 393–97
- rejection: common-mode, 512; common-mode noise, 101; power supply, 334–36; supply, 296
- resistance, 35; calculating, 63–66; gate, 214–15; negative, 505–9; output, 70; series, 624; sheet, 605
- resistive biasing, 135–36
- resistive degeneration, 458–63
- resistive load, common-source stage with, 48–67
- resistors: continuous-time, 439; discrete-time, 439; layout in passive devices, 645–50; mismatched, 120–24; in passive MOS devices, 616–18; thermal noise, 209–12
- ring oscillators, 484–95; amplitude limiting, 487–95; four- and five-stage, 491; three-stage, 486–89; tuning in, 512–21
- ringing, 182
- ripple, 536; in charge-pump phase-locked loops (CPPLLs), 562
- RLC circuits, 496–99

- samplers: and offset cancellation, 476–78; unity-gain, 424–32
- sampling, bottom-plate, 423
- sampling circuits: differential, 422–23; precision considerations, 417–21; speed considerations, 414–17
- sampling mode: noninverting amplifiers, 432–433; switched-capacitor circuits, 408–9, 410–23; unity-gain sampler, 424–25, 429
- sampling switches, 410–23

- saturation, 49; region, 19–21, 22–23, 49; velocity, 587–89
 scaling: constant-field, 579; current, 643–44; theory, 579–83
 second-order effects, 23–28
 self-capacitance, 675
 self-inductance, 668–73
 sense and return mechanisms, 256–58
 sensors, 4–5
 series feedback, 256
 series resistance, of interconnects, 624–25
 settling speed, in phase-locked loops (PLLs), 545–46
 shadowing, 639
 sheet resistance, 605
 shielding, 655–56; cascode stage, 89–90
 short-channel devices, versus long-channel devices, 38
 short-channel effects, 583–91; drain-induced barrier lowering (DIBL), 585, 586; hot carrier effects, 589; mobility degradation with vertical field, 585–87; output impedance variation with drain-source voltage, 589; threshold voltage variation, 583–85; velocity saturation, 587–89
 shunt feedback, 256
 signals: differential, 100–2; output, 512; single-ended, 100–2
 silicide, 614, 616–17
 single-ended signals, versus differential signals, 100–2
 single-pole system, 252–54
 single-stage amplifiers, 47–99, 224–33; basic concepts, 47–48; cascode stage, 83–92, 232–33; choice of device models, 92–93; common-gate stage, 76–83, 228–31; common-source stage, 48–67, 225–28; source followers, 67–76, 231–32
 sinusoid waveform, 525–26
 skew, 565–66; eliminating in voltage-controlled oscillators, 533–36; reducing in phase-locked loops (PLLs), 575–76
 slew rate, operational amplifiers, 326–34
 slewing: negative, 372; positive, 372; in two-stage operation amplifiers, 368–69; in unity-gain sampler/buffer, 431–32
 small-signal analysis, of active current mirrors, 151–54
 small-signal bandwidth, operational amplifiers, 293–95
 small-signal behavior: in active current mirrors, 145–48; differential pair, 110–14
 small-signal characteristics, cascode stage, 84–85
 small-signal gain, 145–51; calculating, 68–69; in nonlinear amplifiers, 450, 452–54
 small-signal models, 61; of common-source stage, 52
 small-signal output resistance, calculating, 70–72
 source, 10, 11
 source degeneration, common stage with, 60–67
 source/drain junction capacitance, scaling, 580–82
 source followers, 67–76; common-mode feedback using, 318; drawbacks of, 73–76; input impedance, 73, 179; input-output characteristic, 68; intrinsic, 72; as level shifters, 145, 178–82; output impedance, 70, 73, 180–82; single-stage amplifiers, 231–32; small-signal equivalent circuit, 68–69
 source impedance, 223–24
 spacers, oxide, 614
 spacing, layout, 633–34
 spectral shaping, 205–6
 speed: in noninverting amplifiers, 436–38; reference generator, 393–97; in sampling circuits, 414–17; settling, 545–46; in unity-gain sampler/buffers, 429–32
 SPICE models, 36–37
 spiking, contact, 615–16
 square wave amplification, 253
 stability, 345–76; in charge-pump phase-locked loops (CPPLLs), 561–62; general considerations, 345–48
 stages: delay, 518–20; in ring oscillators, 486–92; tuned, 498–99, 502
 start-up, 389–90
 statistical characteristics of noise, 201–9
 step response, 326–27
 structure, MOSFET, 10–12
 substrate, 10–12; bounce, 663–65; coupling, 660–65
 subthreshold conduction, 27–28
 supply: dependence, 389–90; rejection, 296; in voltage-controlled oscillators (VCOs), 512
 supply-independent biasing, 377–81
 switched-capacitor amplifiers, 423–39
 switched-capacitor circuits, 405–47; in amplification mode, 408–9; general considerations, 405–9; in sampling mode, 408–9, 410–23
 switched-capacitor common-mode feedback, 442–43
 switched-capacitor integrator, 439–42
 switches: complementary, 422; dummy, 421–22; MOSFETs as, 10, 410–14; sampling, 410–23; zero-offset, 414
 symbols, MOS, 12–13
 symmetry, 113–14, 117–20, 149–50; in layouts, 637–42.
See also asymmetry
 tail current, 120–21
 tanks, LC, 496–98
 telephone bandwidth, and spectral shaping, 205–6
 telescopic cascode operational amplifiers, 297–99, 303–4, 306. *See also* telescopic operational amplifiers
 telescopic operational amplifiers: frequency compensation, 356–61; noise in, 336–37; slewing in, 331. *See also* telescopic cascode operational amplifiers
 temperature, proportional to absolute (PTAT), 377, 390–92
 temperature dependence: forms, 377; in MOS device models, 599
 temperature-independent references, 381; bandgap references, 384–90; negative-TC (temperature coefficient) voltage, 381–82; positive-TC (temperature coefficient) voltage, 382–84
 temperature-independent voltage, 384–85
 terminal impedance modification, 250–52
 terminals, 10–11
 thermal noise, 209–15; MOSFETs, 212–15; resistors, 209–12; voltage, 225–28
 Thevenin equivalent, 72, 79, 112, 153, 191, 437
 three-pole systems, 350–51
 three-stage ring oscillators, 486–89
 threshold voltage, 10, 13–15, 27–28, 149–50; mismatches, 471; variation, 583–85
 time-domain response, 347–48
 topologies: comparison of operational amplifier, 313–14; common-mode feedback, 317; current-folding, 518; feedback, 258–70; folded cascode operational amplifiers, 302; operational amplifiers, 296–98; phase-locked loops (PLLs), 533–42
 transconductance, 22, 28, 48; amplifiers, 254–56; MOSFET, 392; of common-source devices, 62, 66
 transfer function: in charge-pump phase-locked loops (CPPLLs), 557–61; closed-loop, 247; common-gate stage, 171; common-source stage, 172–77; input-output, 169; open-loop, 247; in phase-locked loops (PLLs), 542–49; and spectral shaping, 205–6
 transients in locked condition, response of phase-locked loops (PLLs) to, 539–42
 transimpedance amplifiers, 254–56

- transistors: dummy, 639–40; fabrication of, 611–14; multifinger, 635–37. *See also* CMOS devices; MOSFETs
- triode load, CS stage with, 59–60
- triode region, 17–18, 22–23, 49, 149; common-mode sensing using MOSFETs in, 319; deep, 460–61
- triple cascode operational amplifiers, 307
- tuned stages, 498–99, 502
- tuning: delay variation by interpolation, 518–20; delay variation by positive feedback, 515–18; in LC oscillators, 521–25; linearity, in voltage-controlled oscillators, 511–12; range, in voltage-controlled oscillators, 511; in ring oscillators, 512–21; wide-range, 520–21
- turn-on phenomenon, 14–15
- two-pole systems, 349–50
- two-port network models, 270–72
- two-stage operational amplifiers, 307–9; frequency compensation, 361–69; noise in, 338–40; slewing in, 368–69
- uncorrelated sources of noise, 207–9
- unity-gain buffer, 325, 355. *See also* unity-gain sampler/buffer
- unity-gain sampler/buffer, 424–32; precision considerations, 428–29; slewing behavior, 431–32; speed considerations, 429–32. *See also* unity-gain buffer
- varactors, 521–25
- variable-gain amplifiers (VGAs), 126–28
- velocity saturation, 587–89
- vertical field, mobility degradation with, 585–87
- VGAs. *See* variable-gain amplifiers
- vias, 615
- voltage: amplification, versus current generation, 225; amplifiers, 461; bulk, 23–25; control, 126–29; drain-source, 589–91; floating reference, 398–99; gate, 144; input, 69, 107–10; input-referred thermal noise, 225–28; limitations, 28; meters, 256–58; negative-TC (temperature coefficient), 381–82; notation, 8; output, 66–67, 106–7, 149–50; positive-TC (temperature coefficient), 382–84; sources, noise represented in, 221–22; temperature-independent, 384–85; threshold, 13–15, 27–28, 149–50, 583–85
- voltage-controlled oscillators (VCOs), 510–30; center frequency, 511; common-mode rejection, 512; definition, 510; eliminating skew in, 533–36; jitter in, 568–70; mathematical models, 525–30; output amplitude, 512; output signal purity, 512; power dissipation, 512; supply, 512; tuning linearity, 511–12; tuning range, 511. *See also* oscillators
- voltage-current feedback, 266–69; and input impedance, 266–68; loading in, 275–80; and output impedance, 266–68
- voltage-dependent capacitors, 521–22
- voltage gain, 86–87, 151–54; lemma, 66–68; small-signal, 452–54
- voltage-voltage feedback, 258–63; and closed loop gain, 272–73; loading in, 272–75; and open loop gain, 273–75
- wafers: in device fabrication, 611–16; introducing dopants into, 608–10; processing, 605–6
- waveforms, 525–30; jitter, 568; in locked condition, 536–39; ring oscillators, 487, 490; sinusoid, 525–26; with a skew, 534
- white noise, 204–5; folded, 206
- wide-range tuning, 520–21
- width, layout, 632–33
- wireless receivers, 3–4
- Y models, 270–72, 278
- Z models, 270–72, 276
- zero: calculation in common-source stage, 176–77; in right half plane, 364–65, 369
- zero-offset switches, 414