APPENDIX
A Synopsis of IEEE Std 91–1984 Logic Symbols

APPENDIX
A SYNOPSIS OF IEEE Std 91-1984 LOGIC SYMBOLS

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A1

The IEEE (Institute of Electrical and Electronic Engineers) has adopted a symbolic language that shows the relationship of each input of a digital logic circuit to each output without showing explicity the internal logic. The standard is quite powerful and involved. The material presented here is necessarily brief and is intended to assist technical workers in understanding information to be found in data manuals, block diagrams, and schematic diagrams.

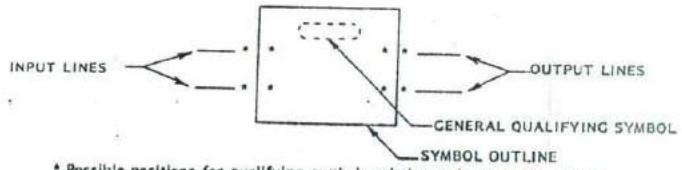
The standard substitutes rectangular shapes for the distinctive shapes representing logic functions such as AND, OR, and negation. The shape is no longer significant, except in the case of a common control block or common output block as shown in Fig. A-1. This illustration also shows the locations for the general qualifying symbol and qualifying symbols relating to inputs and outputs. Fig. A-2 shows the general qualifying symbols, Fig. A-3 the qualifying symbols for inputs and outputs, and Fig. A-4 shows the symbols used inside the outline. Generally, input lines are on the left and output lines are on the right. When exceptions to this are made, the direction of flow is indicated with arrows.

Fig. A-5 compares logic symbols. This activity represents one of the best ways to learn the IEEE standard. Locate symbols for devices that are already understood and verify each symbolic notation and representation.

Dependency notation is the most powerful aspect of the IEEE standard and is consequently the most difficult part to learn. Table A-1 is a summary of the eleven types of dependency identified by the standard and Table A-2 is a summary of the rules for each. The information provided by dependency notation supplements that provided by the qualifying symbols for an element's function. Dependency notation makes extensive use of the words "affecting" and "affected". It may not always be evident as to which should be which and the choice may be made in any convenient way.

Dependency notation is accomplished by labeling the input (or output) affecting other inputs or outputs with the appropriate letter symbol (such as C for AND) followed by an identifying number. Then, each other input or output affected by the affecting input must be labeled with that same number. If it is the complement of the internal logic state of the affecting input or output that does the affecting, then a bar is placed over the identifying numbers at the affected inputs or outputs. If two affecting inputs have the same letter and the same identifying number, they stand in an OR relationship to each other. If the affected input or output requires a label to denote its function (such as "D"), then this label will be prefixed by the identifying number of the affecting input. If an input or output is affected by more than one affecting input, the identifying numbers of each of the affecting inputs will appear in the label of the affected one, separated by commas. The normal reading order of these numbers is the same as the sequence of the affecting relationships. When the labels denoting the functions of affected inputs or outputs must be numbers (such as the outputs of a coder), the identifying numbers are replaced by other characters, such as Greek letters, to avoid ambiguity.

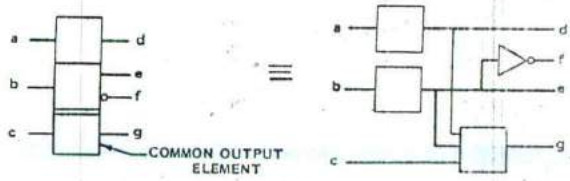
A2



* Possible positions for qualifying symbols relating to inputs and outputs

(A) SYMBOL COMPOSITION

(B) COMMON CONTROL BLOCK



(C) COMMON OUTPUT ELEMENT

GENERAL COMPOSITION OF IEEE STD 91-1984 LOGIC SYMBOLS

A3

SYMBOL	DESCRIPTION
&	AND gate or function.
≥ 1	OR gate or function.
= 1	Exclusive OR.
=	Logic identity. All inputs must stand at the same state.
2k	An even number of inputs must be active.
2k + 1	An odd number of inputs must be active.
1	The one input must be active.
▷ or ◁	More than usual output capacity. Symbol shows direction of flow.
Π	Schmitt trigger. Element with hysteresis.
X/Y	Coder, code converter (DEC/BCD, BIN/7-SEG, etc.).
MUX	Multiplexer or data selector.
DMUX or DX	Demultiplexer.
Σ	Adder.
P-Q	Subtracter.
CPG	Look-ahead carry generator.
π	Multiplier.
COMP	Magnitude comparator.
ALU	Arithmetic logic unit.
⌐	Retriggerable monostable.
1 ⌐	Nonretriggerable monostable (one-shot).
G ⌐	Astable element (waveform is optional).
!G ⌐	Synchronously starting astable.
G! ⌐	Astable element that stops with a completed pulse.
SRGm	Shift register. m = number of bits.
CTRm	Counter. m = number of bits. Cycle length = 2^m.
CTR DIVm	Counter with cycle length = m.
RCTRm	Asynchronous (ripple carry) counter. Cycle length = 2^m.
ROM	Read-only memory.
RAM	Random-access read/write memory.
FIFO	First-in, first-out memory.
I = 0	Element powers up cleared to 0 state.
I = 1	Element powers up set to 1 state.
◊	Highly complex function.

GENERAL QUALIFYING SYMBOLS

A4

SYMBOL	DESCRIPTION
	Logic negation at input. External 0 produces internal 1.
	Logic negation at output. Internal 1 produces external 0.
	Active-low input. Equivalent to —○
	Active-low output. Equivalent to ○—
	Active-low input in the case of right-to-left signal flow.
	Active-low output in the case of right-to-left signal flow.
	Signal flow from right to left; otherwise flow is from left to right.
	Bidirectional signal flow.
	Dynamic input. Active on negative edge.
	Dynamic input. Active on negative edge.
	Dynamic input. Active on positive edge.
	Nonlogic connection. A label inside the symbol may define it.
	Input for analog signal on a digital device.
	Input for a digital signal on an analog device.
	Internal connection. 1 state on left produces 1 state on right.
	Negated internal connection. 1 state on left produces 0 state on right.
	Dynamic internal connection. 0 to 1 transition gives momentary 1.
	Internal input (virtual input). Not connected to a terminal.
	Internal output (virtual output). Not connected to a terminal.

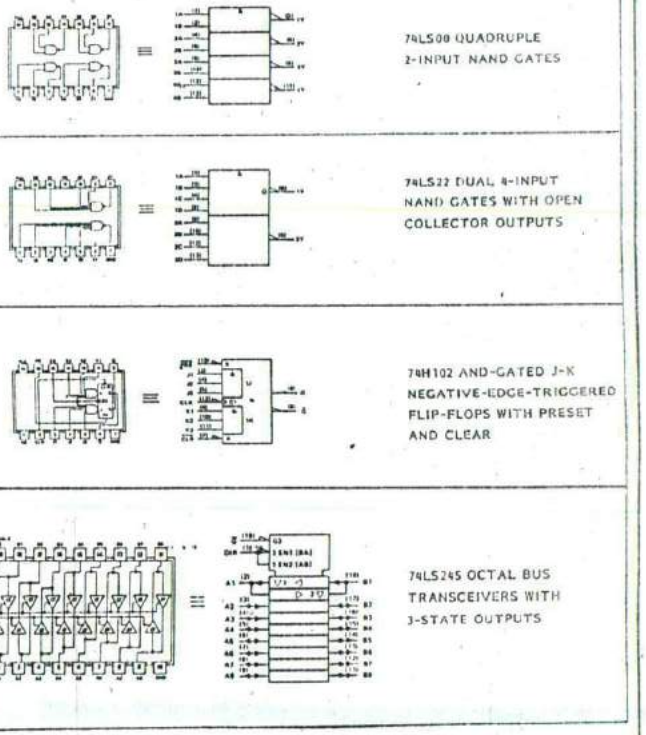
QUALIFYING SYMBOLS FOR INPUTS AND OUTPUTS

A5

SYMBOL	DESCRIPTION
	Postponed output. It changes when input returns to its initial level.
	Bi-threshold input (hysteresis).
	NPN open-collector (or open drain) output. Requires external pull-up. Capable of wired-AND connection.
	Open-collector (or drain) with built-in passive pull-up.
	NPN open emitter (or open source) output. Requires external pull-down. Capable of wired-OR connection.
	Open-emitter (or drain) with built-in passive pull-down.
	3-state output.
	Output with more than usual capability. Symbol shows signal direction.
EN	Enable input. When at its internal 1-state, all outputs are enabled. When 0, open-collector and open-emitter outputs are off, 3-state outputs are at normally defined internal logic states and at external high-Z state, and all other outputs (such as totem poles) are at the internal 0-state.
J,K,R,S,T	Usual meanings associated with flip-flops (reset, set, toggle, etc.).
D	Data input to a storage element. Equivalent to S, R
-m / +m -m	Shift right (left) inputs. m = 1,2,3, etc. If m = 1, it is not shown.
+m -m	Counting up (down) inputs. m = 1,2,3, etc. m not shown if 1.
0 / m	Binary grouping. m is highest power of 2.
CT = 15	The contents-setting input, when active, causes the content of a register to take on the indicated value
CT = 9	The content output is active if the content of the register is as indicated.
	Input line grouping. Indicates two or more terminals used to implement a single logic input. Equivalent to X, X, E
"1"	Fixed-state output always stands at its internal 1 state. An example is the 74185 binary to BCD code converter. This IC is based on a ROM where two of the outputs are not used and are programmed high to conserve power.
[X]	"X" represents non-standard information. In addition, others are used which relate to arithmetic functions and are usually self-explanatory.

SYMBOLS INSIDE THE OUTLINE

A6



A COMPARISON OF LOGIC SYMBOLS

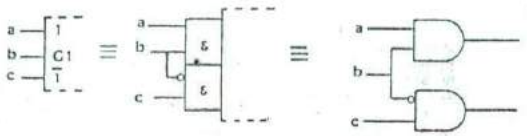
TYPE OF DEPENDENCY	LETTER SYMBOL*	AFFECTING INPUT AT ITS 1-STATE	AFFECTING INPUT AT ITS 0-STATE
Address	A	Permits action (address selected)	Prevents action (address not selected)
Control	C	Permits action	Prevents action
Enable	EN	Permits action	Prevents action of inputs Outputs off Outputs at external high Z, no change in internal logic state Other outputs at internal 0 state
AND	G	Permits action	Imposes 0 state
Mode	M	Permits action (mode selected)	Prevents action (mode not selected)
Negate (XOR)	N	Complements state	No effect
Reset	R	Affected output reacts as it would to S = 0, R = 1	No effect
Set	S	Affected output reacts as it would to S = 1, R = 0	No effect
OR	V	Imposes 1 state	Permits action
Transmission	X	Bidirectional connection exists	Bidirectional connection does not exist
Interconnection	Z	Imposes 1 state	Imposes 0 state

* The letter symbols appear at the affecting input (or output) and are followed by a number. Each input (or output) affected by that input is labeled with that same number. When the labels EN, R, and S appear at inputs without the following numbers, the descriptions above do not apply. The action of these inputs is described in Fig. A-4.

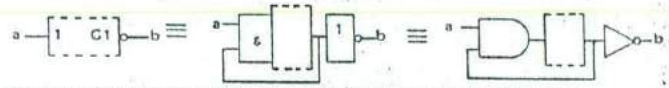
SUMMARY OF DEPENDENCY NOTATION

DEPENDENCY	RULES SUMMARY
Address	An affecting address input is labeled with the letter A followed by an identifying number (n) that corresponds with the address of the particular section of the array selected by this input. Within the general section presented by the symbol, inputs and outputs affected by an An input are labeled with the letter A, which stands for the addresses of the particular sections.
Control	When a Cn input or output stands at its internal 1 state, the inputs affected by Cn have their normally defined effect on the function of the element (these inputs are enabled). When a Cn input or output stands at its internal 0 state, the inputs affected by Cn are disabled and have no effect on the function of the element.
Enable	When an ENn input stands at its internal 0 state, the inputs affected by ENn are disabled and have no effect on the function of the element and the outputs affected by ENn are also disabled. Open collector outputs are turned off, three-state outputs stand externally at their high impedance state, and all other outputs stand at their internal 0 states.
AND	When a Gn input or output stands at its internal 1 state, all inputs and outputs affected by Gn stand at their normally defined internal logic states. When the Gn input or output stands at its 0 state, all inputs and outputs affected by Gn stand at their internal 0 states.
Mode	When an Mn input or output stands at its internal 0 state, the inputs affected have no control over the function of the element. When an affected input has several sets of labels separated by solidi (e.g., C4/2—/3+), any set in which the identifying number of the Mn input or output appears has no effect and is to be ignored.
Negate	When an Nn input or output stands at its internal 1 state, the internal logic state of each input and each output affected by Nn is the complement of what it would otherwise be. When an Nn input or output stands at its internal 0 state, all inputs and outputs affected by Nn stand at their normally defined internal logic states.
Reset	When an Rn input is at its internal 0 state, it has no effect. When it is 1, outputs affected by the Rn input will react, regardless of the state of an S input, as they normally would react to S = 0, R = 1.
Set	When an Sn input is at its internal 0 state, it has no effect. When it is 1, outputs affected by the Sn input will react, regardless of the state of an R input, as they normally would react to S = 1, R = 0.
OR	When a Vn input or output stands at its internal 1 state, all inputs and outputs affected by Vn stand at their internal 1 states. When the Vn input or output stands at its internal 0 state, all inputs and outputs affected by Vn stand at their normally defined internal states.
Transmission	When an Xn input or output stands at its internal 1 state, all I/O ports affected by this input or output are bidirectionally connected together and stand at the same internal logic state or analog level. When an Xn input or output stands at its internal 0 state, the connection does not exist.
Interconnection	The internal logic state of an input or output affected by a Zn input or output will be the same as the internal logic state of the Zn input or output, unless modified by additional dependency notation.

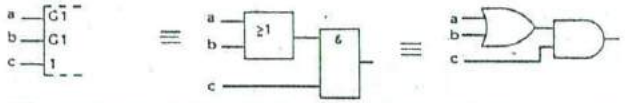
A9



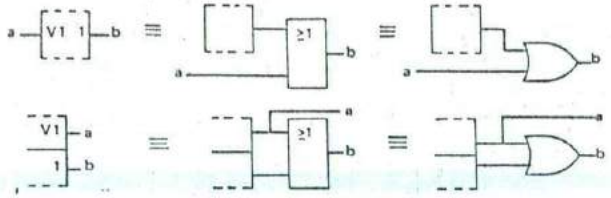
G (AND) dependency is shown in the example above. The letter "G" is used to denote the relationship and is placed at input "b", inside the symbol. Input "b" is ANDed with input "a" and the complement of "b" is ANDed with input "c". A number considered appropriate by the symbol designer (1 has been used here) is placed after the letter "G" and at each affected input. Note the bar over the "1" input at "c" which signifies that the complement of input "b" is to be ANDed with input "c".



The example above shows that output "b" affects input "a" with an AND relationship. Note that it is the internal logic state of "b", unaffected by the negation sign, that is ANDed.

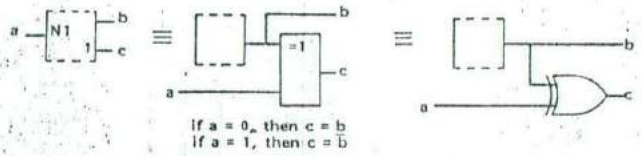


This example shows that two affecting inputs or outputs that have the same letter and the same identifying number stand in an OR relationship to each other.



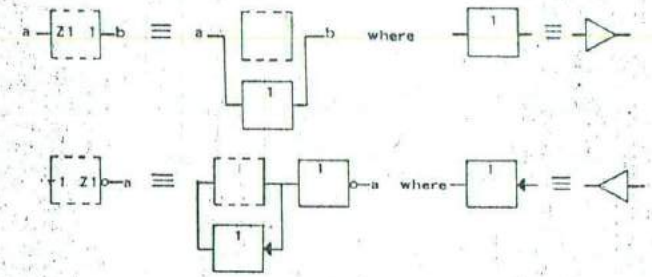
V (OR) dependency is shown in the two above examples. Input "a" is affecting output "b" with the OR relationship in the top and output "a" affects output "b" with the OR relationship in the bottom case.

A10

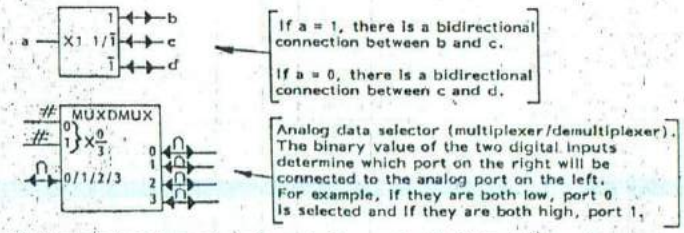


If a = 0, then c = b
If a = 1, then c = $\overline{b}$

N (negate or XOR) dependency is shown above. Input "a" affects output "c" with the exclusive OR relationship.



The two cases above are examples of Z (interconnection) dependency. This dependency is used to indicate the presence of internal logic connections between inputs, outputs, internal inputs, and/or internal outputs.

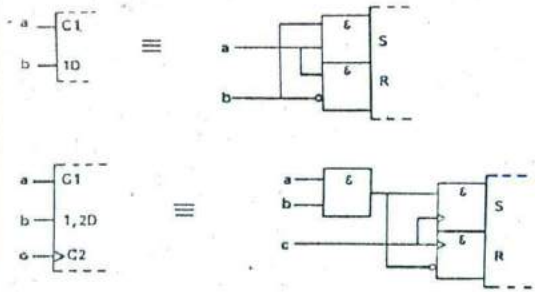


If a = 1, there is a bidirectional connection between b and c.

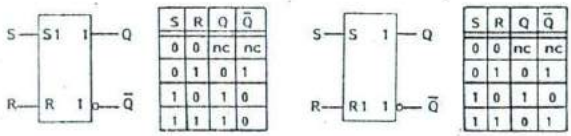
If a = 0, there is a bidirectional connection between c and d.

Analog data selector (multiplexer/demultiplexer). The binary value of the two digital inputs determine which port on the right will be connected to the analog port on the left. For example, if they are both low, port 0 is selected and if they are both high, port 1.

X (transmission) dependency is most often used with CMOS devices. It indicates controlled bidirectional connections between the affected input/output ports as shown in the two above examples.



C (control) dependency is illustrated in the two examples above. Control inputs are usually used to enable the data (D,J,K,R, or S) inputs of storage elements. They may take on their internal 1 states (be active) either statically or dynamically.



S	R	Q	$\bar{Q}$
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	1	0

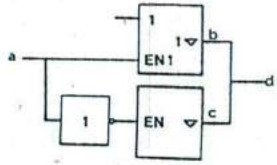
S	R	Q	$\bar{Q}$
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	0	1

S	R	Q	$\bar{Q}$
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	1	1

S	R	Q	$\bar{Q}$
0	0	nc	nc
0	1	0	1
1	0	1	0
1	1	0	0

nc = no change

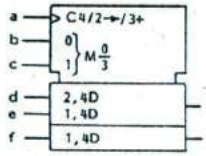
S (set) and R (reset) dependencies are shown above. These dependencies are used in those cases where it is necessary to specify the effect of the combination R = 1, S = 1 on a bistable logic element. The Sn and Rn outputs react as described earlier in the rules summary. Note that the noncomplementary output patterns in the bottom cases are only pseudo stable. The simultaneous return of the inputs to S = 0, R = 0 will produce an unforeseeable and complementary output pattern.



If a = 0, b is disabled and d = c

If a = 1, c is disabled and d = b

EN (enable) dependency is shown above. An ENn input has the same effect on outputs as an EN input, but it affects only those outputs labeled with the identifying number (n). It also affects those inputs labeled with the identifying number. In contrast, an EN input affects all outputs and no inputs.



All operations are synchronous

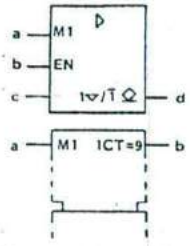
In MODE 0 (b = 0, c = 0), the outputs remain at their existing states as none of the inputs has an effect.

In MODE 1 (b = 1, c = 0), parallel loading takes place via inputs e and f.

In MODE 2 (b = 0, c = 1), shifting down and serial loading via input d takes place.

In MODE 3 (b = 1, c = 1), counting up by an increment of 1 per clock pulse takes place.

An example of M (mode) dependency affecting inputs is shown above. The b and c inputs select one of four modes. Inputs d, e, and f are D inputs subject to dynamic control (clocking) by the a input. The numbers 1 and 2 are in the series chosen to indicate the modes so inputs e and f are only enabled in mode 1 (for parallel loading) and input d is only enabled in mode 2 (for serial loading). The a input has three functions. It is the clock for entering data. In mode 2, it causes right shifting of the data. In mode 3, it causes the contents of the register to be incremented by one count.



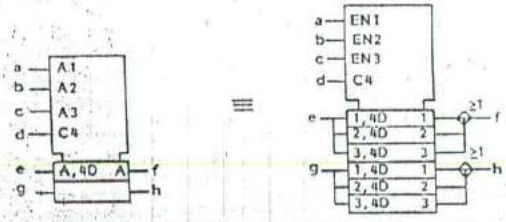
When a = 1 the d output takes on three-state characteristics.

When a = 0, the d output takes on open collector characteristics.

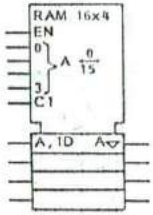
When a = 1 output b will stand at its internal 1 state only when the content of the register = 9.

Since output b is located in the common control block with no defined function outside of mode 1, the state of this output in mode 0 is not defined.

Two examples of mode dependency affecting outputs are shown above.



An example of A (address) dependency is shown above. The symbol represents a 3-word by 2-bit memory having a separate address line for each word. To select word 1, input a is taken to its 1 state, which enables mode 1. Data can now be clocked into the inputs marked 1,4D. Unless words 2 and 3 are also selected, data cannot be clocked in at the inputs marked 2,4D and 3,4D. The outputs will be the OR functions of the selected outputs (only those enabled by the active inputs).



Another example of address dependency is shown above. The symbol represents an array of 16 sections of four transparent latches with three-state outputs. This comprises a 16-word x 4-bit random access memory.

ANSWERS TO ODD-NUMBERED CHAPTER REVIEW QUESTIONS

CHAPTER 1

1-1. microprocessor
1-3. robot
1-5. preventive
1-7. $5000
1-9. signal
1-11. the protective ground

CHAPTER 2

2-1. minority
2-3. no
2-5. 50.6 mA
2-7. it increases
2-9. they are higher
2-11. cutoff, linear, and saturation
2-13. off
2-15. 5 S
2-17. I_H
2-19. it decreases
2-21. snap-on or hysteresis
2-23. no
2-25. non-registered

CHAPTER 3

3-1. false
3-3. PM
3-5. 10.0
3-7. cogging
3-9. true
3-11. full
3-13. toothed
3-15. 32 rpm
3-17. half
3-19. 90
3-21. 36
3-23. stall
3-25. increase
3-27. six

CHAPTER 4

4-1. 3 × 4, 4 × 4
4-3. 0.1 μF; 2.5 Ω
4-5. less; almost zero
4-7. mercury
4-9. on; saturated
4-11. open
4-13. can stick or react slowly
4-15. coil
4-17. false
4-19. interlocks direction changing
4-21. physical size; inches versus millimeters

CHAPTER 5

5-1. 14 h; indefinite
5-3. 180 Hz
5-5. 125 μF
5-7. 338 V
5-9. 1.5 Ω
5-11. 5000 V
5-13. D_1
5-15. 245 kHz
5-17. none
5-19. no output
5-21. no output and blown fuse
5-23. low output at normal load current (premature limiting)

CHAPTER 6

6-1. in saturation
6-3. R_{B1} and R_{B2}
6-5. to increase ac voltage gain
6-7. in phase (0°)
6-9. input offset voltage
6-11. none
6-13. 1 mA; same
6-15. −2 V
6-17. to decrease drift due to offset voltage
6-19. yes
6-21. 5 Hz
6-23. −3 V; quadrant II
6-25. 7.07 V
6-27. to reduce drift
6-29. positive saturation

CHAPTER 7

7-1. dots
7-3. twin
7-5. no signal
7-7. lock-up
7-9. false
7-11. four
7-13. pulses
7-15. lock-up (latch)

CHAPTER 8

8-1. true
8-3. rate
8-5. false
8-7. false
8-9. overheat
8-11. two-thirds
8-13. true
8-15. interphase
8-17. fused
8-19. ring counter

CHAPTER 9

9-1. increase
9-3. 0.05 V
9-5. to sense direction
9-7. low
9-9. nutating disk flowmeter
9-11. thermocouple
9-13. thermocouple
9-15. fast
9-17. 119.25 Ω
9-19. ionization
9-21. scintillation counter
9-23. the reference junctions would not be isothermal with the compensation circuit

CHAPTER 10

10-1. absolute
10-3. false
10-5. 70.7 V
10-7. the direction reverses
10-9. false
10-11. false
10-13. differential
10-15. true
10-17. false
10-19. tachometer (rate generator)
10-21. false
10-23. 90
10-25. power/rotating

10-27. brushes
10-29. zero
10-31. backlash

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