

## BIBLIOGRAPHY

- Ackerman, W. B., and Dennis, J. B., "VAL—A Value-Oriented Algorithmic Language," *TR-218*, Lab. for Computer Science, MIT, June 1979.
- Agerwala, T., "Some Extended Semaphore Primitives," *Acta Informatica 8*, Springer Verlag, 1977.
- Agrawal, D. P., "Graph Theoretical Analysis and Design of Multistage Interconnection Networks," *IEEE Trans. on Comp.*, C-32, July 1983, pp. 637-648.
- Algire, J. L., and Hwang, K., "Sparse Matrix Techniques for Circuit Analysis on the Cyber 205," *TR-EE 83-40*, Purdue University, W. Lafayette, Indiana, October 1983.
- Amdahl Corp., *Amdahl 470 V/6 Machine Reference Manual*, Sunnyvale, California, 1975.
- Amdahl, G. M., Blaauw, G. A., and Boork, F. J., Jr., "Architecture of the IBM System/360," *IBM Journ. of Res. and Dev.*, vol. 8, no. 2, 1964, pp. 87-101.
- Anderson, D. W., Earle, J. G., Goldschmidt, R. E., and Powers, D. M., "The IBM System/360 Model 91: Floating-Point Execution Unit," *IBM Journ. of Res. and Dev.*, January 1967a, pp. 34-53.
- Anderson, D. W., Sparacio, F. A., and Tomasulo, R. M., "The IBM System/360 Model 91: Machine Philosophy and Instruction Handling," *IBM Journ. of Res. and Dev.*, vol. 11, no. 1, 1967b, pp. 8-24.
- Anderson, J. P., Hoffman, S. A., Shifman, J., and Williams, R. J., "D825-A Multiple Computer System for Command and Control," *Proc. AFIPS Fall Joint Computer Conference*, vol. 22, 1962, pp. 86-96.
- Andrews, G. J., and McGraw, J. R., "Language Features for Parallel Processing and Resource Control," *Proceedings of the Conference on Design and Implementation of Programming Languages*, Ithaca, N.Y., October 1976.
- Andrews, G. R., and Schneider, F. B., "Concepts and Notations for Concurrent Programming," *ACM Computing Surveys*, vol. 15, March 1983, pp. 3-43.
- Arnold, C. N., "Performance Evaluation of Three Automatic Vectorizer Packages," *Proc. of Int'l. Conf. Parallel Proc.*, 1982, pp. 235-242.
- Arnold, J. S., Casey, D. P., and McKinstry, R. H., "Design of Tightly-Coupled Multiprocessing Programming," *IBM Systems Journal*, no. 1, 1974.
- Arvind and Gostelow, K. P., "A Computer Capable of Exchanging Processors for Time," *Proc. 1977 IFIP Congress*, North-Holland, Amsterdam, 1977.
- Arvind and Gostelow, K. P., "The U Interpreter," *IEEE Comp.*, vol. 15, no. 2, Feb. 1982, pp. 42-50.
- Arvind and Iannucci, R. A., "A Critique of Multiprocessing von Neumann Style," *Proc. 10th Ann. Symp. Computer Architecture*, June 1983, pp. 426-436.
- Arvind, Kathail, V., and Pingali, K., "A Data Flow Architecture with Tagged Tokens," *Technical Memo 174*, Lab. for Computer Science, MIT, Sept. 1980.
- Association of Computing Machinery, "Special Issue on Computer Architecture," *Comm. of ACM*, vol. 21, no. 1, Jan. 1978.

- Backus, J., "Can Programming Be Liberated from the von Neumann Style? A Functional Style and Its Algebra of Programs," *Comm. of ACM*, vol. 21, no. 8, Aug. 1978, pp. 613-641.
- Baer, J. L., "A Survey of Some Theoretical Aspects of Multiprocessing," *ACM Computing Surveys*, vol. 5, no. 1, March 1973, pp. 31-80.
- Baer, J. L., "Multiprocessing Systems," *IEEE Trans. on Comp.*, C-25, Dec. 1976, pp. 1271-1277.
- Baer, J. L., *Computer Systems Architectures*. Computer Science Press, Potomac, Maryland, 1980.
- Baer, J. L., and Bovet, D. P., "Compilation of Arithmetic Expressions for Parallel Computations," *Proc. IFIP Congress 1968*, North-Holland, Amsterdam, 1968; pp. 340-346.
- Baer, J. L., and Ellis, C., "Model, Design, and Evaluation of a Compiler for a Parallel Processing Environment," *IEEE Trans. on Soft. Eng.*, SE-3, Nov. 1977, pp. 394-405.
- Bain, W. L., Jr., and Ahuja, S. R., "Performance Analysis of High-Speed Digital Buses for Multiprocessing Systems," *Proc. 8th Ann. Symp. Computer Architecture*, May 1981, pp. 107-131.
- Banerjee, U., Gajski, D., and Kuck, D., "Accessing Sparse Arrays in Parallel Memories," *Journ. of VLSI and Computer Systems*, vol. 1, no. 1, 1983, pp. 69-99.
- Barke, D. F., ed., *Very Large Scale Integration (VLSI): Fundamentals and Applications*. Springer-Verlag, New York, 1980.
- Barnes, G. H., Brown, R. M., Kate, M., Kuck, D. J., Slotnick, D. L., and Stokes, R. A., "The ILLIAC IV Computer," *IEEE Trans. on Computers*, Aug. 1968, pp. 746-757.
- Baskett, F., and Keller, T. W., "An Evaluation of the CRAY-I Computer," *High Speed Computer and Algorithm Organization*, Kuck, et al., eds., Academic Press, New York, 1977, pp. 71-84.
- Baskett, F., and Smith, A. J., "Interference in Multiprocessor Computer Systems with Interleaved Memory," *Comm. of ACM*, vol. 19, no. 6, June 1976, pp. 327-334.
- Batcher, K. E., "STARAN Parallel Processor System Hardware," *Proc. AFIPS-NCC*, vol. 43, pp. 405-410.
- Batcher, K. E., "The Flip Network in STARAN," *Int'l. Conf. Parallel Proc.*, Aug. 1976, pp. 65-71.
- Batcher, K. E., "The Multi-dimensional Access Memory in STARAN," *IEEE Trans. on Comps.*, 1977, pp. 174-177.
- Batcher, K. E., "Design of a Massively Parallel Processor," *IEEE Trans. on Comp.*, C-29, Sept. 1980, pp. 836-840.
- Baudet, G. M., "Asynchronous Iterative Methods for Multiprocessors," *Journ. of ACM*, vol. 25, no. 2, Apr. 1978, pp. 226-244.
- Bauer, L. H., "Implementation of Data Manipulating Functions on the STARAN Associative Array Processor," *Proc. Sagamore Comp. Conf. Parallel Proc.*, Aug. 1974, pp. 209-227.
- Bell, C. G., Mudge, J. C., and McNamara, J., *Computer Engineering: A DEC View of Hardware Systems Design*, Digital Press, Bedford, Mass., 1978.
- Bell, J., Casasent, D., and Bell, C. G., "An Investigation of Alternative Cache Organizations," *IEEE Trans. on Comp.*, C-23, Apr. 1974, pp. 346-351.
- Benes, V. E., *Mathematical Theory of Connecting Networks and Telephone Traffic*. Academic Press, New York, 1965.
- Bensoussan, A., Clingen, C. T., and Daley, R. C., "The MULTICS Virtual Memory: Concepts and Design," *Comm. of ACM*, vol. 15, May 1972, pp. 308-315.
- Bernstein, A. J., "Analysis of Programs for Parallel Processing," *IEEE Trans. Elec. Comp.*, E-15, Oct. 1966, pp. 746-757.
- Berra, P. B., and Oliver, E., "The Role of Associative Array Processors in Database Machine Architecture," *IEEE Comp.*, Mar. 1979, pp. 53-61.
- Bhandarkar, D. P., "Analysis of Memory Interference in Multiprocessors," *IEEE Trans. on Comp.*, C-24, Sept. 1975, pp. 897-908.
- Bhandarkar, D. P., "Some Performance Issues in Multiprocessor System Design," *IEEE Trans. on Comp.*, C-26, no. 5, May 1977, pp. 506-511.
- Blaauw, G., "Computer Architecture," *Electronische Rechenanlagen*, vol. 14, no. 4, 1972, pp. 154-160.
- Blaauw, G., *Digital Systems Implementation*. Prentice-Hall, Englewood Cliffs, N.J., 1976.
- Bode, A., and Händler, W., *Rechnerarchitektur: Grundlagen und Verfahren*. Springer-Verlag, Berlin (volumes 1 and 2), 1980, 1982.

- Borgeson, B. R., Hanson, M. L., and Hartley, P. A., "The Evolution of the Sperry Univac 1100 Series: A History, Analysis, and Projection," *Comm. of ACM*, vol. 21, no. 1, Jan. 1978, pp. 25-43.
- Bouknight, W. J., Denenberg, S. A., McIntyre, D. E., Randall, J. M., Samch, A. H., and Slotnick, D. L., "The Illiac IV System," *Proc. IEEE*, vol. 60, no. 4, Apr. 1972, pp. 369-388.
- Bovet, D. P., and Vanneschi, M., "Models and Evaluation of Pipeline Systems," *Computer Architectures and Networks* (Gelenbe and Mahl, eds.), North Holland, Amsterdam, 1976, pp. 99-111.
- Brent, R., "The Parallel Evaluation of General Arithmetic Expressions," *Journ. of ACM*, vol. 21, no. 2, Apr. 1974, pp. 201-206.
- Briggs, F. A., "Performance of Memory Configurations for Parallel-Pipelined Computers," *Proc. 5th Ann. Symp. Computer Architecture*, Apr. 1978, pp. 202-209.
- Briggs, F. A., "Effects of Buffered Memory Requests in Multiprocessor Systems," *Proc. ACM/SIGMETRICS Conf. on Simulation, Measurement and Modeling of Comput. Systems*, 1979, pp. 73-81.
- Briggs, F. A., and Davidson, E. S., "Organization of Semiconductor Memories for Parallel-Pipelined Processors," *IEEE Trans. on Comp.*, Feb. 1977, pp. 162-169.
- Briggs, F. A., and Dubois, M., "Modeling of Synchronized Iterative Algorithms for Multiprocessors," *Proc. 18th Ann. Allerton Conf. on Communication, Control and Computing*, Oct. 1980, pp. 554-563.
- Briggs, F. A., and Dubois, M., "Performance of Cache-Based Multiprocessors," *Proc. ACM/SIGMETRICS Conf. on Measurement and Modeling of Computer Systems*, Sept. 1981.
- Briggs, F. A., and Dubois, M., "Effectiveness of Private Caches in Multiprocessor Systems with Parallel-Pipelined Memories," *IEEE Trans. on Comp.*, C-32, no. 1, Jan. 1983, pp. 48-59.
- Briggs, F. A., Dubois, M., and Hwang, K., "Throughput Analysis and Configuration Design of a Shared-Resource Multiprocessor Systems: PUMPS," *Proc. 8th Ann. Symp. Computer Architecture*, May 1981, pp. 67-80.
- Briggs, F. A., Fu, K. S., Hwang, K., and Patel, J. H., "PM<sup>4</sup>: A Reconfigurable Multiprocessor System for Pattern Recognition and Image Processing," *Proc. of NCC, AFIPS*, June 1979, pp. 255-265.
- Briggs, F. A., Fu, K. S., Hwang, K., and Wah, B. W., "PUMPS Architecture for Pattern Analysis and Image Database Management," *IEEE Trans. on Comp.*, C-31, no. 10, Oct. 1982, pp. 969-982.
- Browning, S. A., "The Tree Machine: A Highly Concurrent Computing Environment," Ph.D. Thesis, Dept. of Computer Science, Cal. Tech., Pasadena, 1980.
- Bucher, I. Y., "The Computational Speed of Supercomputers," *Proc. ACM/SIGMETRICS Conf. on Measurement and Modeling of Computer Systems*, Aug. 1983, pp. 151-165.
- Buchholz, W., *Planning a Computer System: Project Stretch*, McGraw-Hill, New York, 1962.
- Budnik, P. P., and Kuck, D. J., "The Organization and Use of Parallel Memories," *IEEE Trans. on Comp.*, vol. 20, Dec. 1971, pp. 1566-1569.
- Burnett, G. J., and Coffman, E. G., "A Study of Interleaved Memory Systems," *Proc. Spring Joint Computer Conf., AFIPS, SJCC*, vol. 36, 1970, pp. 467-474.
- Burroughs Co., "BSP: Overview Perspective, and Architecture," document no. 61391, Feb. 1978a (30 pages).
- Burroughs Co., "BSP: Floating Point Arithmetic," document no. 61416, 1978b (27 pages).
- Burroughs Co., "BSP: Implementation of FORTRAN," document no. 16391, Nov. 1977 (18 pages).
- Buzen, J. P., "I/O Subsystem Architecture," *Proc. IEEE*, 63, June 1975, pp. 871-879.
- Cappa, M., and Hamacher, V. C., "An Augmented Iterative Array for High-Speed Array Division," *IEEE Trans. on Comp.*, C-22, Feb. 1973, pp. 172-175.
- Carlson, W. W., and Hwang, K., "On Structural Data Accessing in Dataflow Computers," *Proc. 1st Int'l. Conf. Computers and Applications*, Beijing, China, June 1984.
- Case, R. P., and Padegs, A., "Architecture of the IBM System 370," *Comm. of ACM*, vol. 21, no. 1, 1978, pp. 73-96.
- Censi, L. M., and Feautrier, P., "A New Solution to Coherence Problems in Multicache Systems," *IEEE Trans. on Comp.*, C-27, Dec. 1978, pp. 1112-1118.
- Chamberlin, D. D., "Parallel Implementation of a Single Assignment Language," Ph.D. Thesis, Stanford Univ., Calif., 1971.
- Chamberlin, D. D., Fuller, S. H., and Liu, L. Y., "An Analysis of Page Allocation Strategies for Multiprogramming Systems with Virtual Memory," *IBM Journ. of Res. and Dev.*, 1973.

- Chandy, K. M., "Models for the Recognition and Scheduling of Parallel Tasks on Multiprocessor Systems," *Bulletin of the Operations Research Society of America*, vol. 23, suppl. 1, Spring 1975, p. B-117.
- Chang, D., Kuck, D. J., and Lawrie, D. H., "On the Effective Bandwidth of Parallel Memories," *IEEE Trans. on Comp.*, C-26, no. 5, May 1977, pp. 480-490.
- Charlesworth, A. E., "An Approach to Scientific Array Processing: The Architecture Design of the AP-120B/FPS-164 Family," *IEEE Comp.*, Dec. 1981, pp. 12-30.
- Chen, N. F., and Liu, C. L., "On a Class of Scheduling Algorithms for Multiprocessor Computing Systems," *Proc. Conf. on Parallel Proc.*, Raquette Lake, N.Y., August 1974.
- Chen, S. C., "Speedup of Iterative Programs in Multiprocessor Systems," *Ph.D. Thesis*, Univ. of Ill. at Urb.-Champ., Dept. of Computer Science, no. 75-694, Jan. 1975.
- Chen, S. C., "Large-Scale and High-Speed Multiprocessor System for Scientific Applications: Cray X-MP Series," *Proc. NATO Advanced Research Workshop on High-Speed Computing*, J. Kawalik, editor, Springer Verlag, Jülich, W. Germany, June 20-22, 1983.
- Chen, T. C., "Parallelism, Pipelining, and Computer Efficiency," *Computer Design*, Jan. 1971, pp. 69-74.
- Chen, T. C., "Overlap and Pipeline Processing," in *Introduction to Computer Architecture*, Chap. 9 (Stone, ed.), Science Research Associates, Inc., Chicago, 1980, pp. 427-486.
- Chin, C. Y., and Hwang, K., "Connection Principles of Multipath Packet Switching Networks," *Proc. 11th Ann. Symp. Computer Architecture*, Ann Arbor, Mich., June 1984.
- Chow, C. K., "On Optimization of Storage Hierarchies," *IBM Journ. of Res. and Dev.*, May 1974, pp. 194-203.
- Chu, Y., *High Level Language Computer Architecture*, Academic Press, New York, 1975.
- Chu, Y., and Abrams, M., "Programming Languages and Direct-Execution Computer Architecture," *IEEE Comp.*, vol. 14, July 1981, pp. 22-40.
- Coffman, E. G., "Bounds on Parallel Processing of Queues with Multiple Jobs," *Naval Research Logical Quarterly*, 14, Sept. 1967, pp. 345-366.
- Coffman, E. G., Elphick, M. J., and Shoshani, A., "System Deadlocks," *ACM Computer Surveys*, 3, 1971, pp. 67-78.
- Coffman, E. G., and Denning, P. J., *Operating Systems Theory*, Prentice-Hall, Englewood Cliffs, N.J., 1973.
- Coffman, E. G., and Graham, R. L., "Optimal Scheduling for Two Processor Systems," *Acta Informatica*, vol. 1, 1972, pp. 200-213.
- Coffman, E. G., and Ryan, T. J., Jr., "A Study of Storage Partitioning Using a Mathematical Model of Locality," *Comm. of ACM*, vol. 15, Mar. 1972, pp. 185-190.
- Coffman, E. G., ed., *Computer and Job-Shop Scheduling Theory*, John Wiley, New York, 1976.
- Cohen, E., and Jefferson, D., "Protection in the Hydra Operating System," *Proc. 5th Symp. on Operating System Principles*, Nov. 1975, pp. 141-160.
- Cohen, T., "Structured Flowcharts for Multiprocessing," *Computer Languages*, vol. 13, no. 4, 1978, pp. 209-226.
- Connors, W. D., Florkowski, J. H., and Patton, S. K., "The IBM 3033: An Inside Look," *Datamation*, May 1979, pp. 198-218.
- Conrad, V., and Wallach, "Iterative Solution of Linear Equations on a Parallel Processor System," *IEEE Trans. on Comp.*, Sept. 1977, pp. 838-847.
- Conti, C. J., "Concepts for Buffer Storage," *Computer Group News*, 2, Mar. 1969, pp. 9-13.
- Conti, C. J., Gibson, D. H., and Pikowsky, S. H., "Structural Aspects of the System 360/85; General Organization," *IBM Systems Journ.*, 1968, pp. 2-14.
- Control Data Corp., *Control Data STAR-100 Features Manual*, St. Paul, Minn., pub. no. 60425500, Oct. 1973.
- Control Data Corp., *Control Data STAR-100 FORTRAN Language Version 2 Reference Manual*, St. Paul, Minn., pub. no. 60386200, 1976.
- Control Data Corp., *CDC Cyber 200 Operating System 1.4 Reference Manual*, St. Paul, Minn., pub. no. 60457000, vol. 1, 1979a.

- Control Data Corp., *CDC Cyber 200 Fortran Language 1.4 Reference Manual*, St. Paul, Minn., pub. no. 60456040, 1979.
- Control Data Corp., *CDC Cyber 200/Model 205 Technical Description*, St. Paul, Minn., Nov. 1980.
- Conway, M., "A Multiprocessor System Design," *Proc. AFIPS Fall Joint Comput. Conf.*, Spartan Books, N.Y., 1963, pp. 139-146.
- Cooper, R. G., "The Distributed Pipeline," *IEEE Trans. Comp.*, Nov. 1977, pp. 1123-1132.
- Cordennier, V., "A Two Dimension Pipelined Processor for Communication in a Parallel System," *Proc. 1975 Sagamore Comp. Conf. Parallel Proc.*, 1975, pp. 115-121.
- Crane, B. A., Gilmarin, M. J., Huttenhoff, J. H., Rus, P. T., and Shively, R. R., "PEPE Computer Architecture," *IEEE Compcon*, 1972, pp. 57-60.
- Cray Research, Inc., *CRAY-1 Computer System Hardware Reference Manual*, Bloomington, Minn., pub. no. 2240004, 1977.
- Cray Research, Inc., *CRAY-1 Computer System Preliminary CRAY FORTRAN (CFT) Reference Manual*, Bloomington, Minn., pub. no. 2240009, 1978.
- Cray Research Inc., *CRAY-1 Fortran (CFT) Reference Manual*, Bloomington, Minn., pub. no. 2240009, Dec. 1979.
- Gustafson, R. N., and Sparacio, F. J., "IBM 3081 Processor Unit: Design Considerations and Design Process," *IBM Journ. of Res. and Dev.*, vol. 26, no. 1, Jan. 1982, pp. 12-21.
- Daley, R. C., and Dennis, J. B., "Virtual Memory Process and Sharing in Multics," *Comm. of ACM*, vol. 11, May 1968, pp. 306-311.
- Datawest Corp., "Real Time Series of Microprogrammable Array Transform Processors," *Prod. Bulletin Series B*, 1979.
- Davidson, E. S., "The Design and Control of Pipelined Function Generators," *Proc. 1971 Int'l. IEEE Conf. on Systems, Networks, and Computers*, Oaxtepec, Mexico, Jan. 1971, pp. 19-21.
- Davidson, E. S., "Scheduling for Pipelined Processors," *Proc. 7th Hawaii Conf. on System Sciences*, 1974, pp. 58-60.
- Davidson, E. S., Thomas, D. P., Shar, L. E., and Patel, J. H., "Effective Control for Pipelined Computers," *COMPON Proc.*, IEEE 75CH0920-9C, 1975, pp. 181-184.
- Davis, A. L., "The Architecture and System Methodology of DDM1: A Recursively Structured Data Driven Machine," *Proc. 5th Ann. Symp. on Computer Architecture*, 1978, pp. 210-215.
- Davis, C. G., and Vough, R. L., "Ballistic Missile Defense: A Supercomputer Challenge," *IEEE Comp.*, Nov. 1980, pp. 37-46.
- Deitel, H. M., *An Introduction to Operating Systems*, Addison-Wesley, Reading, Mass. 1984.
- Deminet, J., "Experience with Multiprocessor Algorithms," *IEEE Trans. on Comp.*, C-31, Apr. 1982, pp. 278-288.
- Denelcor, Inc., *Heterogeneous Element Processor: Principles of Operation*, April 1981.
- Denning, P. J., "The Working Set Model for Program Behavior," *Comm. of ACM*, vol. 11, no. 5, 1968, pp. 323-333.
- Denning, P. J., "Operating Systems Principles for Data Flow Networks," *IEEE Comp.*, July 1978, pp. 86-96.
- Denning, P. J., "Working Sets Past and Present," *IEEE Trans. on Soft. Eng.*, SE-6, no. 1, Jan. 1980.
- Denning, P. J., "Virtual Memory," *ACM Computing Surveys*, 2, Sept. 1970, pp. 153-189.
- Denning, P. J., and Graham, G. S., "Multiprogrammed Memory Management," *Proc. IEEE*, vol. 63, June 1975, pp. 924-939.
- Denning, P. J., and Schwartz, S. C., "Properties of the Working Set Model," *Comm. of ACM*, vol. 15, 1972.
- Dennis, J. B., "Data Flow Supercomputers," *IEEE Comp.*, Nov. 1980, pp. 48-56.
- Dennis, J. B., "First Version of a Data Flow Procedure Language," in *Lecture Notes in Computer Science*, 19, Springer-Verlag, Berlin, 1974, pp. 362-376.
- Dennis, J. B., Leung, C. K., and Misunas, D. P., "A Highly Parallel Processor Using a Data Flow Machine Language," *CSG Memo 134-1*, Lab. for Computer Science, MIT, June 1979.
- Dennis, J. B., and Misunas, D. P., "A Preliminary Architecture for a Basic Data Flow Processor," *Proc. Second Ann. Symp. on Computer Architecture*, IEEE, Jan. 1975, pp. 126-132.

- Dennis, J., and Rong, G., "Maximum Pipelining of Array Operations on Static Dataflow Machine," *Proc. 1983 Int'l. Conf. Parallel Proc.*, August 23-26, 1983.
- Dennis, J. B., and Weng, K., "Application of Dataflow Computation to the Weather Problem," *High Speed Computer and Algorithm Organization*, Kuck, et al., eds., New York: Academic Press, New York, 1977, pp. 143-157.
- Despain, A. M., and Patterson, D. A., "X-tree—A Tree Structured Multiprocessor Computer Architecture," *Proc. 5th Ann. Symp. on Computer Architecture*, 1978, pp. 144-151.
- Dias, D. M., and Jump, J. R., "Analysis and Simulation of Buffered Delta Networks," *IEEE Trans. on Comp.*, C-30, Apr. 1981a, pp. 273-282.
- Dias, D. M., and Jump, J. R., "Packet Switching Interconnection Networks for Modular Systems," *IEEE Comp.*, Dec. 1981b, pp. 43-53.
- Dijkstra, E. W., "Solution of a Problem in Concurrent Programming," *Comm. of ACM*, vol. 8, Sept. 1965, pp. 569-570.
- Dijkstra, E. W., "Cooperating Sequential Processes," *Programming Languages*, F. Genuys, ed., Academic Press, New York, 1968, pp. 43-112.
- Dorr, F. W., "The Cray-1 at Los Alamos," *Datumation*, Oct. 1978, pp. 113-120.
- Dowling, R. D., "Processor Management in a Multiprocessor System," *Electronic Letters*, vol. 12, no. 24, Nov. 1976.
- Dubois, M., "Analytical Methodologies for the Evaluation of Multiprocessing Structures," *Ph.D. Thesis*, Purdue Univ., Ind., 1982.
- Dubois, M., and Briggs, F. A., "Effects of Cache Coherency in Multiprocessors," *IEEE Trans. on Comp.*, C-31, no. 11, Nov. 1982a.
- Dubois, M., and Briggs, F. A., "Performance of Synchronized Iterative Processes in Multiprocessor Systems," *IEEE Trans. on Soft. Eng.*, July 1982b, pp. 419-431.
- Duff, M. J. B., ed., *Computing Structures for Image Processing*, Academic Press, London, 1983.
- El-Ayat, K. A., "The Intel 8089: An Integrated I/O Processor," *IEEE Comp.*, vol. 12, no. 6, June 1979, pp. 67-78.
- Emer, J. S., and Davidson, E. S., "Control Store Organization for Multiple Stream Pipelined Processors," *Proc. 1978 Int'l. Conf. Parallel Proc.*, 1978, pp. 43-48.
- Enslow, P. H., "Multiprocessor Organization," *Computing Surveys*, vol. 9, Mar. 1977, pp. 103-129.
- Enslow, P. H., ed., *Multiprocessors and Parallel Processing*, Wiley-Interscience, New York, 1974.
- Evans, D. J., ed., *Parallel Processing Systems*, Cambridge Univ. Press, England, 1982.
- Evensen, A. J., and Troy, J. L., "Introduction to the Architecture of a 288-Element PEPE," *Proc. Sagamore Conf. Parallel Proc.*, 1973, pp. 162-169.
- Fabry, R. S., "Capability-based Addressing," *Comm. of ACM*, vol. 17, July 1974, pp. 403-412.
- Faggin, F., "How VLSI Impacts Computer Architecture," *IEEE Spectrum*, 15, May 1978, pp. 28-31.
- Fairbairn, D. G., "VLSI: A New Frontier for System Designers," *IEEE Comp.*, Jan. 1982, pp. 87-96.
- Feierbach, G., and Stevenson, D. K., "The Phoenix Array Processing System," *Phoenix Project Memo*, 7, NASA Ames Research Center, Mountain View, Calif., Nov. 1978.
- Feldman, J. D., and Fulmer, L. C., "RADCAP: Operational Parallel Processing Facility," *Proc. Nat'l Comp. Conf.*, AFIPS, 1974, pp. 7-15.
- Feller, W., *An Introduction to Probability Theory and its Applications*, vol. 1, Wiley, New York, 1970.
- Femt, T. Y., "Some Characteristics of Associative Parallel Processing," *Proc. 1972 Sagamore Comp. Conf.*, Syracuse Univ., 1972, pp. 5-16.
- Feng, T. Y., "Data Manipulation Functions in Parallel Processors and Their Implementations," *IEEE Trans. on Comp.*, C-23, no. 3, Mar. 1974, pp. 309-318.
- Feng, T. Y., ed., "Parallel Processors and Processing," special issue, *ACM Computing Surveys*, vol. 9, no. 1, Mar. 1977a.
- Feng, T. Y., "Parallel Processors and Processing," *Class Notes*, Wayne State Univ., Detroit, Michigan (unpublished), 1977b.
- Feng, T. Y., "A Survey of Interconnection Networks," *IEEE Comp.*, Dec. 1981, pp. 12-27.
- Fennell, K. D., and Lesser, V. R., "Parallelism in Artificial Intelligence Problem Solving: A Case Study of Hearsay II," *IEEE Trans. on Comp.*, Mar. 1977, pp. 98-111.

- Ferrari, D., "An Analytic Study of Memory Allocation in Multiprocessing System," *Computer Architecture and Networks*, Gelenbe and Mahl, eds., North-Holland, Amsterdam, 1974.
- Ferrari, D., Gelenbe, E., and Mahl, R., "An Analytic Study of Memory Allocation in Multiprocessor Systems," *Proc. Conf. on Computer Architecture and Networks*, France, August 1974.
- Floating Point System, Inc., *AP-120B Processor Handbook*, Portland, Oregon, pub. no. 7259-02, May 1976.
- Flynn, M. J., "Very High-Speed Computing Systems" *Proc. IEEE*, vol. 54, 1966, pp. 1901-1909.
- Flynn, M. J., "Some Computer Organization and Their Effectiveness," *IEEE Trans. on Comp.*, C-21, no. 9, Sept. 1972, pp. 948-960.
- Flynn, M. J., "The Interpretive Interface: Resources and Program Representation in Computer Organization," *High Speed Computer and Algorithm Organization*, Kuck et al., Academic Press, New York, 1977, pp. 41-69.
- Flynn, M. J., and Amdahl, G. M., "Engineering Aspects of Large High Speed Computer Design," *Proc. Symp. Microelectronics and Large Systems*, Spartan Press, Washington, D.C., 1965, pp. 77-95.
- Flynn, M. J., Podvin, A., and Shmizu, K., "A Multiple Instruction Stream with Shared Resources," *Parallel Processor Systems, Technologies, and Applications*, Hobbs, ed., Spartan Books, Washington, D.C., 1970, pp. 251-286.
- Fontao, R. O., "A Concurrent Algorithm for Avoiding Deadlocks in Multiprocess Multiple Resonance Systems," *Proc. 3d Symp. Operating System Principles*, Oct. 1971.
- Foster, C. C. (1976). *Content-Addressable Parallel Processors*, Van Nostrand Reinhold Co., New York, 1976.
- Franta, W. R., and Houle, P. A., "Comments on Models of Multiprocessor Multi-Memory Bank Computer Systems," *Proc. 1974 Winter Simulation Conf.*, vol. I, Washington, D.C., Jan. 1974.
- Fritsch, G., Kleinroder, W., Linster, C. U., and Volkert, J., "EMSY 85: The Erlangen Multiprocessor System for a Broad Spectrum of Applications," *Proc. 1983 Int'l. Conf. on Parallel Proc.*, August 1983, pp. 325-330.
- Fuller, S. H., and Harbison, S. P., *The C.mmp Multiprocessor*, Technical Report, Carnegie-Mellon Univ., Computer Science Dept., 1978.
- Fuller, S. H., Swan, R., and Wulf, W. A., "The Instrumentation of C.mmp: A Multi-miniprocessor," *IEEE Compcon*, 1973.
- Gajski, D. D., "An Algorithm for Solving Linear Recurrence Systems on Parallel and Pipelined Machines," *IEEE Trans. on Comp.*, Mar. 1981, pp. 190-205.
- Gajski, D. D., Kuck, D. J., and Padua, D. A., "Dependence Driven Computation," *Proc. COMCON Spring*, Feb. 1981, pp. 168-172.
- Gajski, D., Kuck, D., Lawrie, D., and Sameh, A., "Cedar—A Large Scale Multiprocessor," *Proc. 1983 Int'l. Conf. on Parallel Proc.*, Aug. 1983, pp. 524-529.
- Gajski, D. D., Panda, D. A., Kuck, D. J., and Kuhn, R. H., "A Second Opinion on Dataflow Machines and Languages," *IEEE Comp.*, Feb. 1982, pp. 58-70.
- Gajski, D. D., and Rubinfield, L. P., "Design of Arithmetic Elements for Burroughs Scientific Processor," *Proc. 4th Symp. Computer Arithmetic*, Oct. 1978, pp. 245-256.
- Gao, Q. S., and Zhang, X., "Cellular Vector Computer of Vertical and Horizontal Processing with Vertical Common Memory," *Journ. of Computers*, no. 1, Jan. 1979, pp. 1-12 (in Chinese).
- Gao, Q. S., and Zhang, X., "Another Approach to Making Supercomputer by Microprocessors—Cellular Vector Computer of Vertical and Horizontal Processing with Virtual Common Memory," *Int. Conf. Parallel Proc.*, Aug. 1980, pp. 163-164.
- Gaudet, G., and Stevenson, D., "Optimal Sorting Algorithms for Parallel Computers," *IEEE Trans. on Comp.*, C-27, Jan. 1978, pp. 84-87.
- Gecsei, J., and Lukes, J. A., "A Model for the Evaluation of Storage Hierarchies," *IBM Systems Journ.*, no. 2, 1974, pp. 163-178.
- Ginsberg, M., "Some Numerical Effects of a FORTRAN Vectorizing Compiler on A Texas Instruments Advanced Scientific Computer," *High Speed Computer and Algorithm Organization*, Kuck, et al., eds., Academic Press, New York, 1977, pp. 461-62.

- Goke, R., and Lipovski, G. J., "Banyan Networks for Partitioning on Multiprocessor Systems," *Proc. 1st Ann. Symp. Computer Architecture*, 1973, pp. 21-30.
- Gonzalez, M. J., "Deterministic Processor Scheduling," *Computing Surveys*, vol. 9, no. 3, Sept. 1977, pp. 173-204.
- Gonzalez, M. J., and Ramamoorthy, C. V., "Recognition and Representation of Parallel Processable Streams in Computer Programs," in *Parallel Processor Systems, Technologies and Applications*, Macmillan Ltd., London, England, 1970.
- Gonzalez, M. J., and Ramamoorthy, C. V., "Parallel Task Execution in a Decentralized System," *IEEE Trans. on Comp.*, C-21, Dec. 1972, 1310-1322.
- Gonzalez, T., and Sahni, S., "Preemptive Scheduling of Uniform Processor Systems," *Journ. of ACM*, vol. 25, no. 1, Jan. 1978, pp. 92-101.
- Goodman, J. R., "An Investigation of Multiprocessor Structures and Algorithms for Database Management," *UCB/ERL M81/83*, Dept. of EECS, Univ. of Calif., Berkeley, 1981.
- Goodyear Aerospace Co., "Massively Parallel Processor (MPP)," Tech. Report GER-16684, July 1979.
- Gosden, J. A., "Explicit Parallel Processing Description and Control in Programs for Multi and Uniprocessor Computers," *AFIPS Fall Joint Comput. Conf.*, Spartan Books, N.Y., 1966, pp. 651-660.
- Gostelow, K. P., and Thomas, R. E., "Performance of a Simulatoc Dataflow Computer," *IEEE Trans. on Comp.*, Oct. 1980, pp. 905-919.
- Gottlieb, A., Grishman, R., Kruskal, C. P., McAuliffe, K. P., Randolph, L., and Snir, M., "The NYU Ultracomputer-Designing an MIMD Shared Memory Parallel Computer," *IEEE Trans. on Comp.*, Feb. 1983, pp. 175-189.
- Graham, G. S., *A Study of Program and Memory Policy Behavior*, Ph.D. Thesis, Purdue Univ., Ind., 1976.
- Graham, R. L., "Bounds on Multiprocessing Anomalies and Packing Algorithms," *Proc. AFIPS 1972 Spring Joint Comp. Conf.*, 40, AFIPS Press, Montvale, N.J., 1972, pp. 205-217.
- Graham, W. R., "The Parallel and the Pipeline Computers," *Datamation*, Apr. 1970, pp. 68-71.
- Grimsdale, R. L., and Johnson, D. M., "A Modular Executive for Multiprocessor Systems," *Proc. Conf. on Trends in One-Line Computer Control Systems*, Sheffield, England, Apr. 1972.
- Grinbert, J., Nudd, G. R., and Etchella, R. D., "A Cellular VLSI Architecture," *IEEE Comp.*, Jan. 1984.
- Grohoski, G. R., and Patel, J. H., "A Performance Model for Instruction Prefetch in Pipelined Instruction Units," *Proc. 1982 Int'l. Conf. Parallel Proc.*, August 24-27, 1982, pp. 248-252.
- Gula, J. L., "Operating System Considerations for Multiprocessor Architecture," *Proc. 7th Texas Conf. on Computing Systems*, Houston, Nov. 1978.
- Gurd, J., and Watson, I., "Data Driven System for High Speed Parallel Computing," *Computer Design*, Parts I & II, June & July 1980.
- Habermann, A. N., *Introduction to Operating System Design*, Science Res. Assoc., 1976.
- Hallin, T. G., and Flynn, M. J., "Pipelining of Arithmetic Functions," *IEEE Trans. on Comp.*, Aug. 1972, pp. 880-886.
- Händler, W., "The Impact of Classification Schemes on Computer Architecture," *Proc. 1977 Int. Conf. on Parallel Proc.*, pp. 7-15.
- Hansen, P. B., "The Programming Language Concurrent Pascal," *IEEE Trans. on Soft. Eng.*, 1, 2, June 1975, pp. 199-207.
- Hansen, P. B., *Concurrent Pascal*, Prentice-Hall, New York, 1978.
- Hansen, P. B., *The Architecture of Concurrent Programs*, Prentice-Hall, Englewood Cliffs, N.J., 1977.
- Harris, J. A., and Smith, D. R., "Hierarchical Multiprocessor Organizations," *Proc. 4th Symp. on Computer Architecture*, 1977.
- Hayes, J. P., *Computer Architecture and Organization*, McGraw-Hill, New York, 1978.
- Hedlund, K. S., "Wafer Scale Integration of Parallel Processors," Ph.D. Thesis, Comp. Science Dept., Purdue Univ., Ind., 1982.
- Hellerman, H., *Digital Computer System Principles*, McGraw-Hill, New York, 1967, pp. 228-229.
- Hellerman, H., and Smith, H. J., Jr., "Throughput Analysis of Some Idealized Input, Output, and Compute Overlap Configurations," *Computing Surveys*, 2, June 1970, pp. 111-118.

- Higbie, L. C., "Applications of Vector Processing," *Computer Design*, Apr. 1978, pp. 139-145.
- Higbie, L. C., "Supercomputer Architecture," *IEEE Comp.*, 6, Dec. 1973, pp. 48-58.
- Hintz, R. G., and Tate, D. P., "Control Data STAR-100 Processor Design," *COMPCON Proc.*, Sept. 1972, pp. 1-4.
- Hoare, C. A. R., "Towards a Theory of Parallel Programming," *Operating Systems Techniques*, C. A. R. Hoare, ed., Academic Press, New York, 1972.
- Hoare, C. A. R., "Monitors: An Operating System Structuring Concept," *Comm. of ACM*, vol. 17, no. 10, Oct. 1974, pp. 549-557.
- Hockney, R. W., and Jesshope, C. R., *Parallel Computers: Architecture, Programming and Algorithms*, Adam Hilger Ltd., Bristol, England, 1981.
- Holley, L. H., Parmlee, R. P., et al., "VM/370 Asymmetric Multiprocessing," *IBM Systems Journ.*, vol. 18, no. 1, 1979.
- Holt, R. C., "Some Deadlock Properties of Computer Systems," *ACM Computing Surveys*, 4, Sept. 1972, 179-195.
- Holt, R. C., Graham, G. S., Lazowska, E. D., and Scott, M. A., *Structured Concurrent Programming with Operating Systems Applications*, Addison-Wesley, Mass., 1978.
- Hon, R., and Reddy, D. R., "The Effect of Computer Architecture on Algorithm Decomposition and Performance," *High-Speed Computers and Algorithm Organization*, Kuck, et al., ed., Academic Press, New York, 1977, pp. 411-421.
- Hoogendoorn, C. H., "A General Model for Memory Interference in Multiprocessors," *IEEE Trans. on Comp.*, C-26, no. 10, Oct. 1977a, pp. 998-1005.
- Hoogendoorn, C. H., "Reduction of Memory Interference in Multiprocessor Systems," *Proc. 4th Ann. Symp. on Computer Architecture*, Silver Springs, MD, Mar. 1977b, pp. 179-183.
- Hsiao, D. K., "Data Base Computers," in *Advances in Computers*, vol. 19, Yovits, ed., Academic Press, New York, 1980, pp. 1-64.
- Hsiao, D. K., ed., *Advanced Database Machine Architecture*, Prentice-Hall, Englewood Cliffs, N.J., 1983.
- Hu, T. C., "Parallel Sequencing and Assembly Line Problems," *Oper. Res.*, vol. 9, no. 6, Nov.-Dec., 1961, pp. 841-848.
- Hufnagel, S., "Comparison of Selected Array Processor Architecture," *Computer Design*, Mar. 1979, pp. 151-158.
- Hwang, K., "Fault-Tolerant Microprogrammed Digital Controller Design," *IEEE Trans. on Industrial Electronics and Control Instrumentation*, Aug. 1976, pp. 200-207.
- Hwang, K., "Global and Modular Two's Complement Array Multipliers," *IEEE Trans. on Comp.*, Apr. 1979a, pp. 300-306.
- Hwang, K., *Computer Arithmetic: Principles, Architecture and Design*, Wiley, New York, 1979b.
- Hwang, K., "VLSI Computer Arithmetic for Real-Time Image Processing," Chap. 7, *VLSI Electronics: Microstructure Science*, vol. 7, Einpruch, ed., Academic Press, New York, 1984.
- Hwang, K., and Chang, T. P., "Combinatorial Reliability Analysis of Multiprocessor Computers," *IEEE Trans. Reliability*, vol. R-31, no. 5, Dec. 1982, pp. 469-473.
- Hwang, K., and Cheng, Y. H., "Partitioned Matrix Algorithms for VLSI Arithmetic Systems," *IEEE Trans. on Comp.*, C-31, no. 12, Dec. 1982, pp. 1215-1224.
- Hwang, K., Chin, C. Y., and Ni, L. M., "Adaptive Path-Directed Routing for Packet Switched Computer Networks," *TR-EE 83-37*, Purdue Univ., Ind., 1983.
- Hwang, K., and Fu, S. K., "Integrated Computer Architectures for Image Processing and Database Management," *IEEE Comp.*, vol. 16, no. 1, Jan. 1983, pp. 51-61.
- Hwang, K., and Kuhn, R. H., eds. *Tutorial on Supercomputers Design and Applications*, IEEE Computer Society Press (in press).
- Hwang, K., and Ni, L. M., "Resource Optimization of a Parallel Computer for Multiple Vector Processing," *IEEE Trans. on Comp.*, C-29, Sept. 1980, pp. 831-836.
- Hwang, K., and Su, S. P., "VLSI Architectures of Feature Extraction and Pattern Classification," *Computer Vision, Graphics, and Image Processing*, vol. 24, Academic Press, New York, Nov. 1983a, pp. 215-228.
- Hwang, K., and Su, S. P., "Priority Scheduling in Event-Driven Dataflow Computers," *TR-EE 83-56*, Purdue Univ., Ind. Dec. 1983b.

- Hwang, K., and Su, S. P., "Multitask Scheduling in Vector Supercomputers," *TR-EE 83-52*, Purdue Univ., Ind., Dec. 1983c.
- Hwang, K., Su, S. P., and Ni, L. M., "Vector Computer Architecture and Processing Techniques," *Advanced in Computers*, vol. 20, Yovits, ed., Academic Press, New York, 1981, pp. 115-197.
- Hwang, K., and Yao, S. B., "Optimal Batched Searching of Tree-Structural Files in Multiprocess Computer System," *Journ. of Assoc. of Comp. Mach.*, vol. 24, no. 3, July 1977, pp. 441-454.
- IBM Corp., *IBM System/360 and System/370 I/O Interface Channel to Control Unit*, form GA22-6974-3, 1976.
- IBM Corp., *IBM 3838 Array Processor Functional Characteristics*, no. 6A24-3639-0, file no. S370-08, Endicott, N.Y., Oct. 1976.
- IBM Corp., *IBM System/370 Model 168 Functional Characteristics*, form no. GA22-7010-4, 1976.
- IBM Corp., *3033 Processor Complex Theory of Operation/Diagrams Manual*, vols. 1-5, SY22-7001 through SY22-7005, Jan. 1978.
- IBM Corp., "Special Issue on IBM 3081," *IBM Journ. of Res. and Dev.*, vol. 26, no. 1, Jan. 1982, pp. 2-29.
- IBM Corp., *System/370 Principles of Operation*, GA22-7000-4, 1974.
- Islor, S. S., and Marsland, T. A., "The Deadlock Problem: An Overview," *IEEE Computer*, vol. 13, no. 9, Sept. 1980.
- Jain, N., *Performance Study of Synchronization Mechanisms in a Multiprocessor*, Ph.D. Thesis, Carnegie-Mellon Univ., 1979.
- Jensen, J. E., and Baer, J. L., "A Model of Interference in a Shared Resource Multiprocessor," *Proc. 3d Ann. Symp. on Computer Architecture*, Clearwater, Fla., Jan. 1976, pp. 52-57.
- Jin, L., "A New General-Purpose Distributed Multiprocessor Structure," *Proc. Int'l. Conf. on Parallel Proc.*, Aug. 1980, pp. 153-154.
- Johnson, L., "Gaussian Elimination on Sparse Matrices and Concurrency," *Tech. Report 4087*, TR-80, Dept. of Computer Science, Cal. Tech., Pasadena, 1980.
- Jones, A. K., and Gehringer, E. F. (Editor), "Cm\* Multiprocessor Project: A Research Review," *Tech. Rept. CMU-CS-80-131*, Carnegie-Mellon Univ., July 1980.
- Jones, A. K., and Schwarz, P., "Experience Using Multiprocessor Systems: A Status Report," Dept. of Computer Science, Carnegie-Mellon Univ., Tech. Report CMU-CS-79-146, Oct. 1979.
- Jordan, H. F., "Performance Measurement of HEP-A Pipelined MIMD Computer," *Proc. 10th Ann. Symp. Computer Architecture*, June 1983, pp. 207-212.
- Jordan, H. F., Scalabrin, M., and Calvert, W., "A Comparison of Three Types of Multiprocessor Algorithms," *Proc. 1979 Int'l. Conf. on Parallel Proc.*, Bellaire, MI, Aug. 1979, pp. 231-238.
- Jump, J. R., and Ahuja, S. R., "Effective Pipelining of Digital Systems," *IEEE Trans. on Comp.*, Sept. 1978, pp. 855-865.
- Kaplan, K. R., and Winder, R. V., "Cache-Based Computer Systems," *Computer*, 6, Mar. 1973, 30-36.
- Karp, K. M., and Miller, R. E., "Properties of a Model for Parallel Computations: Determinacy, Terminating, Queueing," *SIAM Journal of Applied Mathematics*, vol. 24, Nov. 1966, pp. 1390-1411.
- Karplus, W. J., and Cohen, D., "Architectural and Software Issues in the Design and Application of Peripheral Array Processors," *IEEE Comp.*, Sep. 1981, pp. 11-17.
- Kartashev, S. I., and Kartashev, S. P., "Problems of Designing Supersystems with Dynamic Architectures," *IEEE Trans. on Comp.*, Dec. 1980, pp. 1114-1132.
- Kasic, M. J., *Vector Processing on the Cyber 200*, Control Data Corp, 1979 (38 pages).
- Katzan, H., *Computer Organization and the System/360*, Van Nostrand Reinhold, New York, 1971.
- Kaufman, M., "An Almost-optimal Algorithm for the Assembly-line Scheduling Problem," *IEEE Trans. on Comp.*, C-23, Nov. 1974, pp. 1169-1174.
- Keller, R. M., "Look-Ahead Processors," *ACM Computing Surveys*, vol. 7, no. 4, Dec. 1975, pp. 177-195.
- Keller, R. M., Patil, S. S., and Lindstrom, G., "A Loosely Coupled Applicative Multiprocessing System," *Proc. Nat'l. Computer Conf.*, AFIPS Press, 1979.
- Kennedy, K., "Optimization of Vector Operations in an Extended Fortran Compiler," *IBM Research Report*, RC-7784, 1979.

- Kinney, L. L., and Arnold, R. G., "Analysis of a Multiprocessor System with a Shared Bus," *Proc. 5th Ann. Symp. on Computer Architecture*, Palo Alto, CA, Apr. 1978, pp. 89-95.
- Kleinrock, L. *Queueing Systems: Theory and Applications*, Wiley, New York, 1975.
- Knuth, D. E., and Rao, G. S., "Activity in Interleaved Memory," *IEEE Trans. on Comp.*, C-24, no. 9, Sept. 1975, pp. 943-944.
- Kober, R., and Kuznia, C., "SMS—A Multiprocessor Architecture for High-Speed Numerical Calculations," *Proc. Int'l. Conf. Parallel Proc.*, 1978, pp. 18-23.
- Kogge, P. M., "The Microprogramming of Pipelined Processors," *Proc. 4th Ann. Conf. Computer Architecture*, IEEE no. 77CH 1182-5C, Mar. 1977a, pp. 63-69.
- Kogge, P. M., "Algorithm Development for Pipelined Processors," *Proc. 1977 Int'l. Conf. Parallel Proc.*, IEEE no. 77 CH1253-4C, Aug. 1977b, p. 217.
- Kogge, P. M., *The Architecture of Pipelined Computers*, McGraw-Hill, New York, 1981.
- Kogge, P. M., and Stone, H. S., "A Parallel Algorithm for the Efficient Solution of a General Class of Recurrence Equations," *IEEE Trans. on Comp.*, C-22, 1973, pp. 786-793.
- Kosinski, P. R., "A Data Flow Programming Language," *Report RC4264*, IBM, T. J. Watson Research Center, Yorktown Heights, N.Y., Mar. 1973.
- Kozdrowicki, E. W., and Theis, D. J., "Second Generation of Vector Supercomputers," *IEEE Computer*, Nov. 1980, pp. 71-83.
- Kraley, M. F., "The Pluribus Multiprocessor," *Digest of Papers, 1975 Int'l. Symp. on Fault-Tolerant Computing*, Paris, France, June 1975, p. 251.
- Kuck, D. J., "Parallel Processing of Ordinary Programs," in *Advances in Computers*, vol. 15, Rubinoff and Yovits, eds., Academic Press, New York, 1976, pp. 119-179.
- Kuck, D. J., "Illiac IV Software and Application Programming," *IEEE Trans. on Comp.* Aug. 1968, pp. 746-757.
- Kuck, D. J., "A Survey of Parallel Machine Organization and Programming," *ACM Computing Surveys*, vol. 9, no. 1, Mar. 1977, pp. 29-59.
- Kuck, D. J., *The Structure of Computers and Computations*, vol. 1, Wiley, New York, 1978.
- Kuck, D. J., Kuhn, R. H., Padua, D. A., Leasure, B., and Wolfe, M., "Dependence Graphs and Compiler Optimizations," *Proc. 8th ACM Symp. Principles Programming Languages*, Jan. 1981, pp. 207-218.
- Kuck, D. J., Lawrie, D. H., and Sameh, A. H., eds. *High Speed Computer and Algorithm Organization*, Academic Press, New York, 1977.
- Kuck, D. J., and Stokes, R. A., "The Burroughs Scientific Processor (BSP)" *IEEE Trans. on Comp.*, C-31, no. 5, May 1982, pp. 363-376.
- Kuhn, R. H., "Optimization and Interconnection Complexity for: Parallel Processors, Single-Stage Networks, and Decision Trees," *Ph.D. Thesis*, Univ. of Ill. at Urb-Champ., Dep. of Computer Science, no. 80-1009, Feb. 1980.
- Kuhn, R. H., and Padua, D. A., eds., *Tutorial on Parallel Processing*, IEEE Computer Society Press, order no. 367, Los Angeles, 1981.
- Kulisch, U. W., and Miranker, W. L., eds., *A New Approach to Scientific Computation*, Academic Press, New York, 1983.
- Kung, H. T., "Synchronized and Asynchronous Parallel Algorithms for Multiprocessors," *Algorithms and Complexity: Recent Results and New Directions*, Traub, ed., Addison-Wesley, 1976.
- Kung, H. T., "The Structure of Parallel Algorithms," *Advances in Computers*, vol. 19, Yovits, ed., Academic Press, New York, 1980, pp. 65-112.
- Kung, H. T., "Why Systolic Architectures," *IEEE Comp.*, Jan. 1982, pp. 37-46.
- Kung, H. T., and Leiserson, C. E., "Systolic Arrays (for VLSI)," *Sparse Matrix Proc.*, Duff, et al., eds., Society of Indust. and Appl. Math., Philadelphia, Pa., 1978, pp. 245-282.
- Kung, S. Y., Arun, K. S., Galezer, R. J., Rao, D. V. B., "Wavefront Array Processor: Language, Architecture, and Applications," *IEEE Trans. on Comp.* C-31, no. 11, Nov. 1982, pp. 1054-1066.
- Kurinckx, A., and Pujolle, G., "Analytic Methods for Multiprocessor Modeling," *4th Int'l. Symp. on Modeling and Performance Evaluation of Computer Systems*, Part II, Vienna, Austria, Feb. 1979.
- Kurtzberg, J. M., "On the Memory Conflict Problem in Multiprocessor Systems," *IEEE Trans. on Comp.*, C-23, no. 3, Mar. 1974, pp. 286-293.

- Lamport, L., "A New Solution of Dijkstra's Concurrent Programming Problem," *Comm. of ACM*, vol. 17, Aug. 1974, pp. 453-454.
- Lamport, L., "The Synchronization of Independent Processes," *Acta Informatica*, vol. 7, no. 1, 1976, pp. 15-34.
- Lamport, L., "Proving the Correctness of Multiprocess Programs," *IEEE Trans. on Soft. Eng.*, SE-3, no. 2, Mar. 1977, pp. 125-143.
- Lampson, B. W., "Dynamic Protection Structures," *1969 Fall Joint Computer Conference*, AFIPS Press, 1969, pp. 27-38.
- Lampson, B. W., "Protection," *Operating Systems Review* 8(1), Jan. 1974.
- Lampson, B. W., and Sturgis, H. E., "Reflections on an Operating System Design," *Comm. of ACM*, vol. 19, May 1976, pp. 251-265.
- Lane, W. G., "Input/Output Processing," *Introduction to Computer Architecture*, Stone, ed., SRA Inc., 1978, pp. 275-316.
- Lang, D. E., Agerwala, T. K., and Chandy, K. M., "A Modeling Approach and Design Tool for Pipelined Central Processors," *Proc. 6th Ann. Symp. on Computer Architecture*, Apr. 1979, pp. 122-129.
- Lang, T., and Stone, H. S., "A Shuffle-Exchange Network with Simplified Control," *IEEE Trans. on Comp.*, C-25, Jan. 1976, pp. 55-56.
- Larson, A. G., "Cost-Effective Processor Design with an Application to Fast Fourier Transform Computers," Ph.D. Thesis, Stanford Univ., 1973.
- Larson, A. G., and Davidson, E. S., "Cost-Effective Design of Special-Purpose Processors: A Fast Fourier Transform Case Study," *Proc. 11th Allerton Conf.*, 1973, pp. 547-557.
- Lawrence Livermore Laboratory, "The S-1 Project: Annual Reports," vol. 1 Architecture, vol. 2 Hardware, and vol. 3 Software, UCID-18619, Univ. of Calif., Livermore, 1979.
- Lawrie, D. H., "Access and Alignment of Data in an Array Processor," *IEEE Trans. on Comp.*, C-24, no. 12, Dec. 1975, pp. 1145-1155.
- Lawrie, D. H., Layman, T., Baer, D., and Randal, J. M., "Glypnir—A Programming Language for ILLIAC IV," *Comm. of ACM*, vol. 18, Mar. 1975, pp. 157-164.
- Lawrie, D. H., and Vora, C. R., "The Prime Memory System for Array Access," *IEEE Trans. on Comp.*, C-31, no. 5, Oct. 1982, pp. 435-442.
- Lee, R. B-L., "Empirical Results on the Speed, Efficiency, Redundancy and Quality of Parallel Computations," *Int'l. Conf. Parallel Proc.*, Aug. 1980, pp. 91-96.
- Levy, H. M., *Capability-Based Computer Systems*, Digital Press, 1983.
- Levy, H. M., and Eckhouse, R. H., Jr., *Computer Programming and Architecture—The Vax-11*, Digital Press, 1980.
- Li, H. F., "Scheduling Trees in Parallel Pipelined Processing Environments," *IEEE Trans. on Comp.*, Nov. 1977, pp. 1101-1112.
- Lincoln, N. R., "Technology and Design Trade Offs in the Creation of a Modern Supercomputer," *IEEE Trans. on Comp.*, C-31, no. 5, May 1982, pp. 363-376.
- Lint, B., and Agerwala, T., "Communication Issues in the Design and Analysis of Parallel Algorithms," *IEEE Trans. on Soft. Eng.*, SE-7, no. 2, Mar. 1981, pp. 174-188.
- Lipovski, G. J., and Malek, M., "A Theory for Multicomputer Interconnection Networks," *Tech. Report TRAC-40*, Univ. of Texas, Austin, Mar. 1981.
- Lipovski, G. J., and Tripathi, A., "A Reconfigurable Varistructured Array Processor," *Proc. 1977 Int'l. Conf. on Parallel Proc.*, 1977, pp. 165-174.
- Liptay, J. S., "Structural Aspects of System 360/85: The Cache," *IBM Systems Journal*, 7, 1969, pp. 15-21.
- Liu, J. W. S., and Liu, C. L., "Bounds on Scheduling Algorithms for Heterogeneous Computing Systems," *Proc. IFIP Congress* 74, 1974, pp. 349-353.
- Liu, J. W. S., and Liu, C. L., "Performance Analysis of Multiprocessor Systems Containing Functionally Dedicated Processors," *Acta Informatica*, vol. 10, no. 1, 1978, pp. 95-104.
- Loomis, H. H., "The Maximum Rate Accumulator," *IEEE Trans. on Comp.*, vol. EC-15, no. 4, Aug. 1966, pp. 628-639.
- Lotin, H. (1972). *Parallelism in Hardware and Software*, Prentice-Hall, Englewood Cliffs, N.J., 1972.
- Madnick, S. E., and Donovan, J. J., *Operating Systems*, McGraw-Hill, New York, 1974.

- Majithia, J. C., "Cellular Array for Extraction of Squares and Square Roots of Binary Numbers," *IEEE Trans. on Comp.*, C-20, no. 12, Dec. 1970, pp. 1617-1618.
- Marathe, M., and Fuller, S. H., "A Study of Multiprocessor Contention for Shared Data in C.mmp," *ACM SIGMETRICS Conf.*, Washington, D.C., Dec. 1977.
- Matick, R. E., *Computer Storage Systems and Technology*, Wiley, New York, 1977.
- Matick, R. E., "Memory and Storage," *Introduction to Computer Architecture*, Stone, ed., SRA Inc., 1980, pp. 205-274.
- Mattson, R. L., Gecsei, J., Slutze, D. R., and Traiger, I. L., "Evaluation Techniques for Storage Hierarchies," *IBM Systems Journ.*, 9, 1970, 78-117.
- Mazare, G., "Multiprocessor Systems," *Proc. 1974 CERN School of Computing*, Godysund, Norway, Aug. 1974.
- McGraw, J. R., "Data Flow Computing—Software Development," *IEEE Trans. on Computers*, Dec. 1980, pp. 1095-1103.
- Mead, C., and Conway, L., *Introduction to VLSI Systems*, Addison-Wesley, Mass., 1980.
- Miranker, G. S., "Implementation of Procedures on a Class of Data Flow Processors," *Proc. Int'l. Conf. Parallel Proc.*, IEEE no. 77CH 1253-4C, 1977, pp. 77-86.
- Miura, K., and Uchida, K., "FACOM Vector Processor VP-100/VP-200," *Proc. NATO Advanced Research Workshop on High-Speed Computing*, Jülich, W. Germany, Springer-Verlag, June 20-22, 1983.
- Moldovan, D. I., "On the Design of Algorithms for VLSI Systolic Array," *Proc. IEEE*, Jan. 1983, pp. 113-120.
- Moto-oka, T., "Overview to the Fifth Generation Computer System Project," *Proc. 10th Ann. Symp. Computer Architecture*, June 1983, pp. 417-422.
- Moto-oka, T., and Fuchi, K., "The Architectures in the Fifth Generation Computers," *Proc. 1983 IFIP Congress*, North-Holland, Amsterdam, 1983, pp. 589-602.
- Mrosousky, I., Wong, J. Y., and Lampe, H. W., "Construction of a Large Field Simulator on a Vector Computer," *Journal of Petroleum Tech.*, Dec. 1980, pp. 2253-2264.
- Mueller, P. T., Siegel, L. J., and Siegel, H. T., "Parallel Algorithms for the Two-dimensional FFT," *Proc. 5th Int'l. Conf. on Pattern Recog. and Image Proc.*, Dec. 1980, pp. 497-502.
- Muntz, R. R., and Coffman, E. G., "Optimal Preemptive Scheduling on Two Processor Systems," *IEEE Trans. on Comp.*, C-18, Nov. 1969, pp. 1014-1020.
- Muraoka, Y., "Parallelism Exposure and Exploitation in Programs," Ph.D. Thesis, Univ. of Ill. at Urb.-Champ., Dept. of Computer Science 71-424, Feb. 1971.
- Myers, G. J., *Advances in Computer Architecture*, Wiley, New York, 1978.
- Nassimi, D., and Sahni, S. H., "Data Broadcasting in SIMD Computers," *Proc. Int'l. Conf. Parallel Proc.*, Aug. 1980, pp. 325-326.
- Nessett, D. M., "The Effectiveness of Cache Memories in a Multiprocessor Environment," *Australian Computer Journ.*, vol. 7, no. 1, Mar. 1975, pp. 33-38.
- Newton, G., "Deadlock Prevention, Detection and Resolution: An Annotated Bibliography," *ACM Operating Sys. Review*, vol. 13, no. 2, Apr. 1979, pp. 33-44.
- Newton, R. S., "An Exercise in Multiprocessor Operating System Design," *Agard Conf. Proc. No. 149 on Real-Time Computer-based Systems*, NATO Advisory Group on Aerospace R & D, Athens, Greece, May 1974.
- Ni, L. M., "Performance Optimization of Parallel Processing Computer Systems," Ph.D. Thesis, School of Electrical Engineering, Purdue Univ., Ind., Dec. 1980.
- Ni, L. M., and Hwang, K., "Performance Modeling of Shared Resource Array Processors," *IEEE Trans. on Soft. Eng.*, SE-7, no. 4, July 1981, pp. 386-394.
- Ni, L. M., and Hwang, K., "Vector Reduction Methods for Arithmetic Pipeline," *Proc. 6th Symp. on Computer Arithmetic*, June 20-22, 1983, pp. 144-150.
- Nolen, J. S., Kuba, D. W., and Kasic, M. J. Jr., "Application of Vector Processors to the Solution of Finite Difference Equations," *AIIM 5th Symp. Reservoir Simulation*, Feb. 1979, pp. 37-44.
- Nutt, G. J., "A Parallel Processor Operating System," *IEEE Trans. on Soft. Eng.*, SE-3, no. 6, Nov. 1977a, pp. 467-475.

- Nutt, G. J., "Memory and Bus Conflict in an Array Processor," *IEEE Trans. on Comp.*, June 1977b, pp. 514-521.
- Oleinick, P. N., *The Implementation and Evaluation of Parallel Algorithms on C.mmp*, Ph.D. Dissertation, Carnegie-Mellon Univ., 1978.
- Oleinick, P. H., and Fuller, S. H., "The Implementation and Evaluation of a Parallel Algorithm on C.mmp," *Technical Report*, Carnegie-Mellon Univ. Computer Science Dept., Dec. 1977.
- Orcutt, S. E., "Computer Organization and Algorithms for Very High-Speed Computations," *Ph.D. Thesis*, Stanford University, Calif., 1974.
- Ousterhout, J. K., "Partitioning and Cooperation in a Distributed Multiprocessor Operating System: Medusa," *Ph.D. Thesis*, Carnegie-Mellon Univ., April 1980.
- Owen, G. J., "Rollback—A Method of Process and System Recovery," *Proc. Conf. on Soft. Eng. for Telecommunication Switching Systems*, Colchester, England, Apr. 1973.
- Owicki, S., and Gries, D., "Verifying Properties of Parallel Programs: An Axiomatic Approach," *Comm. of ACM*, vol. 19, 5, May 1976, pp. 279-285.
- Padua, D. A., Kuck, D. J., and Lawrie, D. H., "High-Speed Multiprocessors and Compilation Techniques," *IEEE Trans. on Comp.*, C-29, Sept. 1980, pp. 763-776.
- Panda, D. A., Kuck, D. J., and Lawrie, D. H., "High-Speed Multiprocessors and Compiling Techniques," *IEEE Trans. on Comp.*, Sept. 1980, pp. 763-776.
- Parasuraman, B., "Pipelined Architectures for Microprocessor," *COMPCON Proc.*, 1976, pp. 225-228.
- Parnas, D. L., "On the Criteria to Be Used in Decomposing Systems into Modules," *Comm. of ACM*, vol. 15, Dec. 1972.
- Patel, J. H., "Improving the Throughput of Pipelines with Delays and Buffers," *Ph.D. Thesis*, University of Illinois at Urb.-Champ., 1976.
- Patel, J. H., "Pipelines with Internal Buffers," *Proc. 5th Ann. Symp. on Computer Architecture*, Apr. 1978, pp. 249-254.
- Patel, J. H., "Performance of Processor-Memory Interconnections for Multiprocessors," *IEEE Trans. on Comp.*, Oct. 1981, pp. 771-780.
- Paul, G., "Large-Scale Vector/Array Processors," *IBM Research Report*, RC 7306, Sept. 1978 (24 pages).
- Paul, G., and Wilson, M. W., *The VECTRAN Language: An Experimental Language for Vector/Matrix Array Processing*, IBM Palo Alto Scientific Center Report 6320-3334, Aug. 1975.
- Pearce, R. C., and Majithia, J. C., "Analysis of a Shared Resource MIMD Computer Organization," *IEEE Trans. on Comp.*, C-27, no. 1, Jan. 1978, pp. 64-67.
- Pease, M. C., "An Adaptation of the Fast Fourier Transform for Parallel Processing," *Journ. of ACM*, vol. 15, Apr. 1968, pp. 252-264.
- Pease, M. C., "The Indirect Binary n-cube Microprocessor Array," *IEEE Trans. on Comp.*, C-25, May 1977, pp. 458-473.
- Perrott, R. H., "A Language for Array and Vector Processors," *ACM Trans. on Programming Languages and Systems*, vol. 1, no. 2, Oct. 1979, pp. 177-195.
- Peterson, J. L., "Petri Nets," *ACM Computing Surveys*, 3028: Sept. 1977, pp. 223-252.
- Pradhan, D. K., and Kodandapani, K. L., "A Uniform Representation of Single- and Multistage Interconnection Networks Used in SIMD Machines," *IEEE Trans. on Comp.*, Sept. 1980, pp. 777-790.
- Prasad, N. S., *Architecture and Implementation of Large Scale IBM Computer Systems*, Q.E.D. Information Sciences, Inc., Wellesley, Mass., 1981.
- Preparata, F. P., "Parallelism in Sorting," *Proc. 1977 Int'l. Conf. on Parallel Proc.*, Detroit, Mich., Aug. 1977, pp. 202-206.
- Preparata, F. P., and Vuillemin, J. E., "The Cube-Connected Cycles: A Versatile Network for Parallel Computation," *Proc. 20th Symp. Foundations of Computer Science*, 1979, pp. 140-147.
- Preston, K., Duff, M. J. B., Levialdi, D. S., Norgren, P. E., and Toriwaki, J. I., "Basics of Cellular Logic With Some Applications in Medical Image Processing," *Proc. IEEE*, May 1979, pp. 826-856.
- Prieve, B.B., and Fabry, R. S., "VMIN—An Optimal Variable-Space Page Replacement Algorithm," *Comm. of ACM*, vol. 19, May 1976, 295-297.

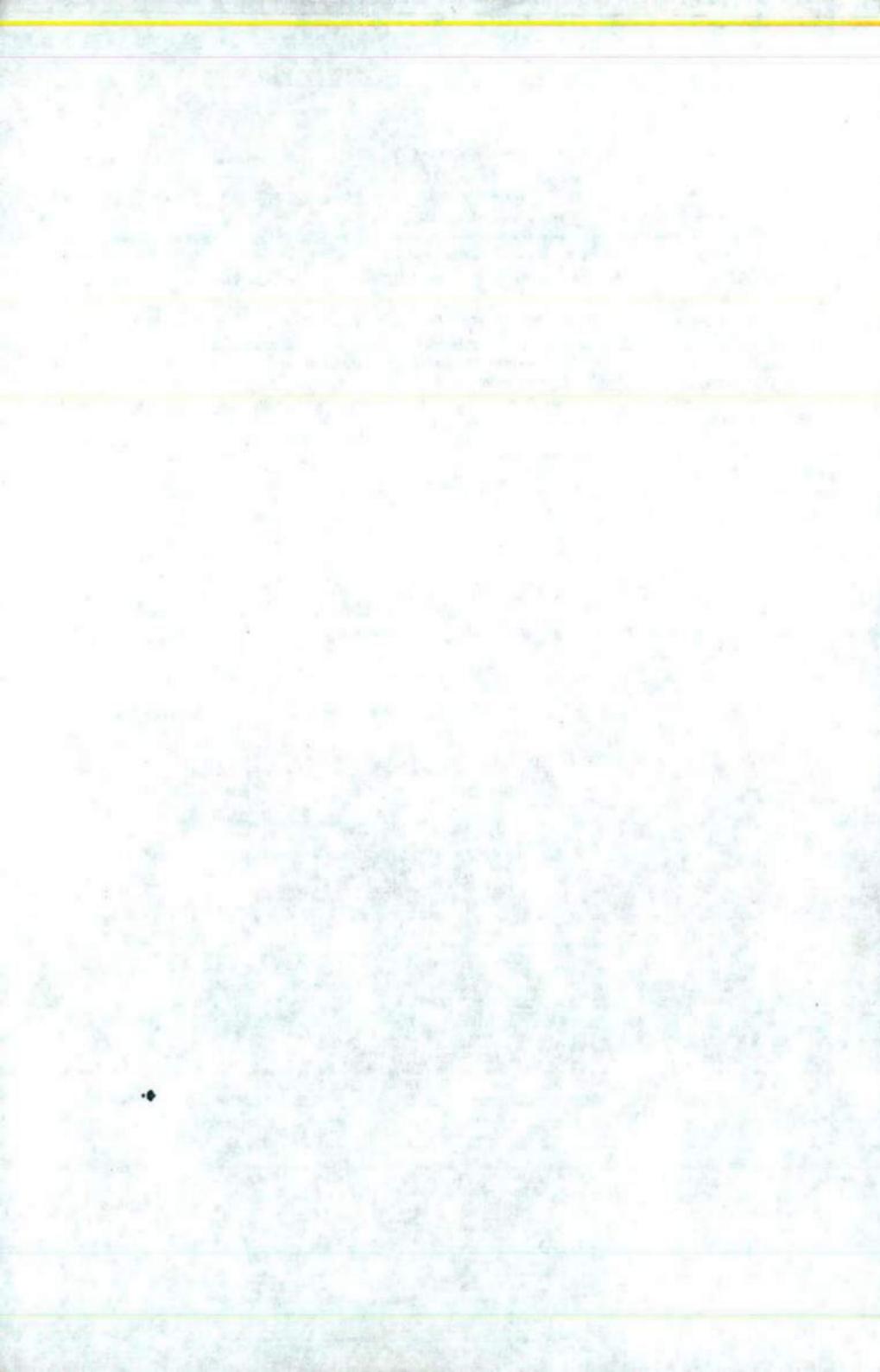
- Purcell, C. J., "The Control Data STAR-100—Performance Measurements," *AFIPS NCC Proc.*, 1974, pp. 385-387.
- Radoy, C. H., and Lipovski, G. J., "Switched Multiple Instruction Multiple Data Stream Processing," *Proc. 2d Ann. Symp. Computer Architecture*, 1974, pp. 183-187.
- Ramamoorthy, C. V., Chandy, K. M., and Gonzalez, M. J., "Optimal Scheduling Strategies in a Multiprocessor System," *IEEE Trans. on Comp.*, C-21, 2, Feb. 1972, pp. 137-146.
- Ramamoorthy, C. V., and Gonzalez, M. J., "Recognition and Representation of Parallel Processable Streams in Computer Programs. II (Task/Process Parallelism)," *Proc. ACM 24th Nat. Conf.*, ACM, New York, 1969, 387-397.
- Ramamoorthy, C. V., and Kim, K. H., "Pipelining—The Generalized Concept and Sequencing Strategies," *NCC Proc.*, AFIPS Press, 1974, pp. 289-97.
- Ramamoorthy, C. V., and Li, H. F., "Sequencing Control in Multifunctional Pipeline Systems," *Proc. 1975 Sagamore Comp. Conf. on Parallel Proc.*, 1975, pp. 79-89.
- Ramamoorthy, C. V., and Li, H. F., "Pipeline Architecture," *ACM Computing Surveys*, vol. 9, no. 1, Mar. 1977, pp. 61-102.
- Rao, G. S., "Performance Analysis of Cache Memories," *Journ. of Assoc. of Comp. Mach.*, vol. 25, no. 3, 1978, pp. 378-395.
- Rau, B. R., and Rossman, G. E., "The Effect of Instruction Fetch Strategies upon the Performance of Pipelined Instruction Units," *Proc. 4th Ann. Symp. Computer Architecture*, IEEE 77CH 1182-5C, 1977, pp. 80-89.
- Raw, B. R., "Program Behavior and the Performance of Interleaved Memories," *IEEE Trans. on Comp.*, C-28, no. 3, Mar. 1979, pp. 191-199.
- Reilly, J., Sutton, A., Nasser, R., and Griscom, R., "Processor Controller for the IBM 3081," *IBM Journ. of Res. and Dev.*, vol. 26, no. 1, Jan., pp. 22-29.
- Rice, J., *Matrix Computations and Mathematical Software*, McGraw-Hill, New York, 1981.
- Ritchie, D. M., and Thompson, K., "The UNIX Time Sharing System," *Comm. of ACM*, vol. 17, July 1974, pp. 365-375.
- Robinson, J. T., "Some Analysis Techniques for Asynchronous Multiprocessor Algorithms," *IEEE Trans. on Soft. Eng.*, Jan. 1979, pp. 24-30.
- Rodrique, G., ed., *Parallel Computations*, Academic Press, New York, 1982.
- Rodrique, G., Giroux, E. D., and Pratt, M., "Perspective on Large-Scale Scientific Computations," *IEEE Comp.*, Oct. 1980, pp. 65-80.
- Roesser, R. P., "Two-Dimensional Microprocessor Pipelines for Image Processing," *IEEE Trans. on Comp.*, Feb. 1978, pp. 144-156.
- Rohrbacher, D., and Potter, J. L., "Image Processing with STARAN Parallel Computer," *IEEE Comp.*, Aug., pp. 54-59.
- Rosene, A. F., "Memory Allocation for Multiprocessors," *IEEE Trans. on Electronic Computers*, vol. 16, no. 5, Oct. 1967, pp. 659-665.
- Rumbaugh, J., "A Data Flow Multiprocessor," *IEEE Trans. on Comp.*, C-26, no. 2, Feb. 1977, pp. 138-146.
- Russell, E. C., "Automatic Program Analysis," *Ph.D. Thesis*, Dep. of Electrical Engineering, Univ. of Calif., Los Angeles, 1969.
- Russell, R. M., "The Cray-1 Computer System," *Comm. of ACM*, Jan. 1978, pp. 63-72.
- Saltzer, J. H., "A Simple Linear Model of Demand Paging Performance," *Comm. of ACM*, vol. 17, April 1974.
- Saltzer, J. H., and Schroeder, M. D., "The Protection of Information in Computer Systems," *Proc. IEEE*, Sept. 1975, pp. 1238-1308.
- Sameh, A. H., "Numerical Parallel Algorithms—A Survey," *High-Speed Computers and Algorithm Organization*, Kuck, et al., eds., Academic Press, 1977, pp. 207-228.
- Sastry, K. V., and Kain, R. Y., "On the Performance of Certain Multiprocessor Computer Organizations," *IEEE Trans. on Comp.*, vol. C-24, no. 11, Nov. 1975, pp. 1066-1074.
- Satyanarayanan, M., *Multiprocessors: A Comparative Study*, Prentice-Hall, Englewood Cliffs, N.J., 1980.

- Schaefer, D. H., "Spatially Parallel Architectures: An Overview," *Computer Design*, Aug. 1982, pp. 117-124.
- Schmid, H. A., "On the Efficient Implementation of Conditional Critical Regions and the Construction of Monitors," *Acta Informatica* 6, Springer-Verlag, 1976, pp. 227-249.
- Schwartz, J. T., "Ultra-Computers," *ACM Trans. Programming Languages and Systems*, vol. 2, no. 4, 1980, pp. 484-521.
- Senzig, D. N., and Smith, R. V., "Computer Organization for Array Processing," *AFIPS FJCC Proc. (part I)*, 1965, pp. 117-128.
- Sethi, A. S., and Deo, N., "Interference in Multiprocessor Systems with Localized Memory Access Probabilities," *IEEE Trans. on Comp.*, vol. C-28, no. 2, Feb. 1979.
- Shapiro, H. D., "A Comparison of Various Methods for Detecting and Utilizing Parallelism in a Single Instruction Stream," *Proc. 1977 Int'l. Conf. Parallel Proc.*, IEEE No. 77CH 1253-4C, 1977, pp. 67-76.
- Shar, L. E., "Design and Scheduling of Statistically Configured Pipelines," *Digital Systems*, Lab Report SU-SEL-72-042, Stanford University, Stanford, Calif., Sept. 1972.
- Shar, L. E., and Davidson, E. S., "A Multiminicomputer System Implemented Through Pipelining," *IEEE Comp.*, Feb. 1975, pp. 42-51.
- Shen, J. P., and Hayes, J. P., "Fault Tolerance of a Class of Connecting Networks," *Proc. 7th Symp. Computer Architecture*, 1980, pp. 61-71.
- Shoshani, A., and Coffman, E. G., Jr., "Sequencing Tasks in Multiprocess, Multiple Resource Systems to Avoid Deadlocks," *Proc. 11th Ann. Symp. Switching and Automata Theory*, Oct. 1970, pp. 225-233.
- Siegel, H. J., "A Model of SIMD Machines and a Comparison of Various Interconnection Networks," *IEEE Trans. on Comp.*, vol. C-28, no. 12, Dec. 1979a, pp. 907-917.
- Siegel, H. J., "Interconnection Networks for SIMD Machines," *IEEE Comp.*, June 1979b, pp. 57-65.
- Siegel, H. J., "The Theory Underlying the Partitioning of Permutation Networks," *IEEE Trans. on Comp.*, vol. C-29, no. 9, Sept. 1980, pp. 791-800.
- Siegel, H. J., *Interconnection Networks for Large-Scale Parallel Processing: Theory and Case Studies*, Lexington Books, Lexington, Mass., 1984.
- Siewiorek, D. P., et al., "A Case Study of C.mmp, Cm\* and C.vmp, Part I: Experience with Fault-Tolerance in Multiprocessor Systems," *Proc. IEEE*, vol. 66, no. 10, Oct. 1978, pp. 1178-1199.
- Siewiorek, D. P., Bell, C. G., and Newell, A., *Principles of Computer Structures*, McGraw-Hill, New York, 1980.
- Sites, R. L., "Operating Systems and Computer Architecture," in *Introduction to Computer Architecture* (Stone, ed.), SRA Inc., 1980, pp. 591-643.
- Slotnick, D. L., "Unconventional Systems," *Computer Design*, Dec. 1982, pp. 49-52.
- Slotnick, D. L., Borck, W. C., and McReynolds, R. C., "The SOLOMON Computer," *Proc. of AFIPS Fall Joint Comp. Conf.*, Wash. D.C., 1962, pp. 97-107.
- Smith, A. J., "A Modified Working-Set Paging Algorithm," *IEEE Trans. on Comp.*, C-29, Sept. 1976, 907-914.
- Smith, A. J., "Multiprocessor Memory Organization and Memory Interference," *Comm. of ACM*, vol. 20, no. 10, Oct. 1977, pp. 754-761.
- Smith, A. J., "A Comparative Study of Set-Associative Memory Mapping Algorithms and Their use for Cache and Main Memory," *IEEE Trans. Soft. Eng.*, vol. SE-4, March 1978, pp. 121-130.
- Smith, A. J., "Cache Memories," *ACM Computing Surveys*, vol. 14, no. 3, Sept. 1982, pp. 473-530.
- Smith, B. J., "A Pipelined Shared Resources MIMD Computer," *Proc. 1978 Int'l. Conf. on Parallel Proc.*, 1978, pp. 6-8.
- Smith, B. J., "Architecture and Applications of the HEP Multiprocessor Computer System," *Real Time Signal Processing IV*, vol. 298, Aug. 1981.
- Smith, J. W., "Cooperation and Competition: An Approach to Parallel Computation," *Proceedings of Southeastcon 1979*, Roanoke, Virg., Apr. 1979.
- Snyder, L., "Introduction to the Configurable Highly Parallel Computer," *IEEE Comp.*, Jan. 1982, pp. 47-64.

- Sperry Univac., *The Univac Series 1100 Announcement*, May 1982..
- Steele, G. L., "Multiprocessing Compactifying Garbage Collection," *Comm. of ACM*, vol. 18, no. 9, Sept. 1975, pp. 495-508.
- Stephenson, C. M., "Control of a Variable Configuration Pipelined Arithmetic Unit," *Proc. 11th Allerton Conf.*, Oct. 1973, pp. 558-567.
- Stevens, K., "CFD—A FORTRAN-like Language for the Illiac IV," *SIGPLAN Notices*, March 1975, pp. 72-80.
- Stevenson, D. K., "Numerical Algorithms for Parallel Computers," *Proc. Nat'l. Computer Conf.*, AFIPS Press, vol. 49, 1980, pp. 357-361.
- Stokes, R. A., "Burroughs Scientific Processor," in *High Speed Computer and Algorithm Organization* (Kuck, et al., eds.) Academic Press, New York, 1977, pp. 85-89.
- Stone, H. S., "Parallel Processing with a Perfect Shuffle," *IEEE Trans. on Comp.*, vol. C-20, Feb. 1971, pp. 153-161.
- Stone, H. S., "An Efficient Parallel Algorithm for the Solution of a Tridiagonal Linear System of Equations," *Journ. of ACM*, vol. 20, 1973, pp. 27-38.
- Stone, H. S., "Multiprocessor Scheduling with the Aid of Network Flow Algorithms," *IEEE Trans. on Soft. Eng.*, vol. SE-5, no. 1, Jan. 1977, pp. 85-93.
- Stone, H. S., "Sorting on STAR," *IEEE Trans. on Comp.*, March 1978, pp. 138-46.
- Stone, H. S., "Parallel Computers," Chap. 8 in *Introduction to Computer Architecture* (Stone, ed.), SRA, 1980, pp. 363-426.
- Stout, Q. F., "Sorting, Merging, Selecting, and Filtering on Tree and Pyramid Machines," *Proc. 1983 Int'l. Conf. Parallel Processing*, 1983, pp. 214-221.
- Strecker, W., "Cache Memories for PDP-11 Family Computers," *Proc. 3rd Symp. on Comp. Arch.*, 1976, 155-157.
- Su, S. P., "Pipelining and Dataflow Techniques for Designing Supercomputers," *Ph.D. Thesis*, School of E.E., Purdue University, Dec. 1982.
- Sugarman, R., "Superpower Computers," *IEEE Spectrum*, Apr. 1980, pp. 28-34.
- Sutherland, I. E., and Mead, C. A., "Microelectronics and Computer Science," *Scientific American*, vol. 237, 1977, pp. 210-229.
- Swan, R. J., Bechtholsheim, A., Lai, K. W., and Ousterhout, J. K., "The Implementation of the CM\* Multimicroprocessor," *Proc. AFIPS 1977 Nat. Comp. Conf.*, 46, AFIPS Press, Montvale, N.J., 1977, pp. 645-655.
- Syre, J. C., Comte, D., and Hifdi, N., "Pipelining, Parallelism and Asynchronism in the LAU System," *Proc. 1977 Int. Conf. on Parallel Processing*, 1977, pp. 87-92.
- Syre, J. C., et al., "The Data Driven LAU Multiprocessor System: Results and Perspectives," in *Information Processing 80* (Lavington, S. H., ed.), North Holland, New York, 1980.
- Takahashi, N., and Amamiya, M., "A Dataflow Processor Array System: Design and Analysis," *Proc. of the 10th Int'l. Symp. on Computer Architecture*, June 13-17, 1983, pp. 243-251.
- Tanenbaum, A., "Implication of Structured Programming for Computer Architecture," *Comm. of ACM*, 21, Mar. 1978, pp. 237-246.
- Tang, C. K., "Cache System Design in the Tightly Coupled Multiprocessor System," *Proc. AFIPS 1976 Nat. Comp. Conf.*, 45, AFIPS Press, Montvale, N.J., 1976, pp. 749-753.
- Tanimoto, S. L., "A Pyramidal Approach to Parallel Processing," *Proc. 10th Annual Symp. Computer Architecture*, Sweden, 1983, pp. 372-378.
- Tannenbaum, A. S., *Structured Computer Organization*, Prentice-Hall, Englewood Cliffs, N.J., 1976.
- Tesler, L. G., and Enea, H., "A Language for Concurrent Processes," *Proc. SJCC*, AFIPS Press, 1968.
- Texas Instruments, Inc., "Description of the ASC System: Parts I to S, Manual Nos. 934662 to 934666, 1971.
- Texas Instruments, Inc., *ASC FORTRAN Reference Manual*, Pub. No. 930044, 1972.
- Theis, D. J., "Special Tutorial: Vector Supercomputers," *IEEE Comp.*, Apr. 1974, pp. 52-61.
- Thomas, A. T., and Davidson, E. S., "Scheduling of Multiconfigurable Pipelines," *Proc. 12th Allerton Conf.*, Univ. of Illinois, Urbana, 1974, pp. 658-69.
- Thomas, R. E., "A Dataflow Architecture with Improved Asymptotic Performance," *Ph.D. Thesis*, Dept. of Computer Science, Univ. of Calif., Irvine, Apr. 1981.

- Thompson, C. D., "Generalized Connection Networks for Parallel Processor Intercommunication," *IEEE Trans. Comp.*, vol. C-27, no. 12, Dec. 1978, pp. 1119-1126.
- Thompson, C. D., and Kung, H. T., "Sorting on a Mesh-Connected Parallel Computer," *Comm. of ACM*, vol. 20, no. 4, Apr. 1977, pp. 263-271.
- Thompson, S. D., "A Complexity Theory for VLSI," *Ph.D. Thesis*, Dept. of Computer Science, Carnegie-Mellon University, Pittsburgh, Penn., Sept. 1980.
- Thornton, J. E., *Design of a Computer, the Control Data 6600*, Scott, Foresman and Co., Glenview, Ill., 1970.
- Thurber, K. J., *Large Scale Computer Architecture—Parallel and Associative Processors*, Hayden Book Co., N.J., 1976.
- Thurber, K. J., "Parallel Processor Architectures—Part I: General Purpose System," *Computer Design*, Jan. 1979a, pp. 89-97.
- Thurber, K. J., "Parallel Processor Architectures—Part II: Special Purpose Systems," *Computer Design*, Feb., 1979b, pp. 103-114.
- Thurber, K. J., and Masson, G. M., *Distributed Processor Communication Architecture*, Lexington Books, Lexington, Mass., 1979.
- Thurber, K. J., and Wald, L. D., "Associative and Parallel Processors," *ACM Computing Surveys*, vol. 7, Dec. 1975, pp. 215-255.
- Tjaden, G. S., and Flynn, M. J., "Representation of Concurrency with Ordering Matrices," *IEEE Trans. on Comp.*, vol. C-22, no. 8, Aug. 1973, pp. 752-761.
- Tokoro, M., "On the Working Set Concept for Dataflow Machine," *Proc. of 10th Ann. Symp. Computer Architecture*, June 1983, pp. 90-97.
- Tomasulo, R. M., "An Efficient Algorithm for Exploiting Multiple Arithmetic Units," *IBM Journ. of Res. and Dev.*, vol. 11, no. 1, Jan. 1967, pp. 25-33.
- Treleaven, P. C., "Exploiting Program Concurrency in Computing Systems," *IEEE Comp.*, 12, Jan. 1979, pp. 42-50.
- Treleaven, P. C., Brownbridge, D. R., and Hopkins, R. P., "Data Driven and Demand-Driven Computer Architecture," *ACM Computing Surveys*, March 1982, pp. 93-144.
- Ullman, J. D., *Computational Aspects of VLSI*, Computer Science Press, Rockville, Md., 1984.
- Uhr, L., *Algorithm-Structured Computer Arrays and Networks*, Academic Press, New York, 1984.
- Vick, C. R., and Merwin, R. E., "An Architecture Description of a Parallel Processing Element," *Proc. Int'l Workshop on Computer Architecture*, 1973.
- Walker, L. L., "Multiprocessor Operating System Design," in *Operating Systems, International Computer State of the Art Report*, Infotech Ltd., Maidenhead, England, 1972.
- Waser, S., and Flynn, M. T., *Introduction to Arithmetic for Digital Systems Designers*, Holt, Rinehart and Winston, New York, 1982.
- Watson, R. W., *Timesharing System Design Concepts*, McGraw-Hill, New York, 1970.
- Watson, W. J., "The TI ASC—A Highly Modular and Flexible Super Computer Architecture," *Proc. AFIPS Fall Joint Computer Conf.*, AFIPS Press, Montvale, N.J., 1972, pp. 221-228.
- Watson, W. J., and Carr, H. M., "Operational Experiences with the TI Advanced Scientific Computer," *AFIPS NCC Proc.*, 1974, pp. 389-97.
- Weckes, S., "A Design for a Multiple Processor Operating Environment," *Digest of Papers, COMPCON 73*, San Francisco, Calif., March 1973, pp. 143-146.
- White, C. H. (ed.), *Multiprocessor Systems, International Computer State of the Art Report*, Infotech Ltd., Maidenhead, England, 1976.
- Widdoes, L. C., Jr., "The S-1 Project: Developing High-Performance Digital Computers," *Digest of Papers: IEEE Compon 80*, Spring 1980, pp. 282-291.
- Wilkes, M. V., *Time-Sharing Computer System*, 2d ed., Elsevier, New York, 1972.
- Wittmayer, W. R., "Array Processor Provides High Throughput Rates," *Computer Design*, March 1978, pp. 93-100.
- Wu, C. L., and Feng, T. Y., "Fault Diagnosis for a Class of Multistage Interconnection Networks," *Proc. 1979 Int'l. Conf. Parallel Processing*, 1979, pp. 269-278.
- Wu, C. L., and Feng, T. Y., "On a Class of Multistage Interconnection Networks," *IEEE Trans. on Comp.*, vol. C-29, no. 8, Aug. 1980, pp. 694-702.

- Wu, C. L., and Feng, T. Y., "Universality of the Shuffle Exchange Network," *IEEE Trans. on Computers*, vol. C-30, no. 5, May 1981, pp. 324-331.
- Wulf, W. A., and Bell, C. G., "C.mmp—A Multi-miniprocessor," *Proc. AFIPS Fall Joint Computer Conference*, vol. 41, AFIPS Press, Montvale, N.J., 1972, pp. 765-777.
- Wulf, W. A., et al., "Overview of the Hydra Operating System," in *Proc. of the 5th Symp. on Operating System Principles*, ACM, Nov. 1975, Austin, pp. 122-131.
- Wulf, W. A., Levin, R., and Harbison, S. P., *HYDRA/C.mmp: An Experimental Computer System*, McGraw-Hill, N.Y., 1981.
- Yau, S. S., and Fung, H. S., "Associative Processor Architecture—A Survey," *ACM Computing Surveys*, March 1977, vol. 9, no. 1, pp. 3-28.
- Yeh, P. C., "Shared Cache Organization for Multiple-Stream Computer Systems," Coordinated Science Lab., Univ. of Ill., Tech. Rep. R-904, Jan. 1981.
- Yeh, P. C., Patel, J. H., and Davidson, E. S., "Shared Cache for Multiple Stream Computer Systems," *IEEE Trans. on Comp.*, vol. C-32, no. 1, Jan. 1983, pp. 38-47.



---

## INDEX

- Access, privileged, 584  
Access conflict (*see* Conflict, memory)  
Access matrix, 587  
Access network, 53  
Access privileges, 69  
Access time, 13, 53, 56-57  
Accumulator register (ACAR), 401, 409  
Ackerman, W. B., 807  
Acknowledge signal, 484-489  
Activity store, 31  
Actus, 301, 441-444, 454  
Adder, 12, 170  
Address:  
  local, 330, 463  
  physical, 479  
  vector, 215  
Address mapping (*see* Mapping, address)  
Address offset, 415  
Address pipe, 270  
Address register, 328  
Address-save register, 268  
Address space, 61  
Address trace, 82  
Address translation process, 70, 72-73  
Addressing:  
  cache, 111-112  
  interleaved, 58-60, 101  
  virtual (*see* Virtual addressing)  
Addressing fault, 62  
Advance instruction station (ADVAST), 402  
Aerodynamics simulation, 44-45  
Age registers, 116  
Agerwala, T., 551  
Ahuja, S. R., 551  
Algol, 3, 355, 440, 544  
Algorithm:  
  decomposition of, 453  
  MIMD, 613-616  
  partitioned, 790-803  
  SIMD, 325-388, 453, 545, 614, 616-628  
  synchronized, 614, 616-622  
Algorithm restructuring, 545  
Alignment network, 327, 412, 413  
Always prefetch, 113  
Amamiya, M., 760, 808  
Amber Operating System, 668  
Amdahl 470/V6, 77, 111, 234  
Amdahl 470/V7, 111  
Amdahl 470/V8, 111, 113, 115, 580  
Amdahl 580, 113  
Anderson, D. W., 229  
Andrews, G. R., 551  
Anticipatory fetch, 113  
AP-120B, 154, 196, 235, 249-258, 319  
AP-190L, 258  
APEX mode, 255, 494, 495  
Arbitration network, 749, 753  
Arithmetic and logic unit (ALU), 9, 170, 326  
Arithmetic control unit, 381  
Arithmetic controller, 261  
Arithmetic element (AE), 411-417  
Arithmetic pipeline, 164-181, 240, 243,  
  798-801  
Arithmetic unit (AU), 243  
ARPA network, 400, 402  
Array:  
  expression statement, 417  
  sorting of, 361-367  
Array control unit (ACU), 326-327, 424, 426,  
  428  
Array pipeline, 181-187  
Array processor (*see* SIMD computers)  
Artificial intelligence, 45, 375, 530  
Arvind's dataflow machine, 745, 757-759,  
  807-808  
Ascending sort, 386  
ASCII (American Standards Committee on  
Information Interchange), 119  
Assignment decision, 590  
Associative array processing, 374-388  
Associative mapping, 64  
Associative memory (AM), 25, 57-58, 64,  
  374-380, 385  
Associative processor, 25, 325, 375, 380-385,  
  393-396  
Astrophysics, 43  
Asymmetry in multiprocessors, 471  
Asynchronous algorithm, 614, 622-628  
Asynchronous communication, 332  
Asynchronous parallelism, 20  
Asynchronous variables, 680  
Attached processor, 235-237, 249-264,  
  327-328  
Attached Support Processor System (IBM), 460

- Attention signal, 482  
 Automation, 45
- Back-end computer database machine, 12, 235, 327–328  
 Backus, J., 807  
 Baer, J. L., 49, 141, 551, 552  
 Bain, W. L., 551  
 Band matrix multiplication, 772  
 Bandwidth, 414, 416, 460, 483, 490, 502–510, 546, 550  
 balancing, 16  
 interconnection network, 374  
 memory, 156, 163  
 Banyan network, 494, 497, 551  
 Barrell shifter, 345–347  
 Base address, global, 330  
 Baseline network, 336–337, 373  
 Baskett, F., 321  
 Batch processing, 3, 6, 16  
 Batcher, K. E., 363, 364, 388, 454  
 BCC-500, 530  
 BCD (binary-coded decimal) arithmetic, 239, 281  
 Belady's lifetime function model, 84–85  
 Belady's optimal algorithm (MIN)  
 replacement, 91–92  
 Bell Laboratories, 381  
 Benes network, 337  
 Bensoussan, A., 141  
 Bernstein condition, 543, 552  
 Best fit memory placement, 75  
 Between-limits search, 386  
 Bin packing, 223  
 Binary cube network, 358  
 Bipolar technology, 53  
 Bit-parallel associative memory, 378  
 WPBP and WSBP, 36–37  
 Bit-serial associative memory, 378  
 WPBS and WSBS, 36–37  
 Bit-serial associative processor, 380–381  
 Bit slice, 34–35, 289, 375–378, 422, 424  
 Bit-slice (bis) processing, 37  
 Bit vector, 289  
 Block frame, 98–99  
 Blocked process, 68  
 Blocking network, 336, 374  
 Bode, A., 50  
 Boolean operator, 386  
 Borgerson, B. R., 729  
 Bovet, D. P., 321  
 Branching, 187–193, 419, 431  
 Briggs, F. A., 229, 454, 518, 551, 634, 637  
 Bucher, I. Y., 726–729  
 Buddy memory placement, 75–76  
 Bulk memory, 259  
 Burroughs B-5500, 73  
 Burroughs B-6500, 400, 409, 410, 440  
 Burroughs B-7800, 4, 410  
 Burroughs Scientific Processor (BSP), 25, 327, 328, 394, 397–422, 438, 440, 447  
 Bus grant signal (BGT), 484, 486  
 Bus receive table (BRT), 707  
 Busing structure, 193–196  
 Busy-wait, 12, 562  
 Butterfly operation, 367–369
- C access memory configuration, 160–161  
 Cache coherence, 55–56, 102, 139–140, 471, 508, 517, 519, 521, 522  
 Cache hit, 98–102, 112–113  
 Cache-invalidate interface, 522  
 Cache memory, 9, 12, 16, 150  
 access time, 114  
 addressing, 111–112  
 bandwidth, 101  
 characteristics of, 98–118  
 cycle time, 520  
 directory, 98–99  
 multiple, 517  
 organization, 102–113  
 partitioned, 112–113  
 placement policy (mapping), 102–106, 109  
 private, 471, 510, 520, 548  
 shared, 520  
 size selection, 108–111  
 Cache miss, 511–512, 517, 522  
 CAD/CAM/CAI (computer-aided design,  
 computer-aided manufacturing, and  
 computer-aided instruction), 45  
 California Institute of Technology, 468  
 Capability, 587–590  
 Carnegie-Mellon University, 463, 470  
 Carr, H. M., 321  
 Carry-lookahead adder, 12  
 Carry-propagation adder (CPA), 170  
 Carry-save adder (CSA), 12, 170, 171  
 CDC computers (*see* Cyber-170; Cyber-205;  
 Star-100)  
 CDC 1604 computer, 280  
 CDC-6600, 3, 11, 12, 177, 233, 235, 280  
 CDC-7600, 3, 381, 410  
 Cell block, 752  
 Central exchange jump (CEJ), 478  
 Central memory (CM), 473, 715  
 CFT, 441  
 Chamberlin's lifetime function model, 85–86  
 Chan, H., 229

- Channel, I/O, 10, 385, 471, 490  
 Channel and arbiter switch (CAS), 460, 461, 463  
 Channel address word (CAW), 131  
 Channel architecture, 128-132  
 Channel command word (CCW), 131  
 Channel program, 131  
 Charge-coupled device (CCD), 53, 55  
 Cheng, Y. H., 551, 789, 791-794, 808  
 Chow, C. K., 141  
 Circuit, integrated, 3-4  
 Circular wait, 540  
 CLIP-4, 394  
 Clock, common, 20  
 Clock period, 146  
 Clock replacement, 92  
 Clos network, 337  
 Closed spiral, 426  
 Cluster, 464  
 Clustering, 550  
 $Cm^*$ , 27, 459, 463, 467, 510, 530, 551  
 C.mmp, 3, 27, 38, 470-472, 478, 481, 489, 490, 549, 645-658  
     architecture, 646-650  
     performance analysis, 650-655  
 Cobegin-coend, 535, 536, 539, 540, 544  
 Cobol, 3  
 Code generation, 305  
 Code motion, 309  
 Coffman, E. G., 141, 603  
 Collision matrix, 208  
 Collision prevention, 203-208  
 Collision vector, 204  
 Command chaining, 131  
 Common bus, 481  
 Communication, 462, 539  
     inter-PE, 332  
     interprocessor, 715-716  
 Communication memory, 462  
 Commutativity, 542  
 Comparand register, 375  
 Compare and swap, 480, 559-562  
 Compiler:  
     address mapping by, 61  
     vectorizing, 217-219, 296, 303-308  
     (See also Languages, computer)  
 Component counter, 274  
 Compress-expand operations, 297-298  
 Compress instruction (vector), 214, 289, 298  
 Computation rate, 14  
 Computer architecture, 2  
     classification schemes, 32-40  
 Computer-assisted tomography (CAT) scan, 48  
 Computer module (CM), 460, 466, 467, 474  
 Computer systems:  
     centralized vs. distributed, 7, 27  
     evolution and generations of, 1-4  
     levels of, 4-6  
 Computer vision, 375  
 Concurrency, high-level, 299, 767  
 Concurrent ALGOL, 355  
 Concurrent event, 6  
 Concurrent processes, 540, 550  
 Concurrent quicksort, 625-627  
 Condition synchronization, 558  
 Conditional critical section, 572-574  
 Conflict, memory, 14, 21, 53, 57-60, 462, 470, 511  
 Connectivity, network, 373  
 Conservation law, 802  
 Consistency, data, 55-56, 102, 139-140, 471, 508, 517  
 Constant folding, 309  
 Content addressable, 325, 375, 380  
     (See also Associative memory)  
 Context switch, 68, 99, 101-102  
 Context switching, 465, 478, 532  
 Control:  
     centralized vs. distributed, 333  
     inter-PE, 332-333  
 Control and maintenance unit, 411  
 Control bus, 327  
 Control Data Corporation (see entries beginning with the term: CDC)  
 Control-driven organization, 734  
 Control flow computer, 29, 733, 734  
 Control link, 430  
 Control processor, 411  
 Control signal, 424, 429  
 Control strategy, 203  
 Control token, 738  
 Control unit (CU), 24, 32, 326-327, 373, 398, 400-402, 409, 422, 441, 448, 452, 453  
 Controller, disk, 16  
 Controller, I/O, 709-712  
 Convergence division, 170, 179  
 Converging factor, 177  
 Conway, L., 552  
 Core storage, 54-55  
     extended (ECS), 55  
     large (LCS), 55  
     magnetic, 3  
 Correlation control unit, 381  
 Coupled systems (see Loosely coupled systems; Tightly coupled systems)  
 CPU (central processing unit), 8-9  
     pipelining in, 150  
 CPU-bound, 18, 769  
 CPU utilization and saturation, 88-91, 595

- Cray-1, 4, 14, 22, 151, 154, 189, 194, 216, 228, 235, 264–280, 319  
 Cray-2, 4, 27, 235, 728  
 Cray Operating System (COS), 718  
 Cray X-MP, 4, 27, 235, 262, 280, 477, 480, 714–728  
     architecture, 715–716  
     performance analysis, 721–728  
 Critical section, 539, 540, 548, 551  
 Cross-interrogate, 521  
 Crossbar network, 25, 336, 338, 342, 502  
 Crossbar switch, 143, 415, 469, 471, 473, 487–492, 495, 504, 513, 517, 548  
 C/S access memory organization, 162  
 Cumulative distribution function (CDF), 592, 606–610  
 Cyber-170 (CDC), 459, 473, 478, 526  
 Cyber-205 (CDC), 3, 4, 15, 22, 153, 154, 216, 235, 280–293, 454  
**Cycle:**  
     pipeline, 20  
     simple and greedy, 206  
**Cycle ratio**, 520  
**Cycle stealing**, 12  
**Cycle time memory**, 13–14, 160  
  
**Daisy chaining**, 482, 484  
**Data buffer unit**, 193–196  
**Data dependency**, 7, 21, 29, 164, 233, 542  
**Data-dependent hazard**, 201  
**Data-driven organization**, 734  
**Data flow computers**, 20, 29–31, 735–737, 748–763  
     advantages, 745–746  
     Data flow graphs, 29, 740–742  
     Data flow languages, 740, 761  
**Data link**, 430  
**Data-manipulator network**, 336, 347–350  
**Data processing**, 4–6  
**Data rate, average**, 161  
**Data routing**, 327–328, 330–332, 344  
**Data-routing register**, 328  
**Data stream**, 32  
**Data token**, 735  
**Data transfer rate**, 14  
**Data transmission (communication)**, 119  
**Data transmit pipeline**, 273  
**Database machine**, 16, 385, 396, 425  
**Database-management system**, 385  
 Davidson, E. S., 154, 208, 229, 321, 551  
 Davis, A. L., 808  
**Deadlock**, 526, 577–583  
     prevention, 580–582  
     recovery, 582–583  
  
**Decimation-in-frequency (DIF) technique**, 367–368  
**DECNET**, 430  
**Decomposition**, 615–616, 619  
**Degree of multiprogramming (DOM)**, 87  
**Delta network**, 494–508, 551, 754  
**Demand fetch**, 82, 113  
**Demultiplexer**, 494  
**Denelcor, Inc.**, 670–676, 729  
**Denning, P.**, 80, 551  
**Dennis, J. B.**, 50, 732, 748–749, 807  
**Dependence-driven**, 764–765  
**Despain, A.**, 468  
**Deterministic scheduling**, 592  
**Device driver**, 118  
**Diagnostic mode**, 409  
**Dias, D. M.**, 551  
**Dijkstra, E. W.**, 552  
**Direct-access storage device (DASD)**, 53  
**Direct mapping**, 64, 102–103  
**Direct-memory access (DMA)**, 12, 122–123, 128, 134–136, 239, 249, 385  
**Disk**, 53–55, 119  
     electronic (CCD, MBM), 55  
**Dispatcher subsystem**, 91, 345–350, 354, 374  
**Distributed Array Processor (DAP)**, 37, 394–395  
**Distributed control**, 333  
**Distributed logic**, 381  
**Distributed processing**, 7, 27  
**Distribution network**, 749, 753  
**Divide loop**, 180  
**Domain of instruction**, 201  
**Dorr, F. W.**, 321  
**Dot product**, 213  
**DR-780**, 430  
**Drain time**, 513  
**Dubois, M.**, 229, 551  
**Dynabus**, 705–707  
**Dynamic address translation (DAT)**, 68  
**Dynamic coherence check**, 521  
**Dynamic data flow computers**, 737, 755–763  
**Dynamic decomposition**, 615–616  
**Dynamic network**, 333–339  
**Dynamic priority algorithm**, 485  
**Dynamic relocation**, 64  
  
**Economic modeling**, 43, 410  
**EDDY dataflow machine**, 760–761  
**EDVAC (Electronic Discrete Variable Automatic Computer)**, 3  
**Efficiency**, 151, 315, 445, 446, 550  
**El-Ayat, K. A.**, 134, 136, 141  
**Element memory control**, 381

- Elemental delay**, 209  
**Enea, H.**, 807  
**Energy resource exploration**, 46–47  
**Engineering design**, 44–46  
**ENIAC (Electronic Numerical Integrator and Computer)**, 2  
**Enslow, P. H., Jr.**, 49, 551  
**Equivalence search**, 385  
**Error detection**, 481  
**Evaluation time**, 154  
**Event**, 540, 541  
  concurrent, 6  
**Event-driven**, 766–767  
**Exchange function**, 350  
**Exchange package**, 189  
**Exchange state**, 336, 344, 352  
**Exclusive read only (EX)**, 522  
**Exclusive read-write (R/W)**, 522  
**EXEC operating system (Univac)**, 701–704  
**Execution unit**, 150, 165, 191  
**Expert systems**, 6  
**Explicit parallelism**, 530  
**Expression optimization**, 308–310  
**Extended core memory (ECM)**, 473–474  
**External interrupt**, 125–126  
**Extreme search**, 385  
  
**Fairbairn, D. G.**, 808  
**Fan-out module**, 425, 494, 495  
**Fast Fourier transform (FFT)**, 258, 352, 355, 367–373, 413, 542  
**Fault**:  
  addressing, 62  
  page (*see* **Page fault**)  
**Fault handling**, 531  
**Feierbach, D. G.**, 454  
**Fellér, W.**, 81  
**Feng, T. V.**, 35, 50, 373, 385, 388  
**Feng's classification**, 35–37  
**Fernbach, S.**, 4  
**Ferromagnetic technology**, 3, 54  
**Fetch-and-add**, 563–565  
**Fetch-fetch forwarding**, 198  
**Fetch policy**, 62, 82, 113–118  
**File memory**, 411, 413, 417  
**Finite-element analysis**, 44  
**First fit memory placement**, 75  
**First-in, first-out (FIFO)**, 92, 150, 482, 487.  
  506  
  global, 211  
**Fixed partition**, 80  
**Fixed time slicing (FTS)**, 485  
**Flagged registered write-back (FRWB)**  
  memory update, 115  
  
**Flagged write-back (RWB) memory update**, 114–115  
**Flip network**, 354  
**Floating supervisor control**, 527, 528  
**Flow of control, sequential**, 734  
**Flow of data**, 352–353, 399, 733  
**Flow time**, 596  
**Flushing time**, 217  
**Flynn, M. J.**, 32, 50, 229  
**Flynn's classification**, 32–35  
**Foley-Sammon algorithm**, 804  
**Forbidden list**, 204–206  
**FORK statement**, 533–535, 552, 733  
**FORTRAN**, 3, 404–409, 414, 418, 440, 441  
**FORTRAN 77/VP**, 296  
**FORTRAN vectorizer**, 303, 417, 418, 454  
**Foster, C. C.**, 388  
**4-cube network**, 358  
**FPS-164**, 258–259  
**Fragmentation**, 79–80  
**Frequency counter**, 546, 547  
**Fritsch, G.**, 729  
**Front-end computer**, 264–265  
**Fujitsu FACOM 200M**, 262  
**Fujitsu FACOM 230/75**, 236, 262  
**Fujitsu M 382**, 4  
**Fujitsu VP-100**, 293  
**Fujitsu VP-200**, 22, 154, 216, 229, 235,  
  293–301  
**Fuller, S. H.**, 646, 728  
**Fully associative cache placement**, 104  
**Fully parallel associative processor**, 380  
**Fung, H. S.**, 388  
  
**Gajski, D.**, 454, 729, 764, 765, 807, 811  
**Generations, computer**, 1–4  
**Genetic engineering**, 49  
**Ginsberg, M.**, 321  
**Global indexing**, 332  
**Global table**, 522, 523, 525  
**Global variable**, 532  
**Glypnir**, 409, 440, 441, 454  
**Goddard Space Flight Center (NASA)**, 422,  
  423  
**Goke, R.**, 551  
**Gonzalez, R.**, 552  
**Goodyear Aerospace Corporation**, 327–328,  
  374, 383, 423, 454  
**Gosden, J. A.**, 552  
**Gostelow, K. P.**, 745, 746, 807–808  
**Gottlieb, A.**, 729  
**Government use of computers**, 43  
**Graham, R. L.**, 80, 603  
**Greater-than search**, 386

- Greedy cycle, 206  
 Greedy strategy, 203  
 Grohoski, G. R., 229  
 Guardian-Expand Network system, 713  
 Guardian operating system, 712-713  
 Gurd, J., 762-763, 808
- Habermann, A. N., 551  
 Händler, W., 37, 50, 151, 229  
 Händler's classification, 137-140  
 Handshaking, 125  
 Hansen, P. B., 552  
 Harbison, S. P., 728  
 Hayer, J. P., 49, 229  
 Hazard, detection and resolution, 200-203  
 Hedlund, K. S., 787, 808  
 Hellermann, H., 163, 229  
 HEP (Denelcor), 4, 27, 262, 477, 669-684  
     architecture, 670-672  
 Hierarchical memory, 12-13  
 Higbie, L. C., 320  
 Hintz, R. G., 229, 321  
 Histogramming, 546, 548  
 Hit, cache, 98-102, 112-113  
 Hit ratio, 56, 98, 525  
 Hoare, C. A. R., 552  
 Hockney, R. W., 49, 320, 388  
 Holes, memory, 75  
 Home memory, 509, 510  
 Honeywell 60/66, 459, 471, 473, 474, 522  
 Horizontal processing, 226-227  
 Host computer, 327-328, 396, 410, 425  
 Hsiao, D., 385  
 Hu, T. C., 602, 604  
 Hwang, K., 50, 180, 218, 229, 230, 321, 388,  
     454, 551, 637, 729, 766, 789, 791-794, 805,  
     807-808  
 Hydra Operating System, 650-654
- IBM 303X computer, 285  
 IBM 360/85, 106  
 IBM 360/91, 3, 11, 154, 164-181, 191-198, 234,  
     236, 249, 259  
 IBM 370/158, 103  
 IBM 370/168, 4, 9-10, 14, 77-78, 118, 427,  
     478, 480, 492, 528, 685-687  
 IBM 370/195, 234, 236, 249, 259  
 IBM 701 electronic calculator, 3  
 IBM 1620 computer, 3  
 IBM 2938 computer, 259  
 IBM 3033 system, 14, 111, 115, 118, 687-690  
 IBM 3035 computer, 235, 249, 259
- IBM 3081 system, 4, 27, 234, 259, 471, 477,  
     690-692  
 IBM 3084 system, 471  
 IBM 3838 computer, 154, 235, 249, 259-262,  
     328  
 IBM 4341 computer, 259  
 IBM 7094 computer, 233  
 IBM AP configuration, 686  
 IBM MP configuration, 686  
 IBM operating system, 693-694  
 ID (Irvine Dataflow) Language, 740  
 Identifier, unique, 61  
 Illiac-IV computer, 3, 25, 37, 234, 328, 394,  
     397-410, 426, 440, 441, 444, 447, 448, 452,  
     454  
 Image processing, 375, 430, 433, 454  
 Implicit parallelism, 530  
 Independent reference model (IRM), 83  
 Index increment, 302  
 Indexing:  
     global vs. local, 332  
     row-major, 362-363  
 Indicator register, 375  
 Individual stage control, 349  
 Information processing, 4-6  
 Initial index, 302  
 Initiation interval set, 209  
 Input/output (I/O):  
     asymmetry, 471  
     overlapping, 12, 18, 233  
     private, 483  
 Input/output-bound (I/O-bound), 18, 769  
 Input/output (I/O) channel, 10, 385, 471, 490  
 Input/output (I/O) control, 429, 709  
 Input/output (I/O) controller, 709-712  
 Input/output (I/O) devices, 14  
 Input/output (I/O) interface, 425, 428, 460  
 Input/output (I/O) interrupt, 120-129  
 Input/output (I/O) processor (independent),  
     410, 428  
 Input/output (I/O) register, 424  
 Input/output (I/O) subsystem, 8-9, 118-141,  
     259, 716  
 Input selector (IS), 334  
 Instruction:  
     control-type, 327  
     decoding, 150  
     execution, 31  
     fetch, 150  
     prefetch, 187-193  
     range and domain of, 201  
     scalar, 327  
 Instruction buffer, 194  
 Instruction cycle, 20-21

- Instruction lookahead**, 153  
**Instruction pipeline**, 12, 21–22, 150, 153, 164–181  
**Instruction processing unit (IPU)**, 218, 242  
**Instruction stream**, 32  
**Instruction unit**, 150, 165, 191  
**Integrated circuit**, 3–4  
**Intel 8089 I/O processor**, 133–141  
**Intelligence processing**, 4–6  
**Interactive state**, 515, 516  
**Intercluster bus**, 464, 466, 467  
**Interconnection network (IN)**, 327–328, 332–354, 373–374, 388, 434, 453, 460, 481, 487, 513, 519, 520  
**Interface unit**, 249  
**Interleaved memory**, 58–60, 156, 233, 508, 513  
**Interlock**, 201–203  
**Internal forwarding**, 196–200  
**Internal interrupt**, 125–126  
**International Computer Limited**, 395  
**Interrupt**:  
 external and internal, 125–126  
 precise and imprecise, 188  
 vectored, 128–129  
**Interrupt handler**, 189  
**Interrupt signal**, 409  
**Interrupt-signal interconnection network (ISIN)**, 468, 471  
**Inverse perfect shuffle**, 350–352  
**Inverse translation buffer (ITB)**, 112  
**I/O (see entries beginning with the term: Input/output)**  
**Irvine dataflow machine**, 756
- Jesshope**, C. R., 49, 320, 388  
**Job sequencing**, 203–208  
**Johnson**, J. B., 275, 321  
**Johnson**, L., 468  
**JOIN statement**, 533–535, 537, 552, 734  
**Jones**, A. K., 530, 551, 728–729  
**Jumps**, J. R., 551
- Kasic**, M. J., 321  
**Katzman**, J. A., 729  
**Kbus**, 465, 466  
**Keller**, R. M., 230, 321  
**Kennedy**, K., 321  
**Kernel code**, 469  
**Kernal multiprogramming system (KMPS)**, 654  
**Kernel semaphore**, 653  
**Kmap**, 464, 467  
**Knee criterion**, 90
- Knowledge processing**, 4–6  
**Knuth**, D. E., 163  
**Kogdrowicki**, E. W., 320, 454  
**Kogge**, P. M., 229, 321  
**Kuck**, D. J., 49, 229, 321, 388, 454  
**Kuhn**, R. H., 50, 729  
**Kung**, H. T., 363, 365, 388, 769–772, 808  
**Kung**, S. Y., 808
- Lang**, W. G., 229, 388  
**Languages, computer**:  
 array processing, 4, 440  
 data flow, 740, 761  
 early, 3–4
- Larc system (Sperry Rand)**, 3, 233  
**Larson**, A. G., 321  
**Last-in, first-out (LIFO) replacement**, 92  
 global, 211
- Latch**, 146, 160  
**Latency**, 203–208  
**Lawrie**, D. H., 352, 388, 438, 454  
**Layered protection**, 585  
**Least frequently used (LFU) replacement**, 92  
**Least processed first (LPF)**, 211  
**Least recently used (LRU) replacement**, 91, 485, 487
- Least recently used stack model (LRUSM)**, 83  
**Least work remaining first (LWRF)**, 211  
**Leontief**, W. W., 43  
**Library**, mathematic, 255  
**Lifetime function (paging)**, 84–85  
**Lincoln**, N. R., 291, 321  
**Line controller (LC)**, 497–498, 512–513  
**Line service time**, 513  
**Linker**, 61  
**Lint**, B., 551  
**Lipovski**, G. J., 551  
**LIPS (logical inferences per second)**, 45  
**List scheduling**, 602  
**L-M memory**, 510–512  
**Load control**, 86–91  
**Load-through**, 113  
**Local address**, 330, 463  
**Local indexing**, 332  
**Locality, programs, models of**, 83–86  
**IRM and LRUSM**, 83  
 micromodel and macromodel, 84
- Locality of reference**:  
 sequential, 62–63  
 spatial, 62, 108  
 temporal, 62–63, 108, 111
- LOCK**, 558–559, 562  
**Lock-out**, 527, 528

- Lock-step operation, 332  
 Logical operation, 431  
 Lookahead algorithm, 92  
 Loosely coupled systems (LCS), 35, 460–462, 508, 550  
 Lower broadcast state, 336, 352  
 Lower instruction parcel (LIP), 269  
 L-S criterion, 90  
 LSI (large-scale integration), 4  
 LSI-11, 467  
 L-U decomposition, 777–779, 790–796
- Macropipelining, 614–615  
 Magnetic bubble memory (MBM), 53, 55  
 Mailbox, 531, 568  
 Main memory (MM), 511  
 Maintenance control unit (MCU), 265  
 Majithia, J. C., 229  
 Manchester machine, 762–763  
 Map bus, 464  
 Mapping, address, 61–64, 72  
     cache, 102–106, 109  
 Marathe, M., 728  
 Mark IIA, 659–665  
 Markov chain, 513  
 Mask pipe, 297  
 Mask register, 297  
 Maskable interrupt, 126  
 Masked operation, 297  
 Masking, PE, 332  
 Masking register, 329, 375  
 Masking vector, 214, 269, 297, 327  
 Massbus, 9  
 Massively parallel processor (MPP) Goodyear Aerospace, 4, 25, 37, 46, 328, 395, 410, 422–437, 454  
 Master-slave configuration, 526, 528  
 Match (*see* Hit, cache)  
 MATP computer (Datawest), 154, 262, 328  
 Matrix algorithms, 355–359, 435, 613–616, 790–803  
 MC 68000 (Motorola), 484  
 Memory:  
     allocation of, 80–88  
     associative (AM), 25, 57–58, 64, 374–380, 385  
     bandwidth of, 156, 163  
     cache (*see* Cache memory)  
     central (CM), 473, 715  
     compaction of, 76  
     described, 8–9  
     fetch and placement, 62, 82, 96–98, 113–115  
     local, 24, 53  
     management policy, 80–98  
     Memory (*Cont.*):  
         mapping of, 285  
         primary vs. secondary, 53  
         private, 483  
         protection of, 479  
         update policy, 113–115  
         virtual, 3, 12, 60–80, 248  
     Memory bank, 415, 417  
     Memory buffer unit (MBU), 242–243  
     Memory control element (MSC), 522  
     Memory cycle, 436, 510, 513  
     Memory fault, 424, 428  
     Memory fragmentation, 68, 76  
     Memory hierarchy, 52–58  
     Memory module, 12, 32, 327, 373–374, 411, 415–416, 435, 461, 468, 470, 481, 487–491, 500, 506–509, 512–513, 517  
     Memory placement algorithms, 75–76  
     Memory policy:  
         global and local, 82  
         inclusion property, 92–93  
     Memory-reference instruction, 330  
     Memory-to-memory instruction, 216, 281, 285  
     Merge, 367  
     Merge instruction (vector), 214, 289, 349  
     Merwin, R., 388  
     Mesh network, 334, 345, 361–362, 365, 399–400  
     Message primitives, 712–713  
     Message-transfer system (MTS), 460–462  
     Metal oxide semiconductor (MOS) technology, 54  
     Microcode unit (MIC), 246  
     Military applications, 49  
     MIMD machine, 32–34, 374, 397, 448, 453, 533, 541  
         algorithms for, 613–616  
     MINIMA search, 387  
     Minimum average latency (MAL), 205–208  
     Minsky's conjecture, 27–29  
     MIPS (million instructions per second), 14, 45, 229  
     MISD machine, 32–34  
     Miss, cache, 511–512, 517, 522  
     MIT dataflow machine, 748–754  
     MIT/IL ACGN, 483  
     Miura, K., 321  
     Models, scientific, 41–43  
     Modem, 119  
     Modified flag, 522  
     Modified table, 522  
     Module, program, 71  
     Moldovan, D. I., 808  
     Monitor, 574–577, 655

- MOPS (million operations per second), 235–236
- Most processed first (MPF), 211
- Most work remaining first (MWRF), 211
- Motooka, T., 764
- MSI (medium-scale integrated) circuits, 3
- MSIMD (multiple-SIMD), 397, 448, 452–453
- MSISD (multiple-SISD), 34
- Mueller, P. T., 369, 388
- Multi-access memory (*see* Associative memory)
- Multi-Associative Processor (MAP), 448
- Multichip carrier (MCC), 296
- Multidimensional access (MDA), 381, 383, 424
- Multipfunctionality, 11–12
- Multiplexor, 128–132, 474
- Multiplication matrix algorithms, 355–359, 435, 796
- Multiplier recoding, 180
- Multiport memory, 25, 487, 490, 492, 517
- Multiprocessing, 6–7
- Multiprocessor, 25–27, 31, 459–460, 468, 471, 526, 531, 591–605, 614, 643–645  
 commercial systems, 644–645  
 evolution of, 4  
 exploratory systems, 643–644  
 interconnections for, 25  
 operating systems for, 525  
 scheduling of, 590–602  
 software requirements for, 528
- Multiprocessor anomalies, 605
- Multiprocessor systems, 459
- Multiprogramming, 3, 6–7, 16–19
- Multistage network, 334–339, 344, 354, 373–374, 492–493
- MUTEXBEGIN and MUTEXEND, 539
- Mutual exclusion, 532, 539, 558
- Naming (compiler), 61
- NASA Ames Research Center, 394, 444
- N-cube network, 336, 343–344, 352
- Nearest below search, 386
- Network:  
 control structure, 336, 339, 344  
 interconnection, 327–328, 332–354, 373–374, 388, 434, 453, 460, 481, 487, 513, 519, 520  
 inter-PE communication, 327  
 passive vs. dynamic, 333  
 topology, 334–354  
*(See also specific network name)*
- Network access device (NAD), 290
- Newton-Raphson iteration, 413
- Newton's iteration, 516, 618, 622–624
- Next instruction parcel (NIP), 269
- Ni, L. M., 50, 454, 551
- Nonblocking crossbar, 487
- Noncacheable data, 520
- Noncompute delay, 208
- Nonlookahead algorithms, 92–93
- Nonmaskable interrupt, 126
- Not-equal-to search, 385
- Not-greater-than search, 386
- Not-smaller-than search, 386, 387
- NP-hard problems, 468
- Nuclear reactor safety, 48
- Numerical Aerodynamic Simulation Facilities (NASF) computer, 45, 293
- Object, data and resource, 201
- Oceanography, 43
- Octets, 243
- Odd-even merge sort, 363–364
- Oleinick, P. H., 657–658, 728
- Omega network, 336, 350–354, 373
- OMEN, 395
- On-line mode, 424
- One block lookahead (OBL), 97–98
- One-sided network, 336
- Operating system, 409, 453, 525–527, 529, 531, 550–551, 693–694  
 classification of, 526  
 requirements for, 531
- Optimization, 305–314
- Order statistics, 611
- Ordered retrieval, 386
- OS/VS2 (IBM), 693–694
- Out queue, 466
- Output selector (OS), 334
- Overlapping, I/O and CPU, 12, 18, 233
- Overlay, 61
- PACK instruction, 302
- Packet-switched bus, 466
- Packet switching, 333
- Packet switching network, 673–674
- Padua, D. A., 50
- Page fault, 91–96, 549  
 rate of, 77–78, 84–86  
*(See also Cache miss)*
- Page-fault frequency (PFF) replacement, 95–96
- Page segmentation, 77–80
- Page size, 79–80
- Page table, 65
- Paging, 65–71

- Parallel algorithm, 355–356, 447, 467, 517, 545, 614  
 Parallel control flow, 734  
 Parallel Element Processing Ensemble (PEPE) (Burroughs), 37, 327, 374, 378, 380–382, 385, 395  
 Parallel event, 6  
 Parallel for (parfor) statement, 537, 547, 549, 552  
 Parallel language, 218, 301–305  
 Parallel memory, 434, 508  
 Parallel priority resolution, 484  
 Parallel processing, 6–27  
     applications of, 40–49  
     vs. serial processing, 7, 35–36  
 Parallel processor (*see* SIMD computers)  
 Parallel search memory (*see* Associative memory)  
 Parallel transmission, 119  
 Parallelism:  
     degree of, 35, 37–40, 218  
     explicit, 530  
     implicit, 530  
     in pipelining, 145–164  
     temporal, 20, 145  
 Parallelization, 310  
 Parbegin-parend, 535  
 Parity checking, 428  
 Partial differential equation (PDE), 619, 627  
 Partitioned algorithm, 790–803  
 Partitioning, 80–98  
     program, 545–551  
 Pascal, 441, 444, 521  
 Patel, J. H., 494–508  
 Pattern classification, 806–807  
 Pattern embedding, 784–786  
 Pattern recognition, 430, 433  
 Paul, G., 301, 321, 388, 551  
 PCU (*see* Control unit)  
 PDP-10, 459, 473, 476  
 PDP-11, 38, 249, 424, 430, 461, 478, 482, 530  
 PE (*see* Processing element)  
 PE/VE semaphore, 568–571  
 Peak speed, 229  
 Pease, M. C., 388  
 Pease binary  $n$ -cube network, 344  
 Pedegs, A., 728  
 Perfect shuffle, 350–352, 365  
 Performance, 27–29, 56–57, 393–453, 505, 515  
 Peripherals, 119–120  
 Permutation, network, 373  
 Perrott, R. H., 301, 441, 454  
 Phoenix project, 343, 394, 397, 448, 452, 454  
 Physical addressing, 111  
 Ping-ponging, 548  
 Pipeline, 154–164  
     array, 181–187  
     chained, 264, 271–276, 310, 719  
     clock period of, 146  
     draining of, 22  
     dynamic, 153, 208–212  
     efficiency of, 151  
     instruction, 12, 21–22, 150, 153, 164–181  
     linear, 146–151  
     multiple, in vector processing, 218, 220–223  
     overhead and delay in, 220  
     speedup of, 148–151  
     stages in, 146  
     static, 153  
     throughput of, 146, 151  
     unifunction vs. multifunction, 153  
     in vector processing, 153, 218–229, 270  
 Pipeline attached computer, 327  
 Pipeline interval, 256  
 Pipeline processor, 20–22, 233–320, 510  
     design of, 187–212  
 Pipelined event, 6  
 Pipelining, 145–229  
     within CPU, 12  
     degree of, and classification of computers, 37–40  
 Placement decision, 590  
 Plasma fusion power, 47–48  
 Pluribus, 530  
 Plus-minus-2' (PM21) network, 345  
 Policy semaphore, 654  
 Polled interrupt, 126  
 Polling, 486  
 Port, I/O, 427  
 Potter, J., 454  
 Precedence graph, 146  
 Precedence partition, 599  
 Precise interrupt, 188  
 Preemptive scheduling, 594  
 Prefetch, 96–98  
 PREP, 537  
 Presence flag, 522–523  
 Printed circuits, 3  
 Priority, 482  
 Priority queue, 766  
 Private table, 527  
 Problem solving, scientific, 40–41  
 Process:  
     communicating, 539  
     lifetime of, 520  
 Process execution module, 674–676  
 Process queue, 86–91  
 Process space, 70

Processing element (PE), 22, 326–327, 381, 394–410, 424–434, 441, 445–448, 452–453, 548  
 Processing element memory (PEM), 327–328, 330–331, 356, 399–410, 445  
 indexing of, 362–363  
 Processing unit (PU), 32  
 Processor pipeline, 153  
 Processor status word (PSW), 463  
 Processor utilization, 515, 517, 596  
 Producer and consumer, 566–568  
 Production system, 530–531  
 Program and data management unit, 424  
 Program behavior, models of, 83–84  
 Program counter (PC), 9, 188  
 Program relocation, 63–64  
 Programmed input-output (PIO), 249  
 Protection, 679  
 Protection mask, 69–71  
 Proximate-to search, 386  
 P semaphore, 565–568  
 PUMPS, 448, 454  
 Purcell, C. J., 321

Queue, 454  
 priority, 766  
 process, 86–91  
 Queueing network, 513  
 Quicksort, concurrent, 625–627

Radar-signal tracking, 375  
 Ramamoorthy, R. V., 153, 229, 552  
 Random-access memory (RAM), 53, 374–375, 378, 393, 423  
 Random replacement, 92  
 Range of an instruction, 201  
 Rao, G. S., 163  
 Rau, B. R., 229  
 Read after write (RAW) hazard, 201–203  
 Read-modify-write memory, 559  
 Read only (RO), 522  
 Read-only memory (ROM), 212, 413, 440  
 Read set, 543  
 Read-through, 113  
 Rearrangeable network, 337  
 Receive-inactive, 345  
 Reciprocal approximation, 270  
 Recirculating network, 334, 342–345, 410  
 Reconfigurability, 208–212, 245, 374  
 Recoverability, 478  
 Recurrence vector instruction, 418  
 Recursive computation, 274–280

Reddi, S. S., 229  
 Reentrant supervisory code, 527–528  
 Reference string, 62, 82–83  
 Register tagging, 196–200  
 Register-to-register instruction, 216, 271  
 Registers, 9  
 local, 327–328  
 optimization of use of, 308  
 RELACS, 396  
 Reliability, 374, 478  
 Remote sensing, 456  
 Replacement policy, 62, 91–92  
 Request rate, 505  
 Reservation table, 154–156, 203  
 Reservoir modeling, 47  
 Resource allocation, 201, 526, 529  
 Resource sharing, 16–17, 32–38  
 Resource space, 221  
 Return message, 467  
 Ring, 585–587  
 Ritchie, D. M., 551  
 Rotate operator, 443  
 Rotating daisy chain (RDC), 485  
 Routing function, 339–340, 343–345, 348, 350–352, 362, 369, 402  
 Routing register, 409  
 Row-major indexing, 362–363  
 Row-major vector storage, 161  
 Rubinfield, L. P., 454  
 Russell, R. M., 321, 552

S access memory configuration, 158–160  
 Satyanarayanan, M., 49, 451, 729  
 Scalar, pipe, 153, 270  
 Scalar processing, 218, 401, 411, 413, 418, 430  
 Scalar-save register, 268  
 Scene analysis, 433, 803–807  
 Scheduler:  
 process, 91  
 system, 18  
 Scheduling, 590  
 fair, 539  
 optimization, 598  
 preemptive, 594  
 Schwartz, P., 530, 551, 728  
 Search algorithms, associative, 385–388  
 SECDED (single error correction and double error detection), 265, 411  
 Sector cache placement, 106  
 Seek time, 53  
 Segment table, 73–75  
 Segmentation, 71–80  
 Seismic exploration, 47, 410

- Selective fetch, 113  
 Selector channel, 128–131  
 Semaphore, 480, 530, 565–571, 653–654  
     synchronization, 565  
 Send-active, 345  
 Sensor-signal processing, 385  
 Senzig, D. N., 394  
 Separate executive system, 527  
 Sequential-access memory (SAM), 53  
 Serial processing vs. parallel processing, 7,  
     35–36  
 Serial transmission, 119  
 Set associative cache placement, 104–106  
 Setup time of a pipeline, 217, 220, 271  
 Shared resource, 16–17, 328  
 Shared variable, 539, 541  
 Shen, J. P., 388  
 Shift operator, 443  
 Shift register, 426, 427  
 Short-circuiting approach, 203  
 Short-stopping, 282  
 Shuffle, 350–352, 363, 497, 498  
 Shuffle-exchange network, 350–354, 373–374  
 Shuffled row-major indexing, 362–363  
 S-I multiprocessor, 4, 27, 113, 235, 471, 490,  
     518, 658–668  
     architecture, 659–665  
     performance, 668  
 Side effects, 744  
 Siegel, H. J., 374, 388  
 Siewiorek, D. P., 728  
 SIMD algorithms, 325–388, 453, 545, 614,  
     616–628  
 SIMD computers, 20–29, 32–34, 325–388,  
     393–453  
     interconnection network, 327–328, 333–354,  
     373–374, 434  
 Similar-to search, 385  
 Simple write-back (SWB) memory update, 114  
 Simulation, computer, 41–43  
 Simultaneous event, 6  
 Single assignment, 740, 744  
 Single-stage network, 334–336, 343, 354, 374  
 SISD computer, 32–34, 355–356, 445–446  
     matrix algorithms, 356  
 Sites, R., 551  
 Skew, 436  
 Skewed vector, 215  
 Skip distance, 160, 302  
 SL-1, 441  
 Slocal, 463  
 Slotnick, D. L., 394  
 Smaller-than search, 386  
 Smith, A. J., 394  
 Smith, B. J., 729  
 Snake-like row-major indexing, 362–363  
 Snyder, L., 780, 782–787, 808  
 Socioeconomics, 43  
 Software interrupt, 125–126  
 Solid-state storage device (SSD), 716  
 Solomon computer, 394  
 Sorting, 361–367  
     ascending and descending, 386  
 Space-time product, 86  
 Sparse vector instruction, 241  
 Spatial parallelism, 20  
 Speed, average vs. peak, 229  
 Speedup, 148–151, 315, 355, 373, 445–447, 550  
 Spin-lock, 562  
 Spiral connection, 426  
 SSI (small-scale integrated) circuits, 3  
 Stack algorithm, 94  
 Stage control, 339, 344  
 Stage space, 151  
 Stand-alone mode, 424  
 Star-100 (CDC), 3, 114, 151, 154, 189, 194,  
     216, 237, 244, 280, 290, 319  
 STARAN, 37, 327–328, 343–344, 349, 374,  
     378, 380–385, 395, 397, 424  
 Static coherence check, 519  
 Static data flow computers, 737, 748–755  
 Static decomposition, 615  
 Static network, 333–339  
 Static pipeline, 153  
 Static relocation, 64  
 Static tag, 520  
 Status checkboard, 233  
 Stephenson, C. M., 184  
 Stevens, K., 454  
 Stevenson, D. K., 454  
 Stirling's formula, 435  
 Stokes, R. A., 321, 454  
 Stone, H. S., 49, 229, 321, 388  
 Storage control unit, 165  
 Storage scheme, 158, 438  
 Store-fetch forwarding, 197  
 Store-store overwriting, 198  
 Straight state, 336, 344, 352  
 Stream processing, 237, 245  
 Stream unit, 238  
 STRETCH, 233  
 Stretch project, 3  
 String unit, 239, 281, 289  
 Strongly connected, 342  
 Su, S. P., 50, 218, 321, 766, 805, 807–808  
 Subtraction, 413, 431  
 Supercomputer, 234–235, 264, 300  
 Superfluity in segmentation, 76

- S**upervisor call (SVC), 478, 529  
**S**upervisor mode, 478  
**S**wain, P., 46  
**S**wapping, 97  
**S**witch, 332–333, 753, 781–783  
**S**witch box, 336, 339, 344, 352  
**S**witch lattice, 781–783  
**S**witching:  
 circuit and packet, 333  
 inter-PE, 332–333  
**S**ynchronization, 558–565, 679–690  
**S**ynchronization primitives, 480, 540  
**S**ynchronous communication, 332  
**S**ynonym problem, 111  
**S**yntax-parsing phase, 305  
**S**yre, J. C., 763, 808  
**S**ystem manager, 410  
**S**ystolic arrays, 334, 769–786  
 reconfigurable, 780–786
- T**able conflict, 527  
**T**agged prefetch, 113  
**T**agged tokens, 738  
**T**agging, 761, 762  
**T**akahashi, N., 760, 808  
**T**AL (Tandem Algorithmic Language), 705  
**T**andem Nonstop System, 27, 705–713  
 architecture, 707  
**T**ask graph, 222–226, 602–609  
**T**ask scheduling (vector processing), 218–229  
**T**ate, D. P., 229, 321  
**T**emplate (data flow computer), 31  
**T**emporary register, 375  
**T**erminal index, 302  
**T**esler, L. G., 807  
**T**est-and-set, 480, 559  
**T**heis, D. J., 320  
**T**hermal conduction module (TCM), 690  
**T**homas, A. T., 229  
**T**homas, R. E., 388, 756, 808  
**T**hompson, C. D., 363, 365, 388  
**T**hrashing, 87  
 3-cube connected-cycle network, 334  
 3-cube network, 334, 342, 358  
 Three-stage network, 343  
 Threshold search, 386  
**T**hroughput, 10, 151, 315, 445, 483, 519  
**T**hurber, K. J., 388, 395  
**T**I-ASC computer, 3, 35, 38, 151, 154, 183,  
 192, 194, 196, 212, 215, 233, 242–249  
**T**ightly coupled systems (TCS), 35, 460, 468,  
 480, 508, 510, 547  
**T**ime complexity, 355–357, 362
- T**ime division multiplexing (TDM), 485  
**T**ime interval (space-time diagram), 151  
**T**ime-shared common bus, 25  
**T**ime sharing, 3, 6–7, 16–19  
**T**ime slice, 18  
**T**ime-space span, 151  
**T**oken, 758, 763  
**T**omasulo, R. M., 230  
**T**opology, register, 426  
**T**RADIC, 3  
**T**ranquil, 440  
**T**ransistors, 3  
**T**ranslation lookahead buffer, 111  
**T**ranslation lookaside buffer (TLB), 64, 99,  
 111  
**T**ransportation sort, 363  
**T**ravel time, 256  
**T**ree machine, 468  
**T**ree task system, 224–225  
**T**releaven, P. C., 808  
**T**riadic operation, 413  
**T**riangular linear system, 797–798  
**T**rue ratio, 297  
**T**uning, 313  
**T**wo-sided network, 336
- U**ART (Universal Asynchronous Receiver-  
 Transmitter), 123  
**U**-interpreter, 745  
**U**nfolded, 744  
**U**nger machine, 394  
**U**nibus, 9  
**U**niform tree, 495  
**U**niprocessor, 8–19  
**U**nivac, 477, 492, 701–702  
**U**nivac 1100 series, 694–695, 701–705  
**U**nivac 1100/80, 4, 27, 471, 522, 696–700  
**U**nivac 1100/90, 492, 701  
**U**nivac multiprocessors, 694–704  
**U**nix, 528  
**U**nmapped local memory (ULM), 469, 471  
**U**unpack instruction, 302  
**U**pdate, memory, 113–115  
**U**pper broadcast state, 336, 352  
**U**ser mode, 478  
**U**tilization, 35, 445, 446, 532
- V** semaphore, 565–568  
**V**acuum tubes, 3  
**V**AL (Value Algorithmic Language), 740  
**V**ariable:  
 asynchronous, 680

- Variable (*Cont.*):  
 common, 536, 539  
 global, 532.  
 Variable parameter, 536  
 Variable partition, 80, 94–95  
 Varneschi, M., 321  
 VAX-11/780, 9, 69, 235, 259, 430, 484  
 Vector address, 215  
 Vector arithmetic multiprocessor (VAMP), 393, 397  
 Vector editing function, 292  
 Vector indirect addressing, 297  
 Vector instructions, 241, 245, 259, 271–272, 297  
 Vector length (VL), 268  
 Vector mask, 214, 269, 297, 327  
 Vector operation, 213–218  
 Vector parameters file (VPF), 248  
 Vector processing, 212–221  
 pipeline in, 153, 218–229, 270  
 Vectored interrupt, 128–129  
 Vectorization, 217, 233–320  
 Vectran, 301, 441  
 Vertical processing, 226–227  
 Vick, C., 388  
 Virtual addressing, 111  
 memory, 237, 466, 479  
 Virtual machine, 18, 394  
 Virtual memory, 3, 12, 50–80, 248  
 Virtual resource, 532  
 VLSI (very-large-scale integrated) technology, 1, 4, 20, 31, 349, 361, 426, 461, 488, 489, 746, 768, 788–807  
 VLSI arithmetic module, 788–790  
 VLSI processor, 20, 31  
 VMIN replacement, 96  
 Von Neumann architecture, 1, 29  
 Vora, C. R., 438, 454
- Wafer-scale integration (WSI), 787  
 Wait, 541  
 circular, 540  
 Wallace tree, 170–174
- Waser, S., 229  
 Wasted cycle, 505, 506  
 Watchdog timer, 481  
 Watson, I., 762, 808  
 Watson, W. J., 321  
 Weather forecasting, 42–43, 398, 410  
 WHERE instruction, 302  
 Widdoes, L. C., Jr., 728  
 Williams' tube memory, 3  
 Wilson, W. W., 301, 321  
 Wittmayer, W. W., 321  
 Word-parallel and bit-parallel (WPBP), 36, 37  
 Word-parallel and bit-serial (WPBS), 36, 37  
 Word parallel operations, 378  
 Word-serial and bit-parallel (WSBP), 36, 37  
 Word-serial and bit-serial (WSBS), 36–37  
 Word serial operations, 378  
 Word slice, 34, 37  
 Working set, 63  
 Working-set (WS) replacement, 95–96, 444  
 Working store, 261  
 Wootton, J., 29  
 Write-fit memory placement, 75  
 Write-around connection, 361–362  
 Write after read (WAR) hazard, 201–202  
 Write after write (WAW) hazard, 201–202  
 Write-back (WB) memory update, 114  
 Write-back-write-allocate replacement, 511  
 Write set, 543  
 Write-through (WT), 113–115  
 Write-through-with-no-allocate (WTWNA)  
 policy, 113, 114  
 Write-through-with-write-allocate (WTWA)  
 policy, 113, 114  
 Wu, C. L., 373, 388  
 Wulf, W. A., 551, 728
- Xerox Sigma 7 processor, 66  
 X-tree project, 468
- Yao, S. B., 637  
 Yau, S. S., 388