BIBLIOGRAPHY

Ackerman, W. B., and Dennis, J. B., "VAL—A Value-Oriented Algorithmic Language," *TR-218*, Lab. for Computer Science, MIT, June 1979.

Agerwala, T., "Some Extended Semaphore Primitives," *Acta Informatica 8*, Springer Verlag, 1977.

Agrawal, D. P., "Graph Theoretical Analysis and Design of Multistage Interconnection Networks," *IEEE Trans. on Comp.*, C-32, July 1983, pp. 637–648.

Algiere, J. L., and Hwang, K., "Sparse Matrix Techniques for Circuit Analysis on the Cyber 205," *TR-EE 83-40*, Purdue University, W. Lafayette, Indiana, October 1983.

Amdahl Corp., *Amdahl 470 V/6 Machine Reference Manual*, Sunnyvale, California, 1975.

Amdahl, G. M., Blaauw, G. A., and Boorks, F. J., Jr., "Architecture of the IBM System/360," *IBM Journ. of Res. and Dev.*, vol. 8, no. 2, 1964, pp. 87–101.

Anderson, D. W., Earle, J. G., Goldschmidt, R. E., and Powers, D. M., "The IBM System/360 Model 91: Floating-Point Execution Unit," *IBM Journ. of Res. and Dev.*, January 1967*a*, pp. 34–53.

Anderson, D. W., Sparacio, F. A., and Tomasulo, R. M., "The IBM System/360 Model 91: Machine Philosophy and Instruction Handling," *IBM Journ. of Res. and Dev.*, vol. 11, no. 1, 1967*b*, pp. 8–24.

Anderson, J. P., Hoffman, S. A., Shifman, J., and Williams, R. J., "D825-A Multiple Computer System for Command and Control," *Proc. AFIPS Fall Joint Computer Conference*, vol. 22, 1962, pp. 86–96.

Andrews, G. J., and McGraw, J. R., "Language Features for Parallel Processing and Resource Control," *Proceedings of the Conference on Design and Implementation of Programming Languages*, Ithaca, N.Y., October 1976.

Andrews, G. R., and Schneider, F. B., "Concepts and Notations for Concurrent Programming," *ACM Computing Surveys*, vol. 15, March 1983, pp. 3–43.

Arnold, C. N., "Performance Evalution of Three Automatic Vectorizer Packages," *Proc. of Int'l. Conf. Parallel Proc.*, 1982, pp. 235–242.

Arnold, J. S., Casey, D. P., and McKinstry, R. H., "Design of Tightly-Coupled Multiprocessing Programming," *IBM Systems Journal*, no. 1, 1974.

Arvind and Gostelow, K. P., "A Computer Capable of Exchanging Processors for Time," *Proc. 1977 IFIP Congress*, North-Holland, Amsterdam, 1977.

Arvind and Gostelow, K. P., "The U Interpreter," *IEEE Comp.*, vol. 15, no. 2, Feb. 1982, pp. 42–50.

Arvind and Iannucci, R. A., "A Critique of Multiprocessing von Neumann Style," *Proc. 10th Ann. Symp. Computer Architecture*, June 1983, pp. 426–436.

Arvind, Kathail, V., and Pingali, K., "A Data Flow Architecture with Tagged Tokens," *Technical Memo 174*, Lab. for Computer Science, MIT, Sept. 1980.

Association of Computing Machinery, "Special Issue on Computer Architecture," *Comm. of ACM*, vol. 21, no. 1, Jan. 1980.

Backus, J., "Can Programming Be Liberated from the von Neumann Style? A Functional Style and Its Algebra of Programs," *Comm. of ACM*, vol. 21, no. 8, Aug. 1978, pp. 613–641.

Baer, J. L., "A Survey of Some Theoretical Aspects of Multiprocessing," *ACM Computing Surveys*, vol. 5, no. 1, March 1973, pp. 31–80.

Baer, J. L., "Multiprocessing Systems," *IEEE Trans. on Comp.*, C-25, Dec. 1976, pp. 1271–1277.

Baer, J. L., *Computer Systems Architectures*, Computer Science Press, Potomac, Maryland, 1980.

Baer, J. L., and Bovet, D. P., "Compilation of Arithmetic Expressions for Parallel Computations," *Proc. IFIP Congress 1968*, North-Holland, Amsterdam, 1968; pp. 340–346.

Baer, J. L., and Ellis, C., "Model, Design, and Evaluation of a Compiler for a Parallel Processing Environment," *IEEE Trans. on Soft. Eng.*, SE-3, Nov. 1977, pp. 394–405.

Bain, W. L., Jr., and Ahuja, S. R., "Performance Analysis of High-Speed Digital Buses for Multiprocessing Systems," *Proc. 8th Ann. Symp. Computer Architecture*, May 1981, pp. 107–131.

Banerjee, U., Gajski, D., and Kuck, D., "Accessing Sparse Arrays in Parallel Memories," *Journ. of VLSI and Computer Systems*, vol. 1, no. 1, 1983, pp. 69–99.

Barke, D. F., ed., *Very Large Scale Integration (VLSI): Fundamentals and Applications*, Springer-Verlag, New York, 1980.

Barnes, G. H., Brown, R. M., Kato, M., Kuck, D. J., Slotnick, D. L., and Stokes, R. A., "The ILLIAC IV Computer," *IEEE Trans. on Computers*, Aug. 1968, pp. 746–757.

Baskett, F., and Keller, T. W., "An Evaluation of the CRAY-1 Computer," *High Speed Computer and Algorithm Organization*, Kuck, et al., eds., Academic Press, New York, 1977, pp. 71–84.

Baskett, F., and Smith, A. J., "Interference in Multiprocessor Computer Systems with Interleaved Memory," *Comm. of ACM*, vol. 19, no. 6, June 1976, pp. 327–334.

Batcher, K. E., "STARAN Parallel Processor System Hardware," *Proc. AFIPS-NCC*, vol. 43, pp. 405–410.

Batcher, K. E., "The Flip Network in STARAN," *Int'l. Conf. Parallel Proc.*, Aug. 1976, pp. 65–71.

Batcher, K. E., "The Multi-dimensional Access Memory in STARAN," *IEEE Trans. on Comps.*, 1977, pp. 174–177.

Batcher, K. E., "Design of a Massively Parallel Processor," *IEEE Trans. on Comp.*, C-29, Sept. 1980, pp. 836–840.

Baudet, G. M., "Asynchronous Iterative Methods for Multiprocessors," *Journ. of ACM*, vol. 25, no. 2, Apr. 1978, pp. 226–244.

Bauer, L. H., "Implementation of Data Manipulating Functions on the STARAN Associative Array Processor," *Proc. Sagamore Comp. Conf. Parallel Proc.*, Aug. 1974, pp. 209–227.

Bell, C. G., Mudge, J. C., and McNamara, J., *Computer Engineering: A DEC View of Hardware Systems Design*, Digital Press, Bedford, Mass., 1978.

Bell, J., Casasent, D., and Bell, C. G., "An Investigation of Alternative Cache Organizations," *IEEE Trans. on Comp.*, C-23, Apr. 1974, pp. 346–351.

Benes, V. E., *Mathematical Theory of Connecting Networks and Telephone Traffic*, Academic Press, New York, 1965.

Bensoussan, A., Clingen, C. T., and Daley, R. C., "The MULTICS Virtual Memory: Concepts and Design," *Comm. of ACM*, vol. 15, May 1972, pp. 308–315.

Bernstein, A. J., "Analysis of Programs for Parallel Processing," *IEEE Trans. Elec. Comp.*, E-15, Oct. 1966, pp. 746–757.

Berra, P. B., and Oliver, E., "The Role of Associative Array Processors in Database Machine Architecture," *IEEE Comp.*, Mar. 1979, pp. 53–61.

Bhandarkar, D. P., "Analysis of Memory Interference in Multiprocessors," *IEEE Trans. on Comp.*, C-24, Sept. 1975, pp. 897–908.

Bhandarkar, D. P., "Some Performance Issues in Multiprocessor System Design," *IEEE Trans. on Comp.*, C-26, no. 5, May 1977, pp. 506–511.

Blaauw, G., "Computer Architecture," *Electronische Rechenanlagen*, vol. 14, no. 4, 1972, pp. 154–160.

Blaauw, G., *Digital Systems Implementation*, Prentice-Hall, Englewood Cliffs, N.J., 1976.

Bode, A., and Händler, W., *Rechnerarchitektur: Grundlagen und Verfahren*, Springer-Verlag, Berlin (volumes 1 and 2), 1980, 1982.

Borgeson, B. R., Hanson, M. L., and Hartley, P. A., "The Evolution of the Sperry Univac 1100 Series: A History, Analysis, and Projection," *Comm. of ACM*, vol. 21, no. 1, Jan. 1978, pp. 25–43.

Bouknight, W. J., Denenberg, S. A., McIntyre, D. E., Randall, J. M., Sameh, A. H., and Slotnick, D. L., "The Illiac IV System," *Proc. IEEE*, vol. 60, no. 4, Apr. 1972, pp. 369–388.

Bovet, D. P., and Vanneschi, M., "Models and Evaluation of Pipeline Systems," *Computer Architectures and Networks* (Gelenbe and Mahl, eds.), North Holland, Amsterdam, 1976, pp. 99–111.

Brent, R., "The Parallel Evaluation of General Arithmetic Expressions," *Journ. of ACM*, vol. 21, no. 2, Apr. 1974, pp. 201–206.

Briggs, F. A., "Performance of Memory Configurations for Parallel-Pipelined Computers," *Proc. 5th Ann. Symp. Computer Architecture*, Apr. 1978, pp. 202–209.

Briggs, F. A., "Effects of Buffered Memory Requests in Multiprocessor Systems," *Proc. ACM/SIGMETRICS Conf. on Simulation, Measurement and Modeling of Comput. Systems*, 1979, pp. 73–81.

Briggs, F. A., and Davidson, E. S., "Organization of Semiconductor Memories for Parallel-Pipelined Processors, *IEEE Trans. on Comp.*, Feb. 1977, pp. 162–169.

Briggs, F. A., and Dubois, M., "Modeling of Synchronized Iterative Algorithms for Multiprocessors," *Proc. 18th Ann. Allerton Conf. on Communication, Control and Computing*, Oct. 1980, pp. 554–563.

Briggs, F. A., and Dubois, M., "Performance of Cache-Based Multiprocessors," *Proc. ACM/SIGMETRICS Conf. on Measurement and Modeling of Computer Systems*, Sept. 1981.

Briggs, F. A., and Dubois, M., "Effectiveness of Private Caches in Multiprocessor Systems with Parallel-Pipelined Memories," *IEEE Trans. on Comp.*, C-32, no. 1, Jan. 1983, pp. 48–59.

Briggs, F. A., Dubois, M., and Hwang, K., "Throughput Analysis and Configuration Design of a Shared-Resource Multiprocessors Systems: PUMPS," *Proc. 8th Ann. Symp. Computer Architecture*, May 1981, pp. 67–80.

Briggs, F. A., Fu, K. S., Hwang, K., and Patel, J. H., "PM^4: A Reconfigurable Multiprocessor System for Pattern Recognition and Image Processing," *Proc. of NCC, AFIPS*, June 1979, pp. 255–265.

Briggs, F. A., Fu, K. S., Hwang, K., and Wah, B. W., "PUMPS Architecture for Pattern Analysis and Image Database Management," *IEEE Trans. on Comp.*, C-31, no. 10, Oct. 1982, pp. 969–982.

Browning, S. A., "The Tree Machine: A Highly Concurrent Computing Environment," Ph.D. Thesis, Dept. of Computer Science, Cal. Tech., Pasadena, 1980.

Bucher, I. Y., "The Computational Speed of Supercomputers," *Proc. ACM/SIGMETRICS Conf. on Measurement and Modeling of Computer Systems*, Aug. 1983, pp. 151–165.

Bucholz, W., *Planning a Computer System: Project Stretch*, McGraw-Hill, New York, 1962.

Budnik, P. P., and Kuck, D. J., "The Organization and Use of Parallel Memories," *IEEE Trans. on Comp.*, vol. 20, Dec. 1971, pp. 1566–1569.

Burnett, G. J., and Coffman, E. G., "A Study of Interleaved Memory Systems," *Proc. Spring Joint Computer Conf., AFIPS*, SJCC, vol. 36, 1970, pp. 467–474.

Burroughs Co., "BSP: Overview Perspective, and Architecture," document no. 61391, Feb. 1978*a* (30 pages).

Burroughs Co., "BSP: Floating Point Arithmetic," document no. 61416, 1978*b* (27 pages).

Burroughs Co., "BSP: Implementation of FORTRAN," document no. 16391, Nov. 1977 (18 pages).

Buzen, J. P., "I O Subsystem Architecture," *Proc. IEEE, 63*, June 1975, pp. 871–879.

Cappa, M., and Hamacher, V. C., "An Augmented Iterative Array for High-Speed Array Division," *IEEE Trans. on Comp.*, C-22, Feb. 1973, pp. 172–175.

Carlson, W. W., and Hwang, K., "On Structural Data Accessing in Dataflow Computers," *Proc. 1st Int'l. Conf. Computers and Applications*, Beijing, China, June 1984.

Case, R. P., and Padegs, A., "Architecture of the IBM System 370," *Comm. of ACM*, vol. 21, no. 1, 1978, pp. 73–96.

Censier, L. M., and Feautrier, P., "A New Solution to Coherence Problems in Multicache Systems," *IEEE Trans. on Comp.*, C-27, Dec. 1978, pp. 1112–1118.

Chamberlin, D. D., "Parallel Implementation of a Single Assignment Language," *Ph.D. Thesis*, Stanford Univ., Calif., 1971.

Chamberlin, D. D., Fuller, S. H., and Liu, L. Y., "An Analysis of Page Allocation Strategies for Multiprogramming Systems with Virtual Memory," *IBM Journ. of Res. and Dev.*, 1973.

Chandy, K. M., "Models for the Recognition and Scheduling of Parallel Tasks on Multiprocessor Systems," *Bulletin of the Operations Research Society of America*, vol. 23, suppl. 1, Spring 1975, p. B-117.

Chang, D., Kuck, D. J., and Lawrie, D. H., "On the Effective Bandwidth of Parallel Memories," *IEEE Trans. on Comp.*, C-26, no. 5, May 1977, pp. 480–490.

Charlesworth, A. E., "An Approach to Scientific Array Processing: The Architecture Design of the AP-120B/FPS-164 Family," *IEEE Comp.*, Dec. 1981, pp. 12–30.

Chen, N. F., and Liu, C. L., "On a Class of Scheduling Algorithms for Multiprocessor Computing Systems," *Proc. Conf. on Parallel Proc.*, Raquette Lake, N.Y., August 1974.

Chen, S. C., "Speedup of Iterative Programs in Multiprocessor Systems," *Ph.D. Thesis*, Univ. of Ill. at Urb.-Champ., Dept. of Computer Science, no. 75–694, Jan. 1975.

Chen, S. C., "Large-Scale and High-Speed Multiprocessor System for Scientific Applications: Cray X-MP Series," *Proc. NATO Advanced Research Workshop on High-Speed Computing*, J. Kawalik, editor, Springer Verlag, Jülich, W. Germany, June 20–22, 1983.

Chen, T. C., "Parallelism, Pipelining, and Computer Efficiency," *Computer Design*, Jan. 1971, pp. 69–74.

Chen, T. C., "Overlap and Pipeline Processing," in *Introduction to Computer Architecture*, Chap. 9 (Stone, ed.), Science Research Associates, Inc., Chicago, 1980, pp. 427–486.

Chin, C. Y., and Hwang, K., "Connection Principles of Multipath Packet Switching Networks," *Proc. 11th Ann. Symp. Computer Architecture*, Ann Arbor, Mich., June 1984.

Chow, C. K., "On Optimization of Storage Hierarchies," *IBM Journ. of Res. and Dev.*, May 1974, pp. 194–203.

Chu, Y., *High Level Language Computer Architecture*, Academic Press, New York, 1975.

Chu, Y., and Abrams, M., "Programming Languages and Direct-Execution Computer Architecture," *IEEE Comp.*, vol. 14, July 1981, pp. 22–40.

Coffman, E. G., "Bounds on Parallel Processing of Queues with Multiple Jobs," *Naval Research Logical Quarterly*, 14, Sept. 1967, pp. 345–366.

Coffman, E. G., Elphick, M. J., and Shoshani, A., "System Deadlocks," *ACM Computer Surveys*, 3, 1971, pp. 67–78.

Coffman, E. G., and Denning, P. J., *Operating Systems Theory*, Prentice-Hall, Englewood Cliffs, N.J., 1973.

Coffman, E. G., and Graham, R. L., "Optimal Scheduling for Two Processor Systems," *Acta Informatica*, vol. 1, 1972, pp. 200–213.

Coffman, E. G., and Ryan, T. J., Jr., "A Study of Storage Partitioning Using a Mathematical Model of Locality," *Comm. of ACM*, vol. 15, Mar. 1972, pp. 185–190.

Coffman, E. G., ed., *Computer and Job-Shop Scheduling Theory*, John Wiley, New York, 1976.

Cohen, E., and Jefferson, D., "Protection in the Hydra Operating System," *Proc. 5th Symp. on Operating System Principles*, Nov. 1975, pp. 141–160.

Cohen, T., "Structured Flowcharts for Multiprocessing," *Computer Languages*, vol. 13, no. 4, 1978, pp. 209–226.

Connors, W. D., Florkowski, J. H., and Patton, S. K., "The IBM 3033: An Inside Look," *Datamation*, May 1979, pp. 198–218.

Conrad, V., and Wallach, "Iterative Solution of Linear Equations on a Parallel Processor System," *IEEE Trans. on Comp.*, Sept. 1977, pp. 838–847.

Conti, C. J., "Concepts for Buffer Storage," *Computer Group News*, 2, Mar. 1969, pp. 9–13.

Conti, C. J., Gibson, D. H., and Pikowsky, S. H., "Structural Aspects of the System 360/85: General Organization," *IBM Systems Journ.*, 1968, pp. 2–14.

Control Data Corp., *Control Data STAR-100 Features Manual*, St. Paul, Minn., pub. no. 60425500, Oct. 1973.

Control Data Corp., *Control Data STAR-100 FORTRAN Language Version 2 Reference Manual*, St. Paul, Minn., pub. no. 60386200, 1976.

Control Data Corp., *CDC Cyber 200 Operating System 1.4 Reference Manual*, St. Paul, Minn., pub. no. 60457000, vol. 1, 1979*a*.

Control Data Corp., *CDC Cyber 200 Fortran Language 1.4 Reference Manual*, St. Paul, Minn., pub. no. 60456040, 1979*b*.

Control Data Corp., *CDC Cyber 200/Model 205 Technical Description*, St. Paul, Minn., Nov. 1980.

Conway, M., "A Multiprocessor System Design," *Proc. AFIPS Fall Joint Comput. Conf.*, Spartan Books, N.Y., 1963, pp. 139–146.

Cooper, R. G., "The Distributed Pipeline," *IEEE Trans. Comp.*, Nov. 1977, pp. 1123–1132.

Cordennier, V., "A Two Dimension Pipelined Processor for Communication in a Parallel System," *Proc. 1975 Sagamore Comp. Conf. Parallel Proc.*, 1975, pp. 115–121.

Crane, B. A., Gilmartin, M. J., Huttenhoff, J. H., Rus, P. T., and Shively, R. R., "PEPE Computer Architecture," *IEEE Compcon*, 1972, pp. 57–60.

Cray Research, Inc., *CRAY-1 Computer System Hardware Reference Manual*, Bloomington, Minn., pub. no. 2240004, 1977.

Cray Research, Inc., *CRAY-1 Computer System Preliminary CRAY FORTRAN (CFT) Reference Manual*, Bloomington, Minn., pub. no. 2240009, 1978.

Cray Research Inc., *CRAY-1 Fortran (CFT) Reference Manual*, Bloomington, Minn., pub. no. 2240009, Dec. 1979*b*.

Gustafson, R. N., and Sparacio, F. J., "IBM 3081 Processor Unit: Design Considerations and Design Process," *IBM Journ. of Res. and Dev.*, vol. 26, no. 1, Jan. 1982, pp. 12–21.

Daley, R. C., and Dennis, J. B., "Virtual Memory Process and Sharing in Multics," *Comm. of ACM*, vol. 11, May 1968, pp. 306–311.

Datawest Corp., "Real Time Series of Microprogrammable Array Transform Processors," Prod. Bulletin Series B, 1979.

Davidson, E. S., "The Design and Control of Pipelined Function Generators," *Proc. 1971 Int'l. IEEE Conf. on Systems, Networks, and Computers*, Oaxtepec, Mexico, Jan. 1971, pp. 19–21.

Davidson, E. S., "Scheduling for Pipelined Processors," *Proc. 7th Hawaii Conf. on System Sciences*, 1974, pp. 58–60.

Davidson, E. S., Thomas, D. P., Shar, L. E., and Patel, J. H., "Effective Control for Pipelined Computers," *COMPCON Proc.*, IEEE 75CH0920-9C, 1975, pp. 181–184.

Davis, A. L., "The Architecture and System Methodology of DDM1: A Recursively Structured Data Driven Machine," *Proc. 5th Ann. Symp. on Computer Architecture*, 1978, pp. 210–215.

Davis, C. G., and Vouch, R. L., "Ballistic Missile Defense: A Supercomputer Challenge," *IEEE Comp.*, Nov. 1980, pp. 37–46.

Deitel, H. M., *An Introduction to Operating Systems*, Addison-Wesley, Reading, Mass. 1984.

Deminet, J., "Experience with Multiprocessor Algorithms," *IEEE Trans. on Comp.*, C-31, Apr. 1982, pp. 278–288.

Denelcor, Inc., *Heterogeneous Element Processor: Principles of Operation*, April 1981.

Denning, P. J., "The Working Set Model for Program Behavior," *Comm. of ACM*, vol. 11, no. 5, 1968, pp. 323–333.

Denning, P. J., "Operating Systems Principles for Data Flow Networks," *IEEE Comp.*, July 1978, pp. 86–96.

Denning, P. J., "Working Sets Past and Present," *IEEE Trans. on Soft. Eng.*, SE-6, no. 1, Jan. 1980.

Denning, P. J., "Virtual Memory," *ACM Computing Surveys*, 2, Sept. 1970, pp. 153–189.

Denning, P. J., and Graham, G. S., "Multiprogrammed Memory Management," *Proc. IEEE*, vol. 63, June 1975, pp. 924–939.

Denning, P. J., and Schwartz, S. C., "Properties of the Working Set Model," *Comm. of ACM*, vol. 15, 1972.

Dennis, J. B., "Data Flow Supercomputers," *IEEE Comp.*, Nov. 1980, pp. 48–56.

Dennis, J. B., "First Version of a Data Flow Procedure Language," in *Lecture Notes in Computer Science*, 19, Springer-Verlag, Berlin, 1974, pp. 362–376.

Dennis, J. B., Leung, C. K., and Misunas, D. P., "A Highly Parallel Processor Using a Data Flow Machine Language," *CSG Memo 134-1*, Lab. for Computer Science, MIT, June 1979.

Dennis, J. B., and Misunas, D. P., "A Preliminary Architecture for a Basic Data Flow Processor," *Proc. Second Ann. Symp. on Computer Architecture*, IEEE, Jan. 1975, pp. 126–132.

Dennis, J., and Rong, G., "Maximum Pipelining of Array Operations on Static Dataflow Machine," *Proc. 1983 Int'l. Conf. Parallel Proc.*, August 23–26, 1983.

Dennis, J. B., and Weng, K., "Application of Dataflow Computation to the Weather Problem," *High Speed Computer and Algorithm Organization*, Kuck, et al., eds., New York: Academic Press, New York, 1977, pp. 143–157.

Despain, A. M., and Patterson, D. A., "X-tree—A Tree Structured Multiprocessor Computer Architecture," *Proc. 5th Ann. Symp. on Computer Architecture*, 1978, pp. 144–151.

Dias, D. M., and Jump, J. R., "Analysis and Simulation of Buffered Delta Networks," *IEEE Trans. on Comp.*, C-30, Apr. 1981*a*, pp. 273–282.

Dias, D. M., and Jump, J. R., "Packet Switching Interconnection Networks for Modular Systems," *IEEE Comp.*, Dec. 1981*b*, pp. 43–53.

Dijkstra, E. W., "Solution of a Problem in Concurrent Programming," *Comm. of ACM*, vol. 8, Sept. 1965, pp. 569–570.

Dijkstra, E. W., "Cooperating Sequential Processes," *Programming Languages*, F. Genuys, ed., Academic Press, New York, 1968, pp. 43–112.

Dorr, F. W., "The Cray-1 at Los Alamos," *Datamation*, Oct. 1978, pp. 113–120.

Dowsing, R. D., "Processor Management in a Multiprocessor System," *Electronic Letters*, vol. 12, no. 24, Nov. 1976.

Dubois, M., "Analytical Methodologies for the Evaluation of Multiprocessing Structures," *Ph.D. Thesis*, Purdue Univ., Ind., 1982.

Dubois, M., and Briggs, F. A., "Effects of Cache Coherency in Multiprocessors," *IEEE Trans. on Comp.*, C-31, no. 11, Nov. 1982*a*.

Dubois, M., and Briggs, F. A., "Performance of Synchronized Iterative Processes in Multiprocessor Systems," *IEEE Trans. on Soft. Eng.*, July 1982*b*, pp. 419–431.

Duff, M. J. B., ed., *Computing Structures for Image Processing*, Academic Press, London, 1983.

El-Ayat, K. A., "The Intel 8089: An Integrated I/O Processor," *IEEE Comp.*, vol. 12, no. 6, June 1979, pp. 67–78.

Emer, J. S., and Davidson, E. S., "Control Store Organization for Multiple Stream Pipelined Processors," *Proc. 1978 Int'l. Conf. Parallel Proc.*, 1978, pp. 43–48.

Enslow, P. H., "Multiprocessor Organization," *Computing Surveys*, vol. 9, Mar. 1977, pp. 103–129.

Enslow, P. H., ed., *Multiprocessors and Parallel Processing*, Wiley-Interscience, New York, 1974.

Evans, D. J., ed., *Parallel Processing Systems*, Cambridge Univ. Press, England, 1982.

Evensen, A. J., and Troy, J. L., "Introduction to the Architecture of a 288-Element PEPE," *Proc. Sagamore Conf. Parallel Proc.*, 1973, pp. 162–169.

Fabry, R. S., "Capability-based Addressing," *Comm. of ACM*, vol. 17, July 1974, pp. 403–412.

Faggin, F., "How VLSI Impacts Computer Architecture," *IEEE Spectrum*, 15, May 1978, pp. 28–31.

Fairbairn, D. G., "VLSI: A New Frontier for System Designers," *IEEE Comp.*, Jan. 1982, pp. 87–96.

Feierbach, G., and Stevenson, D. K., "The Phoenix Array Processing System," *Phoenix Project Memo. 7*, NASA Ames Research Center, Mountain View, Calif., Nov. 1978.

Feldman, J. D., and Fulmer, L. C., "RADCAP:- Operational Parallel Processing Facility," *Proc. Nat'l Comp. Conf.*, AFIPS, 1974, pp. 7–15.

Feller, W., *An Introduction to Probability Theory and its Applications*, vol. 1, Wiley, New York, 1970.

Femt, T. Y., "Some Characteristics of Associative Parallel Processing," *Proc. 1972 Sagamore Comp. Conf.*, Syracuse Univ., 1972, pp. 5–16.

Feng, T. Y., "Data Manipulation Functions in Parallel Processors and Their Implementations," *IEEE Trans. on Comp.*, C-23, no. 3, Mar. 1974, pp. 309–318.

Feng, T. Y., ed., "Parallel Processors and Processing," special issue, *ACM Computing Surveys*, vol. 9, no. 1, Mar. 1977*a*.

Feng, T. Y., "Parallel Processors and Processing," *Class Notes*, Wayne State Univ., Detroit, Michigan (unpublished), 1977*b*.

Feng, T. Y., "A Survey of Interconnection Networks," *IEEE Comp.*, Dec. 1981, pp. 12–27.

Fennell, K. D., and Lesser, V. R., "Parallelism in Artificial Intelligence Problem Solving: A Case Study of Hearsay II," *IEEE Trans. on Comp.*, Mar. 1977, pp. 98–111.

Ferrari, D., "An Analytic Study of Memory Allocation in Multiprocessing System," *Computer Architecture and Networks*, Gelenbe and Mahl, eds., North-Holland, Amsterdam, 1974.

Ferrari, D., Gelenbe, E., and Mahl, R., "An Analytic Study of Memory Allocation in Multiprocessor Systems," *Proc. Conf. on Computer Architecture and Networks*, France, August 1974.

Floating Point System, Inc., *AP-120B Processor Handbook*, Portland, Oregon, pub. no. 7259-02, May 1976.

Flynn, M. J., "Very High-Speed Computing Systems" *Proc. IEEE*, vol. 54, 1966, pp. 1901–1909.

Flynn, M. J., "Some Computer Organization and Their Effectiveness," *IEEE Trans. on Comp.*, C-21, no. 9, Sept. 1972, pp. 948–960.

Flynn, M. J., "The Interpretive Interface: Resources and Program Representation in Computer Organization," *High Speed Computer and Algorithm Organization*, Kuck et al., Academic Press, New York, 1977, pp. 41–69.

Flynn, M. J., and Amdahl, G. M., "Engineering Aspects of Large High Speed Computer Design," *Proc. Symp. Microelectronics and Large Systems*, Spartan Press, Washington, D.C., 1965, pp. 77–95.

Flynn, M. J., Podvin, A., and Shmizu, K., "A Multiple Instruction Stream with Shared Resources," *Parallel Processor Systems, Technologies, and Applications*, Hobbs, ed., Spartan Books, Washington, D.C., 1970, pp. 251–286.

Fontao, R. O., "A Concurrent Algorithm for Avoiding Deadlocks in Multiprocess Multiple Resonance Systems," *Proc. 3d Symp. Operating System Principles*, Oct. 1971.

Foster, C. C. (1976). *Content-Addressable Parallel Processors*, Van Nostrand Reinhold Co., New York, 1976.

Franta, W. R., and Houle, P. A., "Comments on Models of Multiprocessor Multi-Memory Bank Computer Systems," *Proc. 1974 Winter Simulation Conf.*, vol. I, Washington, D.C., Jan. 1974.

Fritsch, G., Kleinoeder, W., Linster, C. U., and Volkert, J., "EMSY 85: The Erlangen Multiprocessor System for a Broad Spectrum of Applications," *Proc. 1983 Int'l. Conf. on Parallel Proc.*, August 1983, pp. 325–330.

Fuller, S. H., and Harbison, S. P., *The C.mmp Multiprocessor*, Technical Report, Carnegie-Mellon Univ., Computer Science Dept., 1978.

Fuller, S. H., Swan, R., and Wulf, W. A., "The Instrumentation of C.mmp: A Multi-miniprocessor," *IEEE Compcon*, 1973.

Gajski, D. D., "An Algorithm for Solving Linear Recurrence Systems on Parallel and Pipelined Machines," *IEEE Trans. on Comp.*, Mar. 1981, pp. 190–205.

Gakski, D. D., Kuck, D. J., and Padua, D. A., "Dependence Driven Computation," *Proc. COMCON Spring*, Feb. 1981, pp. 168–172.

Gajski, D., Kuck, D., Lawrie, D., and Sameh, A., "Cedar—A Large Scale Multiprocessor," *Proc. 1983 Int'l. Conf. on Parallel Proc.*, Aug. 1983, pp. 524–529.

Gajski, D. D., Panda, D. A., Kuck, D. J., and Kuhn, R. H., "A Second Opinion on Dataflow Machines and Languages," *IEEE Comp.*, Feb. 1982, pp. 58–70.

Gajski, D. D., and Rubinfield, L. P., "Design of Arithmetic Elements for Burroughs Scientific Processor," *Proc. 4th Symp. Computer Arithmetic*, Oct. 1978, pp. 245–256.

Gao, Q. S., and Zhang, X., "Cellular Vector Computer of Vertical and Horizontal Processing with Vertical Common Memory," *Journ. of Computers*, no. 1, Jan. 1979, pp. 1–12 (in Chinese).

Gao, Q. S., and Zhang, X., "Another Approach to Making Supercomputer by Microprocessors—Cellular Vector Computer of Vertical and Horizontal Processing with Virtual Common Memory," *Int. Conf. Parallel Proc.*, Aug. 1980, pp. 163–164.

Gaudet, G., and Stevenson, D., "Optimal Sorting Algorithms for Parallel Computers," *IEEE Trans. on Comp.*, C-27, Jan. 1978, pp. 84–87.

Geesei, J., and Lukes, J. A., "A Model for the Evaluation of Storage Hierarchies," *IBM Systems Journ.*, no. 2, 1974, pp. 163–178.

Ginsberg, M., "Some Numerical Effects of A FORTRAN Vectorizing Compiler on A Texas Instruments Advanced Scientific Computer," *High Speed Computer and Algorithm Organization*, Kuck, et al., eds., Academic Press, New York, 1977, pp. 461–62.

Goke, R., and Lipovski, G. J., "Banyan Networks, for Partitioning on Multiprocessor Systems," *Proc. 1st Ann. Symp. Computer Architecture*, 1973, pp. 21–30.

Gonzalez, M. J., "Deterministic Processor Scheduling," *Computing Surveys*, vol. 9, no. 3, Sept. 1977, pp. 173–204.

Gonzalez, M. J., and Ramamoorthy, C. V., "Recognition and Representation of Parallel Processable Streams in Computer Programs," in *Parallel Processor Systems*, Technologies and Applications, Macmillan Ltd., London, England, 1970.

Gonzalez, M. J., and Ramamoorthy, C. V., "Parallel Task Execution in a Decentralized System," *IEEE Trans. on Comp.*, C-21, Dec. 1972, 1310–1322.

Gonzalez, T., and Sahni, S., "Preemptive Scheduling of Uniform Processor Systems," *Journ. of ACM*, vol. 25, no. 1, Jan. 1978, pp. 92–101.

Goodman, J. R. "An Investigation of Multiprocessor Structures and Algorithms for Database Management," *UCB/ERL M81/83*, Dept. of EECS, Univ. of Calif., Berkeley, 1981.

Goodyeàr Aerospace Co., "Massively Parallel Processor (MPP)," Tech. Report GER-16684, July 1979.

Gosden, J. A., "Explicit Parallel Processing Description and Control in Programs for Multi and Uni-processor Computers," *AFIPS Fall Joint Comput. Conf.*, Spartan Books, N.Y., 1966, pp. 651–660.

Gostelow, K. P., and Thomas, R. E., "Performance of a Simulatec Dataflow Computer," *IEEE Trans. on Comp.*, Oct. 1980, pp. 905–919.

Gottlieb, A., Grishman, R., Kruskal, C. P., McAaliffe, K. P., Randolph, L., and Snir, M., "The NYU Ultracomputer-Designing an MIMD Shared Memory Parallel Computer," *IEEE Trans. on Comp.*, Feb. 1983, pp. 175–189.

Graham, G. S., A Study of Program and Memory Policy Behavior, *Ph.D. Thesis*, Purdue Univ., Ind., 1976.

Graham, R. L., "Bounds on Multiprocessing Anomalies and Packing Algorithms," *Proc. AFIPS 1972 Spring Joint Comp. Conf.*, 40, AFIPS Press, Montvale, N.J., 1972, pp. 205–217.

Graham, W. R., "The Parallel and the Pipeline Computers," *Datamation*, Apr. 1970, pp. 68–71.

Grimsdale, R. L., and Johnson, D. M., "A Modular Executive for Multiprocessor Systems," *Proc. Conf. on Trends in One-Line Computer Control Systems*, Sheffield, England, Apr. 1972.

Grinbert, J., Nudd, G. R., and Etchella, R. D., "A Cellular VLSI Architecture," *IEEE Comp.*, Jan. 1984.

Grohoski, G. R., and Patel, J. H., "A Performance Model for Instruction Prefetch in Pipelined Instruction Units," *Proc. 1982 Int'l. Conf. Parallel Proc.*, August 24–27, 1982, pp. 248–252.

Gula, J. L., "Operating System Considerations for Multiprocessor Architecture," *Proc. 7th Texas Conf. on Computing Systems*, Houston, Nov. 1978.

Gurd, J., and Watson, I., "Data Driven System for High Speed Parallel Computing," *Computer Design*, Parts I & II, June & July 1980.

Habermann, A. N., *Introduction to Operating System Design*, Science Res. Assoc., 1976.

Hallin, T. G., and Flynn, M. J., "Pipelining of Arithmetic Functions," *IEEE Trans. on Comp.*, Aug. 1972, pp. 880–886.

Händler, W., "The Impact of Classification Schemes on Computer Architecture," *Proc. 1977 Int. Conf. on Parallel Proc.*, pp. 7–15.

Hansen, P. B., "The Programming Language Concurrent Pascal," *IEEE Trans. on Soft. Eng.*, *1*, 2, June 1975, pp. 199–207.

Hansen, P. B., *Concurrent Pascal*, Prentice-Hall, New York, 1978.

Hansen, P. B., *The Architecture of Concurrent Programs*, Prentice-Hall, Englewood Cliffs, N.J., 1977.

Harris, J. A., and Smith, D. R., "Hierarchical Multiprocessor Organizations," *Proc. 4th Symp. on Computer Architecture*, 1977.

Hayes, J. P., *Computer Architecture and Organization*, McGraw-Hill, New York, 1978.

Hedlund, K. S., "Wafer Scale Integration of Parallel Processors," Ph.D. Thesis, Comp. Science Dept., Purdue Univ., Ind., 1982.

Hellerman, H., *Digital Computer System Principles*, McGraw-Hill, New York, 1967, pp. 228–229.

Hellerman, H., and Smith, H. J., Jr., "Throughput Analysis of Some Idealized Input, Output, and Compute Overlap Configurations," *Computing Surveys*, *2*, June 1970, pp. 111–118.

Higbie, L. C., "Applications of Vector Processing," *Computer Design*, Apr. 1978, pp. 139–145.

Higbie, L. C., "Supercomputer Architecture," *IEEE Comp.*, 6, Dec. 1973, pp. 48–58.

Hintz, R. G., and Tate, D. P., "Control Data STAR-100 Processor Design," *COMPCON Proc.*, Sept. 1972, pp. 1–4.

Hoare, C. A. R., "Towards a Theory of Parallel Programming," *Operating Systems Techniques*, C. A. R. Hoare, ed., Academic Press, New York, 1972.

Hoare, C. A. R., "Monitors: An Operating System Structuring Concept," *Comm. of ACM*, vol. 17, no. 10, Oct. 1974, pp. 549–557.

Hockney, R. W., and Jesshope, C. R., *Parallel Computers: Architecture, Programming and Algorithms*, Adam Hilger Ltd., Bristol, England, 1981.

Holley, L. H., Parmlee, R. P., et al., "VM/370 Asymmetric Multiprocessing," *IBM Systems Journ.*, vol. 18, no. 1, 1979.

Holt, R. C., "Some Deadlock Properties of Computer Systems," *ACM Computing Surveys*, 4, Sept. 1972, 179–195.

Holt, R. C., Graham, G. S., Lazowska, E. D., and Scott, M. A., *Structured Concurrent Programming with Operating Systems Applications*, Addison-Wesley, Mass., 1978.

Hon, R., and Reddy, D. R., "The Effect of Computer Architecture on Algorithm Decomposition and Performance," *High-Speed Computers and Algorithm Organization*, Kuck, et al., ed., Academic Press, New York, 1977, pp. 411–421.

Hoogendoorn, C. H., "A General Model for Memory Interference in Multiprocessors," *IEEE Trans. on Comp.*, C-26, no. 10, Oct. 1977*a*, pp. 998–1005.

Hoogendoorn, C. H., "Reduction of Memory Interference in Multiprocessor Systems," *Proc. 4th Ann. Symp. on Computer Architecture*, Silver Springs, MD. Mar. 1977*b*, pp. 179–183.

Hsiao, D. K., "Data Base Computers," in *Advances in Computers*, vol. 19, Yovits, ed., Academic Press, New York, 1980, pp. 1–64.

Hsiao, D. K., ed., *Advanced Database Machine Architecture*, Prentice-Hall, Englewood Cliffs, N.J., 1983.

Hu, T. C., "Parallel Sequencing and Assembly Line Problems," *Oper. Res.*, vol. 9, no. 6, Nov.-Dec., 1961, pp. 841–848.

Hufnagel, S., "Comparison of Selected Array Processor Architecture," *Computer Design*, Mar. 1979, pp. 151–158.

Hwang, K., "Fault-Tolerant Microprogrammed Digital Controller Design," *IEEE Trans. on Industrial Electronics and Control Instrumentation*, Aug. 1976, pp. 200–207.

Hwang, K., "Global and Modular Two's Complement Array Multipliers," *IEEE Trans. on Comp.*, Apr. 1979*a*, pp. 300–306.

Hwang, K., *Computer Arithmetic: Principles, Architecture and Design*, Wiley, New York, 1979*b*.

Hwang, K., "VLSI Computer Arithmetic for Real-Time Image Processing," Chap. 7, *VLSI Electronics: Microstructure Science*, vol. 7, Einpruch, ed., Academic Press, New York, 1984.

Hwang, K., and Chang, T. P., "Combinatorial Reliability Analysis of Multiprocessor Computers," *IEEE Trans. Reliability*, vol. R-31, no. 5, Dec. 1982, pp. 469–473.

Hwang, K., and Cheng, Y. H., "Partitioned Matrix Algorithms for VLSI Arithmetic Systems," *IEEE Trans. on Comp.*, C-31, no. 12, Dec. 1982, pp. 1215–1224.

Hwang, K., Chin, C. Y., and Ni., L. M., "Adaptive Path-Directed Routing for Packet Switched Computer Networks," *TR-EE 83-37*, Purdue Univ., Ind., 1983.

Hwang, K., and Fu, S. K., "Integrated Computer Architectures for Image Processing and Database Management," *IEEE Comp.*, vol. 16, no. 1, Jan. 1983, pp. 51–61.

Hwang, K., and Kuhn, R. H., eds. *Tutorial on Supercomputers Design and Applications*, IEEE Computer Society Press (in press).

Hwang, K., and Ni, L. M., "Resource Optimization of a Parallel Computer for Multiple Vector Processing," *IEEE Trans. on Comp.*, C-29, Sept. 1980, pp. 831–836.

Hwang, K., and Su., S. P., "VLSI Architectures of Feature Extraction and Pattern Classification," *Computer Vision, Graphics, and Image Processing*, vol. 24, Academic Press, New York, Nov. 1983*a*, pp. 215–228.

Hwang, K., and Su, S. P., "Priority Scheduling in Event-Driven Dataflow Computers," *TR-EE 83-56*, Purdue Univ., Ind. Dec. 1983*b*.

Hwang, K., and Su, S. P., "Multitask Scheduling in Vector Supercomputers," *TR-EE 83-52*, Purdue Univ., Ind., Dec. 1983*c*.

Hwang, K., Su, S. P., and Ni, L. M., "Vector Computer Architecture and Processing Techniques," *Advanced in Computers*, vol. 20, Yovits, ed., Academic Press, New York, 1981, pp. 115–197.

Hwang, K., and Yao, S. B., "Optimal Batched Searching of Tree-Structural Files in Multiprocess Computer System," *Journ. of Assoc. of Comp. Mach.*, vol. 24, no. 3, July 1977, pp. 441–454.

IBM Corp., *IBM System/360 and System/370 I/O Interface Channel to Control Unit*, form GA22-6974-3, 1976.

IBM Corp., *IBM 3838 Array Processor Functional Characteristics*, no. 6A24-3639-0, file no. S370-08, Endicott, N.Y., Oct. 1976.

IBM Corp., *IBM System/370 Model 168 Functional Characteristics*, form no. GA22-7010-4, 1976.

IBM Corp., *3033 Processor Complex Theory of Operation/Diagrams Manual*, vols. 1–5, SY22-7001 through SY22-7005, Jan. 1978.

IBM Corp., "Special Issue on IBM 3081," *IBM Journ. of Res. and Dev.*, vol. 26, no. 1, Jan. 1982, pp. 2–29.

IBM Corp., *System/370 Principles of Operation*, GA22-7000-4, 1974.

Isloor, S. S., and Marsland, T. A., "The Deadlock Problem: An Overview," *IEEE Computer*, vol. 13, no. 9, Sept. 1980.

Jain, N., *Performance Study of Synchronization Mechanisms in a Multiprocessor, Ph.D. Thesis*, Carnegie-Mellon Univ., 1979.

Jensen, J. E., and Baer, J. L., "A Model of Interference in a Shared Resource Multiprocessor," *Proc. 3d Ann. Symp. on Computer Architecture*, Clearwater, Fla., Jan. 1976, pp. 52–57.

Jin, L., "A New General-Purpose Distributed Multiprocessor Structure," *Proc. Int'l. Conf. on Parallel Proc.*, Aug. 1980, pp. 153–154.

Johnson, L., "Gaussian Elimination on Sparse Matrices and Concurrency," *Tech. Report 4087 : TR:80*, Dept. of Computer Science, Cal. Tech., Pasadena, 1980.

Jones, A. K., and Gehringer, E. F. (Editor), "Cm* Multiprocessor Project: A Research Review," *Tech. Rept. CMU-CS-80-131*, Carnegie-Mellon Univ., July 1980.

Jones, A. K., and Schwarz, P., "Experience Using Multiprocessor Systems: A Status Report," Dept. of Computer Science, Carnegie-Mellon Univ., Tech. Report CMU-CS-79-146, Oct. 1979.

Jordan, H. F., "Performance Measurement of HEP-A Pipelined MIMD Computer," *Proc. 10th Ann. Symp. Computer Architecture*, June 1983, pp. 207–212.

Jordan, H. F., Scalabrin, M., and Calvert, W., "A Comparison of Three Types of Multiprocessor Algorithms," *Proc. 1979 Int'l. Conf. on Parallel Proc.*, Bellaire, MI, Aug. 1979, pp. 231–238.

Jump, J. R., and Ahuja, S. R., "Effective Pipelining of Digital Systems," *IEEE Trans. on Comp.*, Sept. 1978, pp. 855–865.

Kaplan, K. R., and Winder, R. V., "Cache-Based Computer Systems," *Computer*, 6, Mar. 1973, 30–36.

Karp, K. M., and Miller, R. E., "Properties of a Model for Parallel Computations: Determinancy, Terminating, Queueing," *SIAM Journal of Applied Mathematics*, vol. 24, Nov. 1966, pp. 1390–1411

Karplus, W. J., and Cohen, D., "Architectural and Software Issues in the Design and Application of Peripheral Array Processors," *IEEE Comp.*, Sep. 1981, pp. 11–17.

Kartashev, S. I., and Kartashev, S. P., "Problems of Designing Supersystems with Dynamic Architectures," *IEEE Trans. on Comp.*, Dec. 1980, pp. 1114–1132.

Kascic, M. J., *Vector Processing on the Cyber 200*, Control Data Corp, 1979 (38 pages).

Katzan, H., *Computer Organization and the System/360*, Van Nostrand Reinhold, New York, 1971.

Kaufman, M., "An Almost-optimal Algorithm for the Assembly-line Scheduling Problem," *IEEE Trans. on Comp.*, C-23, Nov. 1974, pp. 1169–1174.

Keller, R. M., "Look-Ahead Processors," *ACM Computing Surveys*, vol. 7, no. 4, Dec. 1975, pp. 177–195.

Keller, R. M., Patil, S. S., and Lindstrom, G., "A Loosely Coupled Applicative Multiprocessing System," *Proc. Nat'l. Computer Conf.*, AFIHS Press, 1979.

Kennedy, K., "Optimization of Vector Operations in an Extended Fortran Compiler," *IBM Research Report*, RC-7784, 1979.

Kinney, L. L., and Arnold, R. G., "Analysis of a Multiprocessor System with a Shared Bus," *Proc. 5th Ann. Symp. on Computer Architecture*, Palo Alto, CA, Apr. 1978, pp. 89–95.

Kleinrock, L. *Queueing Systems: Theory and Applications*, Wiley, New York, 1975.

Knuth, D. E., and Rao, G. S., "Activity in Interleaved Memory," *IEEE Trans. on Comp.*, C-24, no. 9, Sept. 1975, pp. 943–944.

Kober, R., and Kuznia, C., "SMS—A Multiprocessor Architecture for High-Speed Numerical Calculations," *Proc. Int'l. Conf. Parallel Proc.*, 1978, pp. 18–23.

Kogge, P. M., "The Microprogramming of Pipelined Processors," *Proc. 4th Ann. Conf. Computer Architecture*, IEEE no. 77CH 1182-5C, Mar. 1977*a*, pp. 63–69.

Kogge, P. M., "Algorithm Development for Pipelined Processors," *Proc. 1977 Int'l. Conf. Parallel Proc.*, IEEE no. 77 CH1253-4C, Aug. 1977*b*, p. 217.

Kogge, P. M., *The Architecture of Pipelined Computers*, McGraw-Hill, New York, 1981.

Kogge, P. M., and Stone, H. S., "A Parallel Algorithm for the Efficient Solution of a General Class of Recurrence Equations," *IEEE Trans. on Comp.*, C-22, 1973, pp. 786–793.

Kosinski, P. R., "A Data Flow Programming Language," *Report RC4264*, IBM, T. J. Watson Research Center, Yorktown Heights, N.Y., Mar. 1973.

Kozdrowicki, E. W., and Theis, D. J., "Second Generation of Vector Supercomputers," *IEEE Computer*, Nov. 1980, pp. 71–83.

Kraley, M. F., "The Pluribus Multiprocessor," *Digest of Papers, 1975 Int'l. Symp. on Fault-Tolerant Computing*, Paris, France, June 1975, p. 251.

Kuck, D. J., "Parallel Processing of Ordinary Programs," in *Advances in Computers*, vol. 15, Rubinoff and Yovits, eds., Academic Press, New York, 1976, pp. 119–179.

Kuck, D. J., "Illiac IV Software and Application Programming," *IEEE Trans. on Comp.* Aug. 1968, pp. 746–757.

Kuck, D. J., "A Survey of Parallel Machine Organization and Programming," *ACM Computing Surveys*, vol. 9, no. 1, Mar. 1977, pp. 29–59.

Kuck, D. J., *The Structure of Computers and Computations*, vol. 1, Wiley, New York, 1978.

Kuck, D. J., Kuhn, R. H., Padua, D. A., Leasure, B., and Wolfe, M., "Dependence Graphs and Compiler Optimizations," *Proc. 8th ACM Symp. Principles Programming Languages*, Jan. 1981, pp. 207–218.

Kuck, D. J., Lawrie, D. H., and Sameh, A. H., eds. *High Speed Computer and Algorithm Organization*, Academic Press, New York, 1977.

Kuck, D. J., and Stokes, R. A., "The Burroughs Scientific Processor (BSP)" *IEEE Trans. on Comp.*, C-31, no. 5, May 1982, pp. 363–376.

Kuhn, R. H., "Optimization and Interconnection Complexity for: Parallel Processors, Single-Stage Networks, and Decision Trees," *Ph.D. Thesis*, Univ. of Ill. at Urb-Champ., Dep. of Computer Science, no. 80-1009, Feb. 1980.

Kuhn, R. H., and Padau, D. A., eds., *Tutorial on Parallel Processing*, IEEE Computer Society Press, order no. 367, Los Angeles, 1981.

Kulisch, U. W., and Miranker, W. L., eds., *A New Approach to Scientific Computation*, Academic Press, New York, 1983.

Kung, H. T., "Synchronized and Asynchronous Parallel Algorithms for Multiprocessors," *Algorithms and Complexity: Recent Results and New Directions*, Traub, ed., Addison-Wesley, 1976.

Kung, H. T., "The Structure of Parallel Algorithms," *Advances in Computers*, vol. 19, Yovits, ed., Academic Press, New York, 1980, pp. 65–112.

Kung, H. T., "Why Systolic Architectures," *IEEE Comp.*, Jan. 1982, pp. 37–46.

Kung, H. T., and Leiserson, C. E., "Systolic Arrays (for VLSI)," *Spare Matrix Proc.*, Duff, et al., eds., Society of Indust. and Appl. Math., Philadelphia, Pa., 1978, pp. 245–282.

Kung, S. Y., Arun, K. S., Galezer, R. J., Rao, D. V. B., "Wavefront Array Processor: Language, Architecture, and Applications," *IEEE Trans. on Comp.* C-31, no. 11, Nov. 1982, pp. 1054–1066.

Kurinckx, A., and Pujolle, G., "Analytic Methods for Multiprocessor Modeling," *4th Int'l. Symp. on Modeling and Performance Evaluation of Computer Systems*, Part II, Vienna, Austria, Feb. 1979.

Kurtzberg, J. M., "On the Memory Conflict Problem in Multiprocessor Systems," *IEEE Trans. on Comp.*, C-23, no. 3, Mar. 1974, pp. 286–293.

Lamport, L., "A New Solution of Dijkstra's Concurrent Programming Problem," *Comm. of ACM*, vol. 17, Aug. 1974, pp. 453–454.

Lamport, L., "The Synchronization of Independent Processes," *Acta Informatica*, vol. 7, no. 1, 1976, pp. 15–34.

Lamport, L., "Proving the Correctness of Multiprocess Programs," *IEEE Trans. on Soft. Eng.*, SE-3, no. 2, Mar. 1977, pp. 125–143.

Lampson, B. W., "Dynamic Protection Structures," *1969 Fall Joint Computer Conference*, AFIPS Press, 1969, pp. 27–38.

Lampson, B. W., "Protection," *Operating Systems Review* 8(1), Jan. 1974.

Lampson, B. W., and Sturgis, H. E., "Reflections on an Operating System Design," *Comm. of ACM*, vol. 19, May 1976, pp. 251–265.

Lane, W. G., "Input/Output Processing," *Introduction to Computer Architecture*, Stone, ed., SRA Inc., 1978, pp. 275–316.

Lang, D. E., Agerwala, T. K., and Chandy, K. M., "A Modeling Approach and Design Tool for Pipelined Central Processors," *Proc. 6th Ann. Symp. on Computer Architecture*, Apr. 1979, pp. 122–129.

Lang, T., and Stone, H. S., "A Shuffle-Exchange Network with Simplified Control," *IEEE Trans. on Comp.*, C-25, Jan. 1976, pp. 55–56.

Larson, A. G., "Cost-Effective Processor Design with an Application to Fast Fourier Transform Computers," Ph.D. Thesis, Stanford Univ., 1973.

Larson, A. G., and Davidson, E. S., "Cost-Effective Design of Special-Purpose Processors: A Fast Fourier Transform Case Study," *Proc. 11th Allerton Conf.*, 1973, pp. 547–557.

Lawrence Livermore Laboratory. "The S-1 Project: *Annual Reports*," vol. 1 Architecture, vol. 2 Hardware, and vol. 3 Software, UCID-18619, Univ. of Calif., Livermore, 1979.

Lawrie, D. H., "Access and Alignment of Data in an Array Processor," *IEEE Trans. on Comp.*, C-24, no. 12, Dec. 1975, pp. 1145–1155.

Lawrie, D. H., Layman, T., Baer, D., and Randal, J. M., "Glypnir—A Programming Language for ILLIAC IV," *Comm. of ACM*, vol. 18, Mar. 1975, pp. 157–164.

Lawrie, D. H., and Vora, C. R., "The Prime Memory System for Array Access," *IEEE Trans. on Comp.*, C-31, no. 5, Oct. 1982, pp. 435–442.

Lee, R. B-L., "Empirical Results on the Speed, Efficiency, Redundancy and Quality of Parallel Computations," *Int'l. Conf. Parallel Proc.*, Aug. 1980, pp. 91–96.

Levy, H. M., *Capability-Based Computer Systems*, Digital Press, 1983.

Levy, H. M., and Eckhouse, R. H., Jr., *Computer Programming and Architecture—The Vax-11*, Digital Press, 1980.

Li, H. F., "Scheduling Trees in Parallel Pipelined Processing Environments," *IEEE Trans. on Comp.*, Nov. 1977, pp. 1101–1112.

Lincoln, N. R., "Technology and Design Trade Offs in the Creation of a Modern Supercomputer," *IEEE Trans. on Comp.*, C-31, no. 5, May 1982, pp. 363–376.

Lint, B., and Agerwala, T., "Communication Issues in the Design and Analysis of Parallel Algorithms," *IEEE Trans. on Soft. Eng.*, SE-7, no. 2, Mar. 1981, pp. 174–188.

Lipovski, G. J., and Malek, M., "A Theory for Multicomputer Interconnection Networks," *Tech. Report TRAC-40*, Univ. of Texas, Austin, Mar. 1981.

Lipovski, G. J., and Tripathi, A., "A Reconfigurable Varistructured Array Processor," *Proc. 1977 Int'l. Conf. on Parallel Proc.*, 1977, pp. 165–174.

Liptay, J. S., "Structural Aspects of System 360/85; The Cache," *IBM Systems Journal*, 7, 1969, pp. 15–21.

Liu, J. W. S., and Liu, C. L., "Bounds on Scheduling Algorithms for Heterogeneous Computing Systems," *Proc. IFIP Congress* 74, 1974, pp. 349–353.

Liu, J. W. S., and Liu, C. L., "Performance Analysis of Multiprocessor Systems Containing Functionally Dedicated Processors," *Acta Informatica*, vol. 10, no. 1, 1978, pp. 95–104.

Loomis, H. H., "The Maximum Rate Accumulator," *IEEE Trans. on Comp.*, vol. EC-15, no. 4, Aug. 1966, pp. 628–639.

Lorin, H. (1972). *Parallelism in Hardware and Software*, Prentice-Hall, Englewood Cliffs, N.J., 1972.

Madnick, S. E., and Donovan, J. J., *Operating Systems*, McGraw-Hill, New York, 1974.

Majithia, J. C., "Cellular Array for Extraction of Squares and Square Roots of Binary Numbers," *IEEE Trans. on Comp.*, C-20, no. 12, Dec. 1970, pp. 1617–1618.

Marathe, M., and Fuller, S. H., "A Study of Multiprocessor Contention for Shared Data in C.mmp.," *ACM/SIGMETRICS Conf.*, Washington, D.C., Dec. 1977.

Matick, R. E., *Computer Storage Systems and Technology*, Wiley, New York, 1977.

Matick, R. E., "Memory and Storage," *Introduction to Computer Architecture*, Stone, ed., SRA Inc., 1980, pp. 205–274.

Mattson, R. L., Gecsei, J., Slutz, D. R., and Traiger, I. L., "Evaluation Techniques for Storage Hierarchies," *IBM Systems Journ.*, 9, 1970, 78–117.

Mazare, G., "Multiprocessor Systems," *Proc. 1974 CERN School of Computing*, Godysund, Norway, Aug. 1974.

McGraw, J. R., "Data Flow Computing—Software Development," *IEEE Trans. on Computers*, Dec. 1980, pp. 1095–1103.

Mead, C., and Conway, L., *Introduction to VLSI Systems*, Addison-Wesley, Mass., 1980.

Miranker, G. S., "Implementation of Procedures on a Class of Data Flow Processors," *Proc. Int'l. Conf. Parallel Proc.*, IEEE no. 77CH 1253-4C, 1977, pp. 77–86.

Miura, K., and Uchida, K., "FACOM Vector Processor VP-100/VP-200," *Proc. NATO Advanced Research Workshop on High-Speed Computing*, Jülich, W. Germany, Springer-Verlag, June 20–22, 1983.

Moldovan, D. I., "On the Design of Algorithms for VLSI Systolic Array," *Proc. IEEE*, Jan. 1983, pp. 113–120.

Moto-oka, T., "Overview to the Fifth Generation Computer System Project," *Proc. 10th Ann. Symp. Computer Architecture*, June 1983, pp. 417–422.

Moto-oka, T., and Fuchi, K., "The Architectures in the Fifth Generation Computers," *Proc. 1983 IFIP Congress*, North-Holland, Amsterdam, 1983, pp. 589–602.

Mrosousky, I., Wong, J. Y., and Lampe, H. W., "Construction of a Large Field Simulator on a Vector Computer," *Journal of Petroleum Tech.*, Dec. 1980, pp. 2253–2264.

Mueller, P. T., Siegel, L. J., and Siegel, H. T., "Parallel Algorithms for the Two-dimensional FFT," *Proc. 5th Int'l. Conf. on Pattern Recog. and Image Proc.*, Dec. 1980, pp. 497–502.

Muntz, R. R., and Coffman, E. G., "Optimal Preemptive Scheduling on Two Processor Systems," *IEEE Trans. on Comp.*, C-18, Nov. 1969, pp. 1014–1020.

Muraoka, Y., "Parallelism Exposure and Exploitation in Programs," Ph.D. Thesis, Univ. of Ill. at Urb.-Champ., Dept. of Computer Science 71-424, Feb. 1971.

Myers, G. J., *Advances in Computer Architecture*, Wiley, New York, 1978.

Nassimi, D., and Sahni, S. H., "Data Broadcasting in SIMD Computers," *Proc. Int'l. Conf. Parallel Proc.*, Aug. 1980, pp. 325–326.

Nessett, D. M., "The Effectiveness of Cache Memories in a Multiprocessor Environment," *Australian Computer Journ.*, vol. 7, no. 1, Mar. 1975, pp. 33–38.

Newton, G., "Deadlock Prevention, Detection and Resolution: An Annotated Bibliography," *ACM Operating Sys. Review*, vol. 13, no. 2, Apr. 1979, pp. 33–44.

Newton, R. S., "An Exercise in Multiprocessor Operating System Design," *Agard Conf. Proc. No. 149 on Real-Time Computer-based Systems*, NATO Advisory Group on Aerospace R & D, Athens, Greece, May 1974.

Ni, L. M., "Performance Optimization of Parallel Processing Computer Systems," *Ph.D. Thesis*, School of Electrical Engineering, Purdue Univ., Ind., Dec. 1980.

Ni, L. M., and Hwang, K., "Performance Modeling of Shared Resource Array Processors," *IEEE Trans. on Soft. Eng.*, SE-7, no. 4, July 1981, pp. 386–394.

Ni, L. M., and Hwang, K., "Vector Reduction Methods for Arithmetic Pipeline," *Proc. 6th Symp. on Computer Arithmetic*, June 20–22, 1983, pp. 144–150.

Nolen, J. S., Kuba, D. W., and Kascic, M. J., Jr., "Application of Vector Processors to the Solution of Finite Difference Equations," *AIME 5th Symp. Reservoir Simulation*, Feb. 1979, pp. 37–44.

Nutt, G. J., "A Parallel Processor Operating System," *IEEE Trans. on Soft. Eng.*, SE-3, no. 6, Nov. 1977*a*, pp. 467–475.

Nutt, G. J., "Memory and Bus Conflict in an Array Processor," *IEEE Trans. on Comp.*, June 1977*b*, pp. 514–521.

Oleinick, P. N., The Implementation and Evaluation of Parallel Algorithms on C.mmp, Ph.D. Dissertation, Carnegie-Mellon Univ., 1978.

Oleinick, P. H., and Fuller, S. H., "The Implementation and Evaluation of a Parallel Algorithm on C.mmp," *Technical Report*, Carnegie-Mellon Univ. Computer Science Dept., Dec. 1977.

Orcutt, S. E., "Computer Organization and Algorithms for Very High-Speed Computations," *Ph.D. Thesis*, Stanford University, Calif., 1974.

Ousterhout, J. K., "Partitioning and Cooperation in a Distributed Multiprocessor Operating System: Medusa," *Ph.D. Thesis*, Carnegie-Mellon Univ., April 1980.

Owen, G. J., "Rollback—A Method of Process and System Recovery," *Proc. Conf. on Soft. Eng. for Telecommunication Switching Systems*, Colchester, England, Apr. 1973.

Owicki, S., and Gries, D., "Verifying Properties of Parallel Programs: An Axiomatic Approach," *Comm. of ACM*, vol. 19, 5, May 1976, pp. 279–85.

Padua, D. A., Kuck, D. J., and Lawrie, D. H., "High-Speed Multiprocessors and Compilation Techniques," *IEEE Trans. on Comp.*, C-29, Sept. 1980, pp. 763–776.

Panda, D. A., Kuck, D. J., and Lawrie, D. H., "High-Speed Multiprocessors and Compiling Techniques," *IEEE Trans. on Comp.*, Sept. 1980, pp. 763–776.

Parasuraman, B., "Pipelined Architectures for Microprocessor," *COMPCON Proc.*, 1976, pp. 225–228.

Parnas, D. L., "On the Criteria to Be Used in Decompositng Systems into Modules," *Comm. of ACM*, vol. 15, Dec. 1972.

Patel, J. H., "Improving the Throughput of Pipelines with Delays and Buffers," *Ph.D. Thesis*, University of Illinois at Urb.-Champ., 1976.

Patel, J. H., "Pipelines with Internal Buffers," *Proc. 5th Ann. Symp. on Computer Architecture*, Apr. 1978, pp. 249–254.

Patel, J. H., "Performance of Processor-Memory Interconnections for Multiprocessors," *IEEE Trans. on Comp.*, Oct. 1981, pp. 771–780.

Paul, G., "Large-Scale Vector/Array Processors," *IBM Research Report*, RC 7306, Sept. 1978 (24 pages).

Paul, G., and Wilson, M. W., *The VECTRAN Language: An Experimental Language for Vector/Matrix Array Processing*, IBM Palo Alto Scientific Center Report 6320-3334, Aug. 1975.

Pearce, R. C., and Majithia, J. C., "Analysis of a Shared Resource MIMD Computer Organization," *IEEE Trans. on Comp.*, C-27, no. 1, Jan. 1978, pp. 64–67.

Pease, M. C., "An Adaptation of the Fast Fourier Transform for Parallel Processing," *Journ. of ACM*, vol. 15, Apr. 1968, pp. 252–264.

Pease, M. C., "The Indirect Binary n-cube Microprocessor Array," *IEEE Trans. on Comp.*, C-25, May 1977, pp. 458–473.

Perrott, R. H., "A Language for Array and Vector Processors," *ACM Trans. on Programming Languages and Systems*, vol. 1, no. 2, Oct. 1979, pp. 177–195.

Peterson, J. L., "Petri Nets," *ACM Computing Surveys*, 3028: Sept. 1977, pp. 223–252.

Pradhan, D. K., and Kodandapani, K. L., "A Uniform Representation of Single- and Multistage Interconnection Networks Used in SIMD Machines," *IEEE Trans. on Comp.*, Sept. 1980, pp. 777–790.

Prasad, N. S., *Architecture and Implementation of Large Scale IBM Computer Systems*, Q.E.D. Information Sciences, Inc., Wellesley, Mass., 1981.

Preparata, F. P., "Parallelism in Sorting," *Proc. 1977 Int'l. Conf. on Parallel Proc.*, Detroit, Mich., Aug. 1977, pp. 202–206.

Preparata, F. P., and Vuillemin, J. E., "The Cube-Connected Cycles: A Versatile Network for Parallel Computation," *Proc. 20th Symp. Foundations of Computer Science*, 1979, pp. 140–147.

Preston, K., Duff, M. J. B., Levialdi, D. S., Norgren, P. E., and Toriwaki, J. I., "Basics of Cellular Logic With Some Applications in Medical Image Processing," *Proc. IEEE*, May 1979, pp. 826–856.

Prieve, B.B., and Fabry, R. S., "VMIN—An Optimal Variable-Space Page Replacement Algorithm," *Comm. of ACM*, vol. 19, May 1976, 295–297.

Purcell, C. J., "The Control Data STAR-100—Performance Measurements," *AFIPS NCC Proc.*, 1974, pp. 385–387.

Radoy, C. H., and Lipovski, G. J., "Switched Multiple Instruction Multiple Data Stream Processing," *Proc. 2d Ann. Symp. Computer Architecture*, 1974, pp. 183–187.

Ramamoorthy, C. V., Chandy, K. M., and Gonzalez, M. J., "Optimal Scheduling Strategies in a Multiprocessor System," *IEEE Trans. on Comp.*, C-21, 2, Feb. 1972, pp. 137–146.

Ramamoorthy, C. V., and Gonzalez, M. J., "Recognition and Representation of Parallel Processable Streams in Computer Programs, II (Task/Process Parallelism)," *Proc. ACM 24th Nat. Conf.*, ACM, New York, 1969, 387–397.

Ramamoorthy, C. V., and Kim, K. H., "Pipelining—The Generalized Concept and Sequencing Strategies," *NCC Proc.*, AFIPS Press, 1974, pp. 289–97.

Ramamoorthy, C. V., and Li, H. F., "Sequencing Control in Multifunctional Pipeline Systems," *Proc. 1975 Sagamore Comp. Conf. on Parallel Proc.*, 1975, pp. 79–89.

Ramamoorthy, C. V., and Li, H. F., "Pipeline Architecture," *ACM Computing Surveys*, vol. 9, no. 1, Mar. 1977, pp. 61–102.

Rao, G. S., "Performance Analysis of Cache Memories," *Journ. of Assoc. of Comp. Mach.*, vol. 25, no. 3, 1978, pp. 378–395.

Rau, B. R., and Rossman, G. E., "The Effect of Instruction Fetch Strategies upon the Performance of Pipelined Instruction Units," *Proc. 4th Ann. Symp. Computer Architecture*, IEEE 77CH 1182-5C, 1977, pp. 80–89.

Raw, B. R., "Program Behavior and the Performance of Interleaved Memories," *IEEE Trans. on Comp.*, C-28, no. 3, Mar. 1979, pp. 191–199.

Reilly, J., Sutton, A., Nasser, R., and Griscom, R., "Processor Controller for the IBM 3081," *IBM Journ. of Res. and Dev.*, vol. 26, no. 1, Jan., pp. 22–29.

Rice, J., *Matrix Computations and Mathematical Software*, McGraw-Hill, New York, 1981.

Ritchie, D. M., and Thompson, K., "The UNIX Time Sharing System," *Comm. of ACM*, vol. 17, July 1974, pp. 365–375.

Robinson, J. T., "Some Analysis Techniques for Asynchronous Multiprocessor Algorithms," *IEEE Trans. on Soft. Eng.*, Jan. 1979, pp. 24–30.

Rodrique, G., ed., *Parallel Computations*, Academic Press, New York, 1982.

Rodrique, G., Giroux, E. D., and Pratt, M., "Perspective on Large-Scale Scientific Computations," *IEEE Comp.*, Oct. 1980, pp. 65–80.

Roesser, R. P., "Two-Dimensional Microprocessor Pipelines for Image Processing," *IEEE Trans. on Comp.*, Feb. 1978, pp. 144–56.

Rohrbacher, D., and Potter, J. L., "Image Processing with STARAN Parallel Computer," *IEEE Comp.*, Aug., pp. 54–59.

Rosene, A. F., "Memory Allocation for Multiprocessors," *IEEE Trans. on Electronic Computers*, vol. 16, no. 5, Oct. 1967, pp. 659–665.

Rumbaugh, J., "A Data Flow Multiprocessor," *IEEE Trans. on Comp.*, C-26, no. 2, Feb. 1977, pp. 138–146.

Russell, E. C., "Automatic Program Analysis," *Ph.D. Thesis*, Dep. of Electrical Engineering, Univ. of Calif., Los Angeles, 1969.

Russell, R. M., "The Cray-1 Computer System," *Comm. of ACM*, Jan. 1978, pp. 63–72.

Saltzer, J. H., "A Simple Linear Model of Demand Paging Performance," *Comm. of ACM*, vol. 17, April 1974.

Saltzer, J. H., and Schroeder, M. D., "The Protection of Information in Computer Systems," *Proc. IEEE*, Sept. 1975, pp. 1238–1308.

Sameh, A. H., "Numerical Parallel Algorithms—A Survey," *High-Speed Computers and Algorithm Organization*, Kuck, et al., eds., Academic Press, 1977, pp. 207–228.

Sastry, K. V., and Kain, R. Y., "On the Performance of Certain Multiprocessor Computer Organizations," *IEEE Trans. on Comp.*, vol. C-24, no. 11, Nov. 1975, pp. 1066–1074.

Satyanarayanan, M., *Multiprocessors: A Comparative Study*, Prentice-Hall, Englewood Cliffs, N.J., 1980.

Schaefer, D. H., "Spatially Parallel Architectures: An Overview," *Computer Design*, Aug. 1982, pp. 117–124.

Schmid, H. A., "On the Efficient Implementation of Conditional Critical Regions and the Construction of Monitors," *Acta Informatica* 6, Springer-Verlag, 1976, pp. 227–249.

Schwartz, J. T., "Ultra-Computers," *ACM Trans. Programming Languages and Systems*, vol. 2, no. 4, 1980, pp. 484–521.

Senzig, D. N., and Smith, R. V., "Computer Organization for Array Processing," *AFIPS FJCC Proc.* (part I), 1965, pp. 117–128.

Sethi, A. S., and Deo, N., "Interference in Multiprocessor Systems with Localized Memory Access Probabilities," *IEEE Trans. on Comp.*, vol. C-28, no. 2, Feb. 1979.

Shapiro, H. D., "A Comparison of Various Methods for Detecting and Utilizing Parallelism in a Single Instruction Stream," *Proc. 1977 Int'l. Conf. Parallel Proc.*, IEEE No. 77CH 1253-4C, 1977, pp. 67–76.

Shar, L. E., "Design and Scheduling of Statistically Configured Pipelines," *Digital Systems*, Lab Report SU-SEL-72-042, Stanford University, Stanford, Calif., Sept. 1972.

Shar, L. E., and Davidson, E. S., "A Multiminiprocessor System Implemented Through Pipelining," *IEEE Comp.*, Feb. 1975, pp. 42–51.

Shen, J. P., and Hayes, J. P., "Fault Tolerance of a Class of Connecting Networks," *Proc. 7th Symp. Computer Architecture*, 1980, pp. 61–71.

Shoshani, A., and Coffman, E. G., Jr., "Sequencing Tasks in Multiprocess, Multiple Resource Systems to Avoid Deadlocks," *Proc. 11th Ann. Symp. Switching and Automata Theory*, Oct. 1970, pp. 225–233.

Siegel, H. J., "A Model of SIMD Machines and a Comparison of Various Interconnection Networks," *IEEE Trans. on Comp.*, vol. C-28, no. 12, Dec. 1979a, pp. 907–917.

Siege, H. J., "Interconnection Networks for SIMD Machines," *IEEE Comp.*, June 1979b, pp. 57–65.

Siegel, H. J., "The Theory Underlying the Partitioning of Permutation Networks," *IEEE Trans. on Comp.*, vol. C-29, no. 9, Sept. 1980, pp. 791–800.

Siegel, H. J., *Interconnection Networks for Large-Scale Parallel Processing: Theory and Case Studies*, Lexington Books, Lexington, Mass. 1984.

Siewiorek, D. P., et al., "A Case Study of C.mmp, Cm* and C.vmp. Part 1: Experience with Fault-Tolerance in Multiprocessor Systems," *Proc. IEEE*, vol. 66, no. 10, Oct. 1978, pp. 1178–1199.

Siewiorek, D., Bell, C. G., and Newell, A., *Principles of Computer Structures*, McGraw-Hill, New York, 1980.

Sites, R. L., "Operating Systems and Computer Architecture," in *Introduction to Computer Architecture* (Stone, ed.), SRA Inc., 1980, pp. 591–643.

Slotnick, D. L., "Unconventional Systems," *Computer Design*, Dec. 1982, pp. 49–52.

Slotnick, D. L., Borck, W. C., and McReynolds, R. C., "The SOLOMON Computer," *Proc. of AFIPS Fall Joint Comp. Conf.*, Wash. D.C., 1962, pp. 97–107.

Smith, A. J., "A Modified Working-Set Paging Algorithm," *IEEE Trans. on Comp.*, C-29, Sept. 1976, 907–914.

Smith, A. J., "Multiprocessor Memory Organization and Memory Interference," *Comm. of ACM*, vol. 20, no. 10, Oct. 1977, pp. 754–761.

Smith, A. J., "A Comparative Study of Set-Associative Memory Mapping Algorithms and Their use for Cache and Main Memory," *IEEE Trans. Soft. Eng.*, vol. SE-4, March 1978, pp. 121–130.

Smith, A. J., "Cache Memories," *ACM Computing Surveys*, vol. 14, no. 3, Sept. 1982, pp. 473–530.

Smith, B. J., "A Pipelined Shared Resources MIMD Computer," *Proc. 1978 Int'l. Conf. on Parallel Proc.*, 1978, pp. 6–8.

Smith, B. J., "Architecture and Applications of the HEP Multiprocessor Computer System," *Real Time Signal Processing IV*, vol. 298, Aug. 1981.

Smith, J. W., "Cooperation and Competition: An Approach to Parallel Computation," *Proceedings of Southeaston 1979*, Roanoake, Virg., Apr. 1979.

Snyder, L., "Introduction to the Configurable Highly Parallel Computer," *IEEE Comp.*, Jan. 1982, pp. 47–64.

Sperry Univac., *The Univac Series 1100 Announcement*, May 1982..

Steele, G. L., "Multiprocessing Compactifying Garbage Collection," *Comm. of ACM*, vol. 18, no. 9, Sept. 1975, pp. 495–508.

Stephenson, C. M., "Control of a Variable Configuration Pipelined Arithmetic Unit," *Proc. 11th Allerton Conf.*, Oct. 1973, pp. 558–567.

Stevens, K., "CFD—A FORTRAN-like Language for the Illiac IV," *SIGPLAN Notices*, March 1975, pp. 72–80.

Stevenson, D. K., "Numerical Algorithms for Parallel Computers," *Proc. Nat'l. Computer Conf.*, AFIPS Press, vol. 49, 1980, pp. 357–361.

Stokes, R. A., "Burroughs Scientific Processor," in *High Speed Computer and Algorithm Organization* (Kuck, et al., eds.) Academic Press, New York, 1977, pp. 85–89.

Stone, H. S., "Parallel Processing with a Perfect Shuffle," *IEEE Trans. on Comp.*, vol. C-20, Feb. 1971, pp. 153–161.

Stone, H. S., "An Efficient Parallel Algorithm for the Solution of a Tridiagonal Linear System of Equations," *Journ. of ACM*, vol. 20, 1973, pp. 27–38.

Stone, H. S., "Multiprocessor Scheduling with the Aid of Network Flow Algorithms," *IEEE Trans. on Soft. Eng.*, vol. SE-5, no. 1, Jan. 1977, pp. 85–93.

Stone, H. S., "Sorting on STAR," *IEEE Trans. on Comp.*, March 1978, pp. 138–46.

Stone, H. S., "Parallel Computers," Chap. 8 in *Introduction to Computer Architecture* (Stone, ed.), SRA, 1980, pp. 363–426.

Stout, Q. F., "Sorting, Merging, Selecting, and Filtering on Tree and Pyramid Machines," *Proc. 1983 Int'l. Conf. Parallel Processing*, 1983, pp. 214–221.

Strecker, W., "Cache Memories for PDP-11 Family Computers," *Proc. 3rd Symp. on Comp. Arch.*, 1976, 155–157.

Su, S. P., "Pipelining and Dataflow Techniques for Designing Supercomputers," *Ph.D. Thesis*, School of E.E., Purdue University, Dec. 1982.

Sugarman, R., "Superpower Computers," *IEEE Spectrum*, Apr. 1980, pp. 28–34.

Sutherland, I. E., and Mead, C. A., "Microelectronics and Computer Science," *Scientific American*, vol. 237, 1977, pp. 210–229.

Swan, R. J., Bechtholsheim, A., Lai, K. W., and Ousterhout, J. K., "The Implementation of the Cm* Multimicroprocessor," *Proc. AFIPS 1977 Nat. Comp. Conf.*, 46, AFIPS Press, Montvale, N.J., 1977, pp. 645–655.

Syre, J. C., Comte, D., and Hifdi, N., "Pipelining, Parallelism and Asynchronism in the LAU System," *Proc. 1977 Int. Conf. on Parallel Processing*, 1977, pp. 87–92.

Syre, J. C., et al., "The Data Driven LAU Multiprocessor System: Results and Perspectives," in *Information Processing 80* (Lavington, S. H., ed.), North Holland, New York, 1980.

Takahashi, N., and Amamiya, M., "A Dataflow Processor Array System: Design and Analysis," *Proc. of the 10th Int'l. Symp. on Computer Architecture*, June 13–17, 1983, pp. 243–251.

Tanenbaum, A., "Implication of Structured Programming for Computer Architecture," *Comm. of ACM, 21*, Mar. 1978, pp. 237–246.

Tang, C. K., "Cache System Design in the Tightly Coupled Multiprocessor System," *Proc. AFIPS 1976 Nat. Comp. Conf., 45*, AFIPS Press, Montvale, N.J., 1976, pp. 749–753.

Tanimoto, S. L., "A Pyramidal Approach to Parallel Processing," *Proc. 10th Annual Symp. Computer Architecture*, Sweden, 1983, pp. 372–378.

Tannenbaum, A. S., *Structured Computer Organization*, Prentice-Hall, Englewood Cliffs, N.J., 1976.

Tesler, L. G., and Enea, H., "A Language for Concurrent Processes," *Proc. SJCC*, AFIPS Press, 1968.

Texas Instruments, Inc., "Description of the ASC System: Parts 1 to 5, Manual Nos. 934662 to 934666, 1971.

Texas Instruments, Inc., *ASC FORTRAN Reference Manual*, Pub. No. 930044, 1972.

Theis, D. J., "Special Tutorial: Vector Supercomputers," *IEEE Comp.*, Apr. 1974, pp. 52–61.

Thomas, A. T., and Davidson, E. S., "Scheduling of Multiconfigurable Pipelines," *Proc. 12th Allerton Conf.*, Univ. of Illinois, Urbana, 1974, pp. 658–69.

Thomas, R. E., "A Dataflow Architecture with Improved Asymptotic Performance," *Ph.D. Thesis*, Dept. of Computer Science, Univ. of Calif., Irvine, Apr. 1981.

Thompson, C. D., "Generalized Connection Networks for Parallel Processor Intercommunication," *IEEE Trans. Comp.*, vol. C-27, no. 12, Dec. 1978, pp. 1119–1126.

Thompson, C. D., and Kung, H. T., "Sorting on a Mesh-Connected Parallel Computer," *Comm. of ACM*, vol. 20, no. 4, Apr. 1977, pp. 263–271.

Thompson, S. D., "A Complexity Theory for VLSI," *Ph.D. Thesis*, Dept. of Computer Science, Carnegie-Mellon University, Pittsburgh, Penn. Sept. 1980.

Thornton, J. E., *Design of a Computer, the Control Data 6600*, Scott, Foresman and Co., Glenview, Ill., 1970.

Thurber, K. J., *Large Scale Computer Architecture—Parallel and Associative Processors*, Hayden Book Co., N.J., 1976.

Thurber, K. J., "Parallel Processor Architectures—Part I: General Purpose System," *Computer Design*, Jan. 1979a, pp. 89–97.

Thurber, K. J., "Parallel Processor Architectures—Part II: Special Purpose Systems," *Computer Design*, Feb., 1979b, pp. 103–114.

Thurber, K. J., and Masson, G. M., *Distributed Processor Communication Architecture*, Lexington Books, Lexington, Mass., 1979.

Thurber, K. J., and Wald, L. D., "Associative and Parallel Processors," *ACM Computing Surveys*, vol. 7, Dec. 1975, pp. 215–255.

Tjaden, G. S., and Flynn, M. J., "Representation of Concurrency with Ordering Matrices," *IEEE Trans. on Comp.*, vol. C-22, no. 8, Aug. 1973, pp. 752–761.

Tokoro, M., "On the Working Set Concept for Dataflow Machine," *Proc. of 10th Ann. Symp. Computer Architecture*, June 1983, pp. 90–97.

Tomasulo, R. M., "An Efficient Algorithm for Exploiting Multiple Arithmetic Units," *IBM Journ. of Res. and Dev.*, vol. 11, no. 1, Jan. 1967, pp. 25–33.

Treleaven, P. C., "Exploiting Program Concurrency in Computing Systems," *IEEE Comp.*, 12, Jan. 1979, pp. 42–50.

Treleaven, P. C., Brownbridge, D. R., and Hopkins, R. P., "Data Driven and Demand-Driven Computer Architecture," *ACM Computing Surveys*, March 1982, pp. 93–144.

Ullman, J. D., *Computational Aspects of VLSI*, Computer Science Press, Rockville, Md., 1984.

Uhr, L., *Algorithm-Structured Computer Arrays and Networks*, Academic Press, New York, 1984.

Vick, C. R., and Merwin, R. E., "An Architecture Description of a Parallel Processing Element," *Proc. Int'l Workshop on Computer Architecture*, 1973.

Walker, L. L., "Multiprocessor Operating System Design," in *Operating Systems, International Computer State of the Art Report*, Infotech Ltd., Maidenhead, England, 1972.

Waser, S., and Flynn, M. T., *Introduction to Arithmetic for Digital Systems Designers*, Holt, Rinehart and Winston, New York, 1982.

Watson, R. W., *Timesharing System Design Concepts*, McGraw-Hill, New York, 1970.

Watson, W. J., "The TI ASC—A Highly Modular and Flexible Super Computer Architecture," *Proc. AFIPS Fall Joint Computer Conf.*, AFIPS Press, Montvale, N.J., 1972, pp. 221–228.

Watson, W. J., and Carr, H. M., "Operational Experiences with the TI Advanced Scientific Computer," *AFIPS NCC Proc.*, 1974, pp. 389–97.

Weckes, S., "A Design for a Multiple Processor Operating Environment," *Digest of Papers, COMPCON 73*, San Francisco, Calif., March 1973, pp. 143–146.

White, C. H. (ed.), *Multiprocessor Systems, International Computer State of the Art Report*, Infotech Ltd., Maidenhead, England, 1976.

Widdoes, L. C., Jr., "The S-1 Project: Developing High-Performance Digital Computers," *Digest of Papers:* IEEE Compcon 80, Spring 1980, pp. 282–291.

Wilkes, M. V., *Time-Sharing Computer System*, 2d ed., Elsevier, New York, 1972.

Wittmayer, W. R., "Array Processor Provides High Throughput Rates," *Computer Design*, March 1978, pp. 93–100.

Wu, C. L., and Feng, T. Y., "Fault Diagnosis for a Class of Multistage Interconnection Networks," *Proc. 1979 Int'l. Conf. Parallel Processing*, 1979, pp. 269–278.

Wu, C. L., and Feng, T. Y., "On a Class of Multistage Interconnection Networks," *IEEE Trans. on Comp.*, vol. C-29, no. 8, Aug. 1980, pp. 694–702.

Wu, C. L., and Feng, T. Y., "Universitility of the Shuffle Exchange Network," *IEEE Trans. on Computers*, vol. C-30, no. 5, May 1981, pp. 324–331.

Wulf, W. A., and Bell, C. G., "C.mmp—A Multi-miniprocessor," *Proc. AFIPS Fall Joint Computer Conference*, vol. 41, AFIPS Press, Montvale, N.J., 1972, pp. 765–777.

Wulf, W. A., et al., "Overview of the Hydra Operating System," in *Proc. of the 5th Symp. on Operating System Principles*, ACM, Nov. 1975, Austin, pp. 122–131.

Wulf, W. A., Levin, R., and Harbison, S. P., *HYDRA/C.mmp: An Experimental Computer System*, McGraw-Hill, N.Y., 1981.

Yau, S. S., and Fung, H. S., "Associative Processor Architecture—A Survey," *ACM Computing Surveys*, March 1977, vol. 9, no. 1, pp. 3–28.

Yeh, P. C., "Shared Cache Organization for Multiple-Stream Computer Systems," Coordinated Science Lab., Univ. of Ill., Tech. Rep. R-904, Jan. 1981.

Yeh, P. C., Patel, J. H., and Davidson, E. S., "Shared Cache for Multiple Stream Computer Systems," *IEEE Trans. on Comp.*, vol. C-32, no. 1, Jan. 1983, pp. 38–47.

INDEX